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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

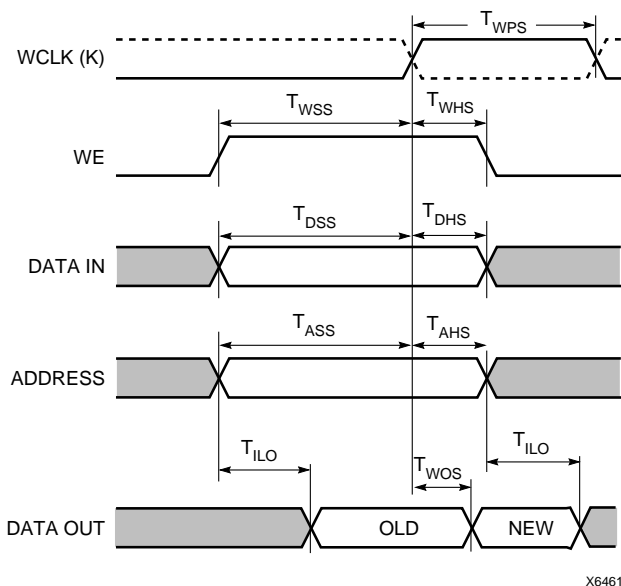
#### Details

|                                |                                                                                                                                       |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                              |
| Number of LABs/CLBs            | 100                                                                                                                                   |
| Number of Logic Elements/Cells | 238                                                                                                                                   |
| Total RAM Bits                 | 3200                                                                                                                                  |
| Number of I/O                  | 77                                                                                                                                    |
| Number of Gates                | 3000                                                                                                                                  |
| Voltage - Supply               | 4.5V ~ 5.5V                                                                                                                           |
| Mounting Type                  | Surface Mount                                                                                                                         |
| Operating Temperature          | -40°C ~ 100°C (TJ)                                                                                                                    |
| Package / Case                 | 100-TQFP                                                                                                                              |
| Supplier Device Package        | 100-VQFP (14x14)                                                                                                                      |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/xilinx/xc4003e-4vq100i">https://www.e-xfl.com/product-detail/xilinx/xc4003e-4vq100i</a> |

tions of the CLB, with the exception of the redefinition of the control signals. In 16x2 and 16x1 modes, the H' function generator can be used to implement Boolean functions of F', G', and D1, and the D flip-flops can latch the F', G', H', or D0 signals.

### Single-Port Edge-Triggered Mode

Edge-triggered (synchronous) RAM simplifies timing requirements. XC4000 Series edge-triggered RAM timing operates like writing to a data register. Data and address are presented. The register is enabled for writing by a logic High on the write enable input, WE. Then a rising or falling clock edge loads the data into the register, as shown in [Figure 3](#).



**Figure 3: Edge-Triggered RAM Write Timing**

Complex timing relationships between address, data, and write enable signals are not required, and the external write enable pulse becomes a simple clock enable. The active edge of WCLK latches the address, input data, and WE sig-

nals. An internal write pulse is generated that performs the write. See [Figure 4](#) and [Figure 5](#) for block diagrams of a CLB configured as 16x2 and 32x1 edge-triggered, single-port RAM.

The relationships between CLB pins and RAM inputs and outputs for single-port, edge-triggered mode are shown in [Table 5](#).

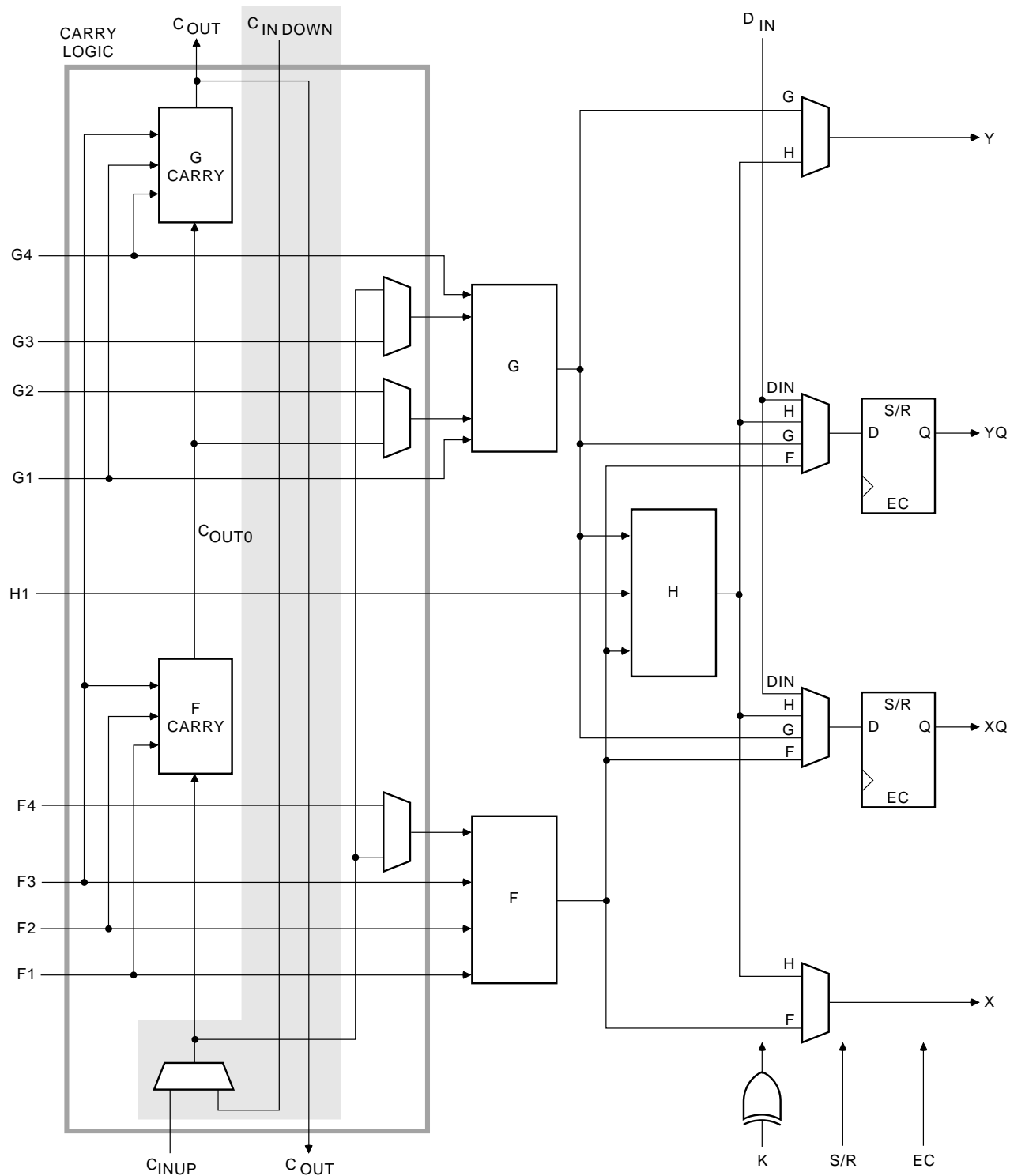
The Write Clock input (WCLK) can be configured as active on either the rising edge (default) or the falling edge. It uses the same CLB pin (K) used to clock the CLB flip-flops, but it can be independently inverted. Consequently, the RAM output can optionally be registered within the same CLB either by the same clock edge as the RAM, or by the opposite edge of this clock. The sense of WCLK applies to both function generators in the CLB when both are configured as RAM.

The WE pin is active-High and is not invertible within the CLB.

**Note:** The pulse following the active edge of WCLK ( $T_{WPS}$  in [Figure 3](#)) must be less than one millisecond wide. For most applications, this requirement is not overly restrictive; however, it must not be forgotten. Stopping WCLK at this point in the write cycle could result in excessive current and even damage to the larger devices if many CLBs are configured as edge-triggered RAM.

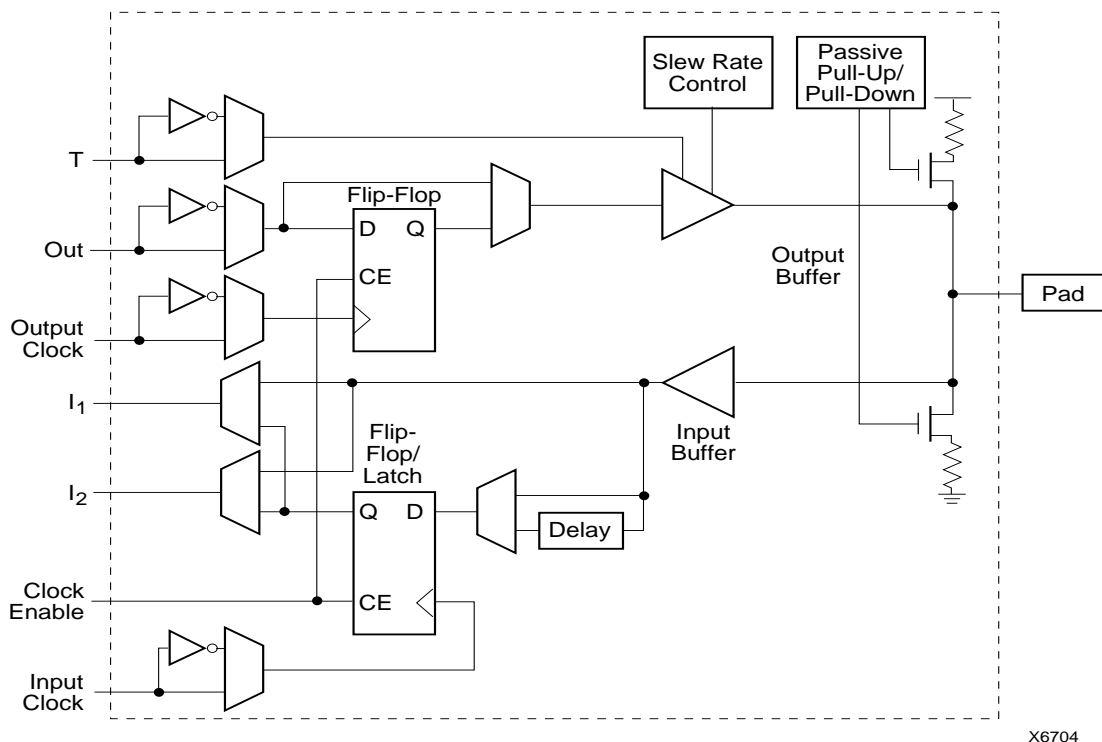
**Table 5: Single-Port Edge-Triggered RAM Signals**

| RAM Signal     | CLB Pin                          | Function                   |
|----------------|----------------------------------|----------------------------|
| D              | D0 or D1 (16x2, 16x1), D0 (32x1) | Data In                    |
| A[3:0]         | F1-F4 or G1-G4                   | Address                    |
| A[4]           | D1 (32x1)                        | Address                    |
| WE             | WE                               | Write Enable               |
| WCLK           | K                                | Clock                      |
| SPO (Data Out) | F' or G'                         | Single Port Out (Data Out) |

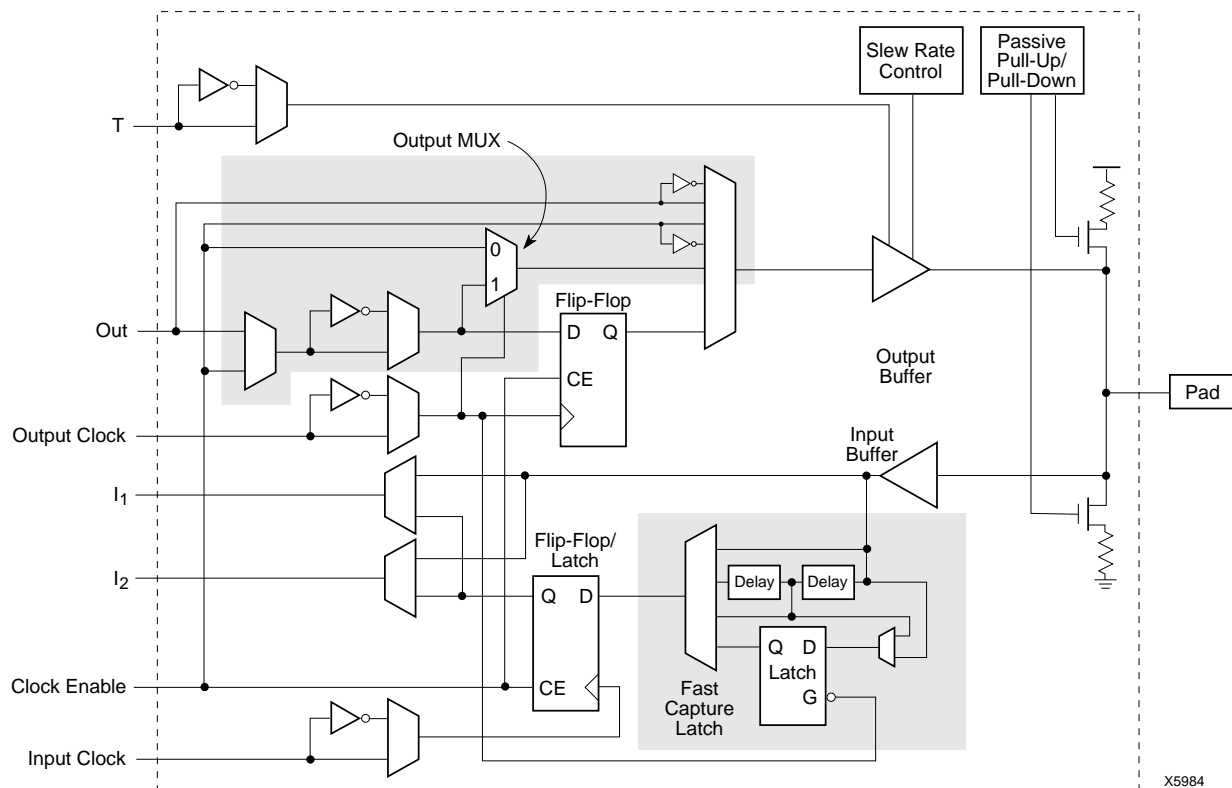


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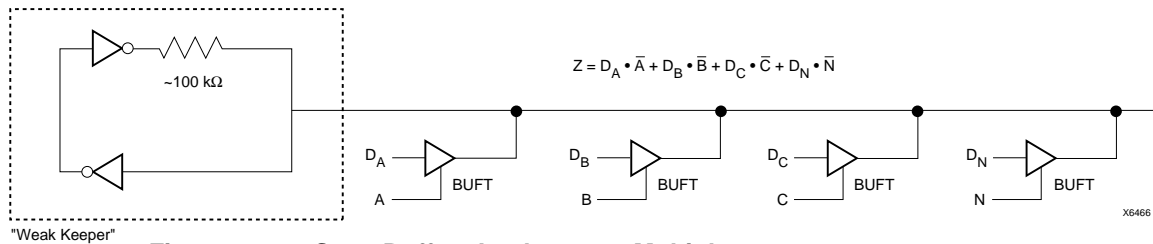
**Figure 13: Fast Carry Logic in XC4000E CLB (shaded area not present in XC4000X)**



**Figure 15: Simplified Block Diagram of XC4000E IOB**



**Figure 16: Simplified Block Diagram of XC4000X IOB (shaded areas indicate differences from XC4000E)**



**Figure 22: 3-State Buffers Implement a Multiplexer**

## Wide Edge Decoders

Dedicated decoder circuitry boosts the performance of wide decoding functions. When the address or data field is wider than the function generator inputs, FPGAs need multi-level decoding and are thus slower than PALs. XC4000 Series CLBs have nine inputs. Any decoder of up to nine inputs is, therefore, compact and fast. However, there is also a need for much wider decoders, especially for address decoding in large microprocessor systems.

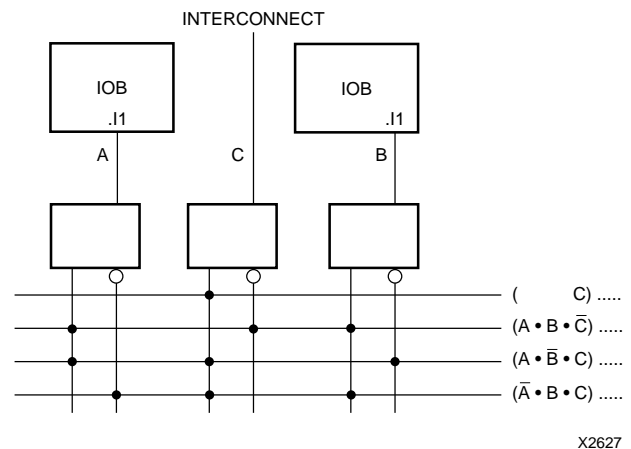
An XC4000 Series FPGA has four programmable decoders located on each edge of the device. The inputs to each decoder are any of the IOB I1 signals on that edge plus one local interconnect per CLB row or column. Each row or column of CLBs provides up to three variables or their complements., as shown in Figure 23. Each decoder generates a High output (resistor pull-up) when the AND condition of the selected inputs, or their complements, is true. This is analogous to a product term in typical PAL devices.

Each of these wired-AND gates is capable of accepting up to 42 inputs on the XC4005E and 72 on the XC4013E. There are up to 96 inputs for each decoder on the XC4028X and 132 on the XC4052X. The decoders may also be split in two when a larger number of narrower decoders are required, for a maximum of 32 decoders per device.

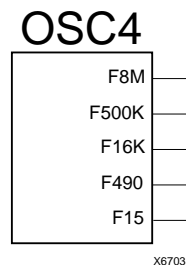
The decoder outputs can drive CLB inputs, so they can be combined with other logic to form a PAL-like AND/OR structure. The decoder outputs can also be routed directly to the chip outputs. For fastest speed, the output should be on the same chip edge as the decoder. Very large PALs can be emulated by ORing the decoder outputs in a CLB. This decoding feature covers what has long been considered a weakness of older FPGAs. Users often resorted to external PALs for simple but fast decoding functions. Now, the dedicated decoders in the XC4000 Series device can implement these functions fast and efficiently.

To use the wide edge decoders, place one or more of the WAND library symbols (WAND1, WAND4, WAND8, WAND16). Attach a DECODE attribute or property to each WAND symbol. Tie the outputs together and attach a PUL-

LUP symbol. Location attributes or properties such as L (left edge) or TR (right half of top edge) should also be used to ensure the correct placement of the decoder inputs.



**Figure 23: XC4000 Series Edge Decoding Example**



**Figure 24: XC4000 Series Oscillator Symbol**

## On-Chip Oscillator

XC4000 Series devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration modes. The oscillator runs at a nominal 8 MHz frequency that varies with process, Vcc, and temperature. The output frequency falls between 4 and 10 MHz.

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8 MHz clock, plus any two of 500 kHz, 16kHz, 490Hz and 15Hz (up to 10% lower for low-voltage devices). These frequencies can vary by as much as -50% or +25%.

These signals can be accessed by placing the OSC4 library element in a schematic or in HDL code (see [Figure 24](#)).

The oscillator is automatically disabled after configuration if the OSC4 symbol is not used in the design.

## Programmable Interconnect

All internal connections are composed of metal segments with programmable switching points and switching matrices to implement the desired routing. A structured, hierarchical matrix of routing resources is provided to achieve efficient automated routing.

The XC4000E and XC4000X share a basic interconnect structure. XC4000X devices, however, have additional routing not available in the XC4000E. The extra routing resources allow high utilization in high-capacity devices. All XC4000X-specific routing resources are clearly identified throughout this section. Any resources not identified as XC4000X-specific are present in all XC4000 Series devices.

This section describes the varied routing resources available in XC4000 Series devices. The implementation software automatically assigns the appropriate resources based on the density and timing requirements of the design.

## Interconnect Overview

There are several types of interconnect.

- CLB routing is associated with each row and column of the CLB array.
- IOB routing forms a ring (called a VersaRing) around the outside of the CLB array. It connects the I/O with the internal logic blocks.

- Global routing consists of dedicated networks primarily designed to distribute clocks throughout the device with minimum delay and skew. Global routing can also be used for other high-fanout signals.

Five interconnect types are distinguished by the relative length of their segments: single-length lines, double-length lines, quad and octal lines (XC4000X only), and longlines. In the XC4000X, direct connects allow fast data flow between adjacent CLBs, and between IOBs and CLBs.

Extra routing is included in the IOB pad ring. The XC4000X also includes a ring of octal interconnect lines near the IOBs to improve pin-swapping and routing to locked pins.

XC4000E/X devices include two types of global buffers. These global buffers have different properties, and are intended for different purposes. They are discussed in detail later in this section.

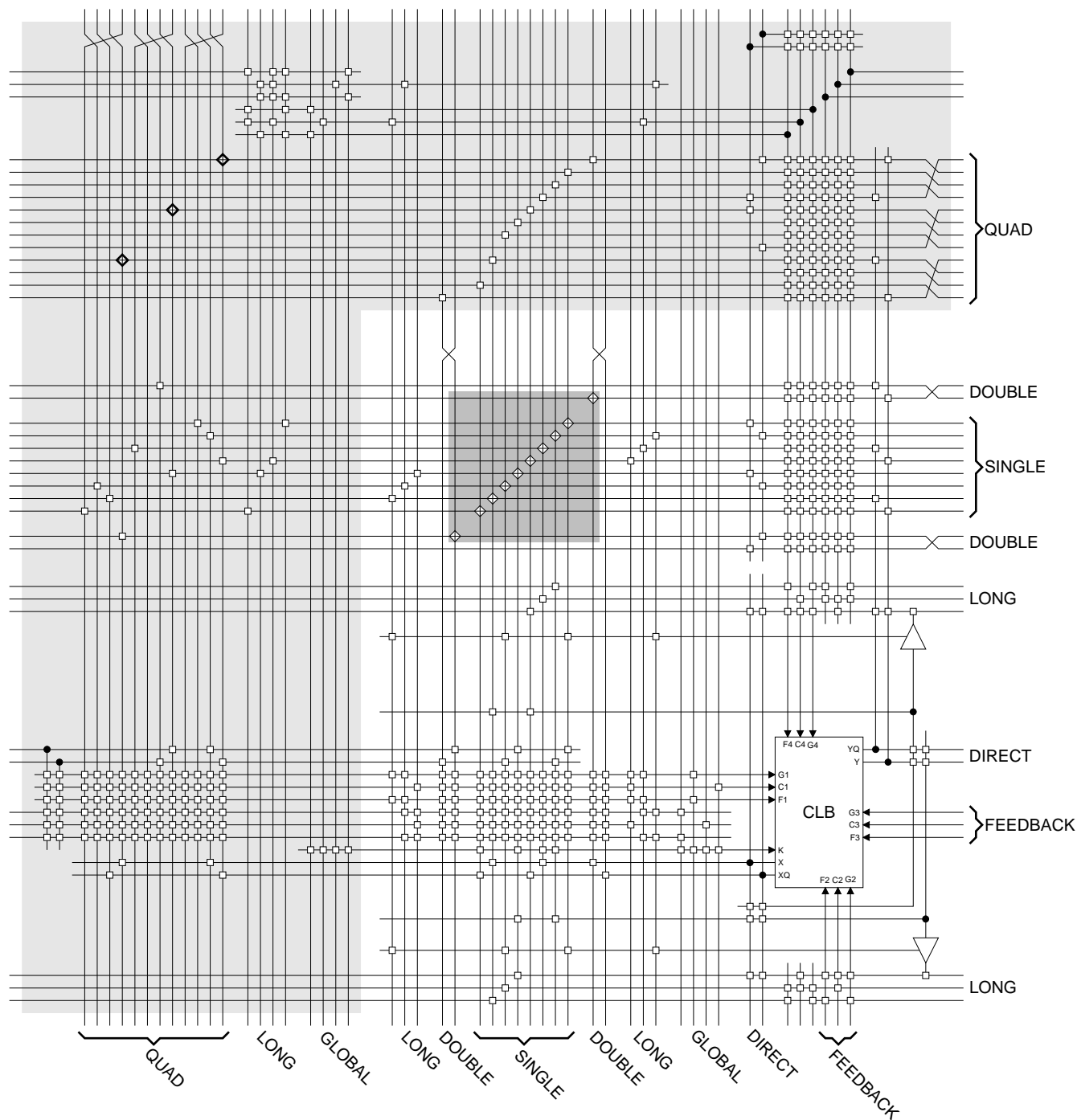
## CLB Routing Connections

A high-level diagram of the routing resources associated with one CLB is shown in [Figure 25](#). The shaded arrows represent routing present only in XC4000X devices.

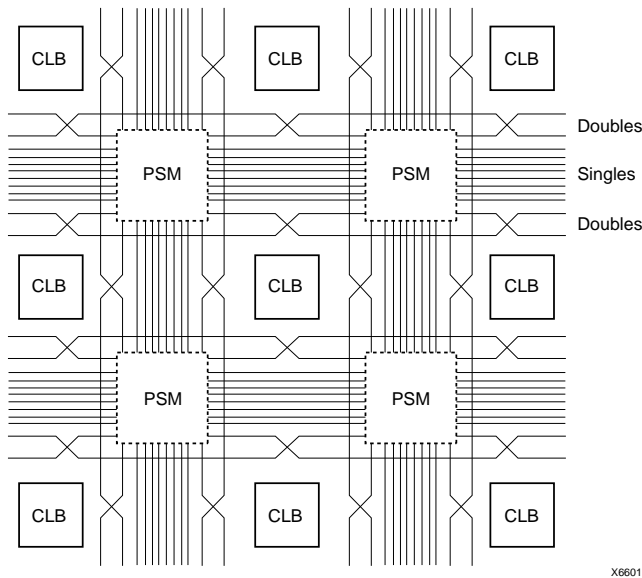
[Table 14](#) shows how much routing of each type is available in XC4000E and XC4000X CLB arrays. Clearly, very large designs, or designs with a great deal of interconnect, will route more easily in the XC4000X. Smaller XC4000E designs, typically requiring significantly less interconnect, do not require the additional routing.

[Figure 27 on page 30](#) is a detailed diagram of both the XC4000E and the XC4000X CLB, with associated routing. The shaded square is the programmable switch matrix, present in both the XC4000E and the XC4000X. The L-shaped shaded area is present only in XC4000X devices. As shown in the figure, the XC4000X block is essentially an XC4000E block with additional routing.

CLB inputs and outputs are distributed on all four sides, providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation.



**Figure 27: Detail of Programmable Interconnect Associated with XC4000 Series CLB**



**Figure 28: Single- and Double-Length Lines, with Programmable Switch Matrices (PSMs)**

### Double-Length Lines

The double-length lines consist of a grid of metal segments, each twice as long as the single-length lines: they run past two CLBs before entering a switch matrix. Double-length lines are grouped in pairs with the switch matrices staggered, so that each line goes through a switch matrix at every other row or column of CLBs (see [Figure 28](#)).

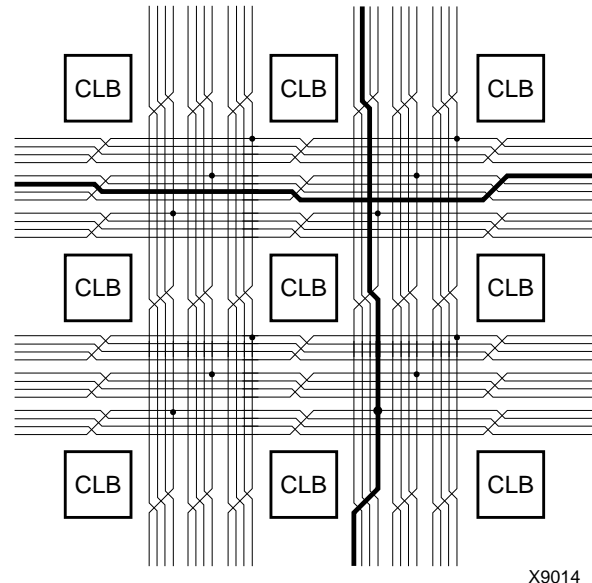
There are four vertical and four horizontal double-length lines associated with each CLB. These lines provide faster signal routing over intermediate distances, while retaining routing flexibility. Double-length lines are connected by way of the programmable switch matrices. Routing connectivity is shown in [Figure 27](#).

### Quad Lines (XC4000X only)

XC4000X devices also include twelve vertical and twelve horizontal quad lines per CLB row and column. Quad lines are four times as long as the single-length lines. They are interconnected via buffered switch matrices (shown as diamonds in [Figure 27 on page 30](#)). Quad lines run past four CLBs before entering a buffered switch matrix. They are grouped in fours, with the buffered switch matrices staggered, so that each line goes through a buffered switch matrix at every fourth CLB location in that row or column. (See [Figure 29](#).)

The buffered switch matrixes have four pins, one on each edge. All of the pins are bidirectional. Any pin can drive any or all of the other pins.

Each buffered switch matrix contains one buffer and six pass transistors. It resembles the programmable switch matrix shown in [Figure 26](#), with the addition of a programmable buffer. There can be up to two independent inputs



**Figure 29: Quad Lines (XC4000X only)**

and up to two independent outputs. Only one of the independent inputs can be buffered.

The place and route software automatically uses the timing requirements of the design to determine whether or not a quad line signal should be buffered. A heavily loaded signal is typically buffered, while a lightly loaded one is not. One scenario is to alternate buffers and pass transistors. This allows both vertical and horizontal quad lines to be buffered at alternating buffered switch matrices.

Due to the buffered switch matrices, quad lines are very fast. They provide the fastest available method of routing heavily loaded signals for long distances across the device.

### Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances. In XC4000X devices, quad lines are preferred for critical nets, because the buffered switch matrices make them faster for high fan-out nets.

Two horizontal longlines per CLB can be driven by 3-state or open-drain drivers (TBUFs). They can therefore implement unidirectional or bidirectional buses, wide multiplexers, or wired-AND functions. (See ["Three-State Buffers" on page 26](#) for more details.)

Each horizontal longline driven by TBUFs has either two (XC4000E) or eight (XC4000X) pull-up resistors. To activate these resistors, attach a PULLUP symbol to the long-line net. The software automatically activates the appropriate number of pull-ups. There is also a weak keeper at each end of these two horizontal longlines. This



circuit prevents undefined floating levels. However, it is overridden by any driver, even a pull-up resistor.

Each XC4000E longline has a programmable splitter switch at its center, as does each XC4000X longline driven by TBUFs. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Each XC4000X longline not driven by TBUFs has a buffered programmable splitter switch at the 1/4, 1/2, and 3/4 points of the array. Due to the buffering, XC4000X longline performance does not deteriorate with the larger array sizes. If the longline is split, the resulting partial longlines are independent.

Routing connectivity of the longlines is shown in [Figure 27 on page 30](#).

### **Direct Interconnect (XC4000X only)**

The XC4000X offers two direct, efficient and fast connections between adjacent CLBs. These nets facilitate a data flow from the left to the right side of the device, or from the top to the bottom, as shown in [Figure 30](#). Signals routed on the direct interconnect exhibit minimum interconnect propagation delay and use no general routing resources.

The direct interconnect is also present between CLBs and adjacent IOBs. Each IOB on the left and top device edges has a direct path to the nearest CLB. Each CLB on the right and bottom edges of the array has a direct path to the nearest two IOBs, since there are two IOBs for each row or column of CLBs.

The place and route software uses direct interconnect whenever possible, to maximize routing resources and minimize interconnect delays.



**Figure 30: XC4000X Direct Interconnect**

### **I/O Routing**

XC4000 Series devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines spanning two CLBs (four IOBs), and four longlines. Global lines and Wide Edge Decoder lines are provided. XC4000X devices also include eight octal lines.

A high-level diagram of the VersaRing is shown in [Figure 31](#). The shaded arrows represent routing present only in XC4000X devices.

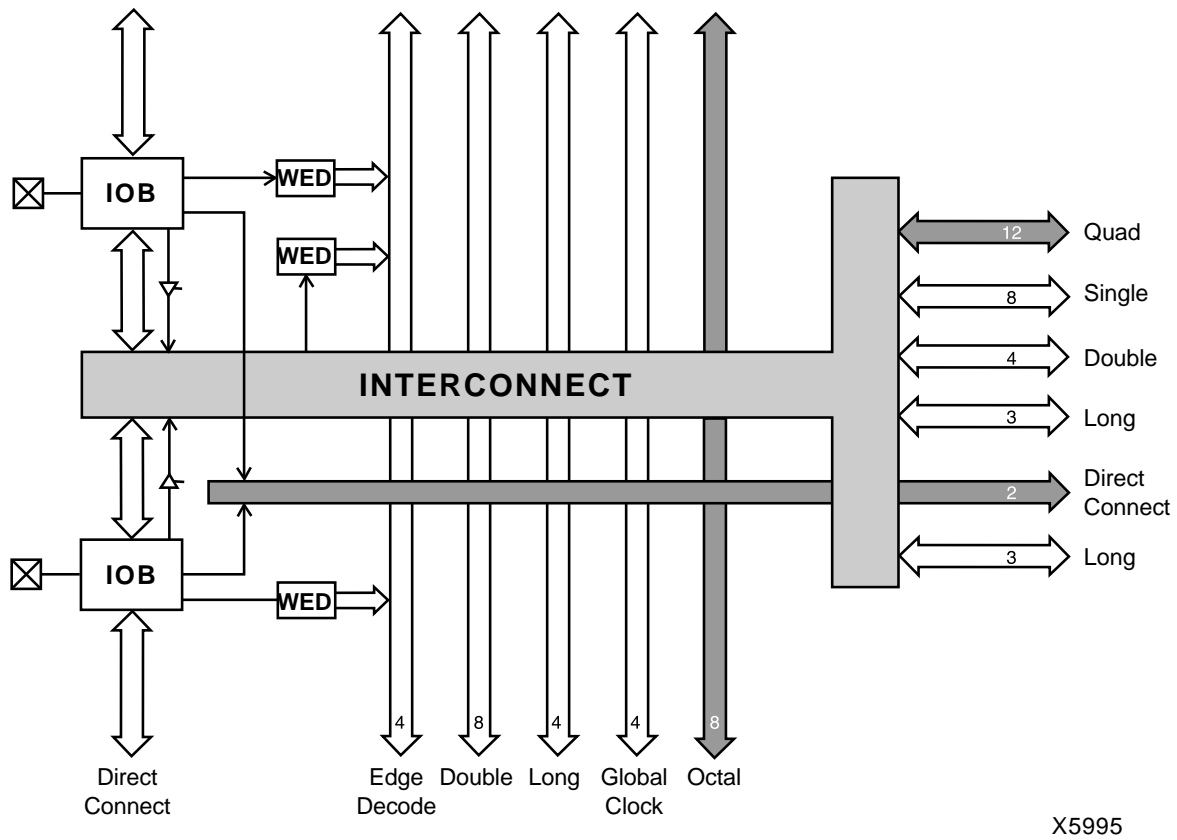
[Figure 33 on page 34](#) is a detailed diagram of the XC4000E and XC4000X VersaRing. The area shown includes two IOBs. There are two IOBs per CLB row or column, therefore this diagram corresponds to the CLB routing diagram shown in [Figure 27 on page 30](#). The shaded areas represent routing and routing connections present only in XC4000X devices.

### **Octal I/O Routing (XC4000X only)**

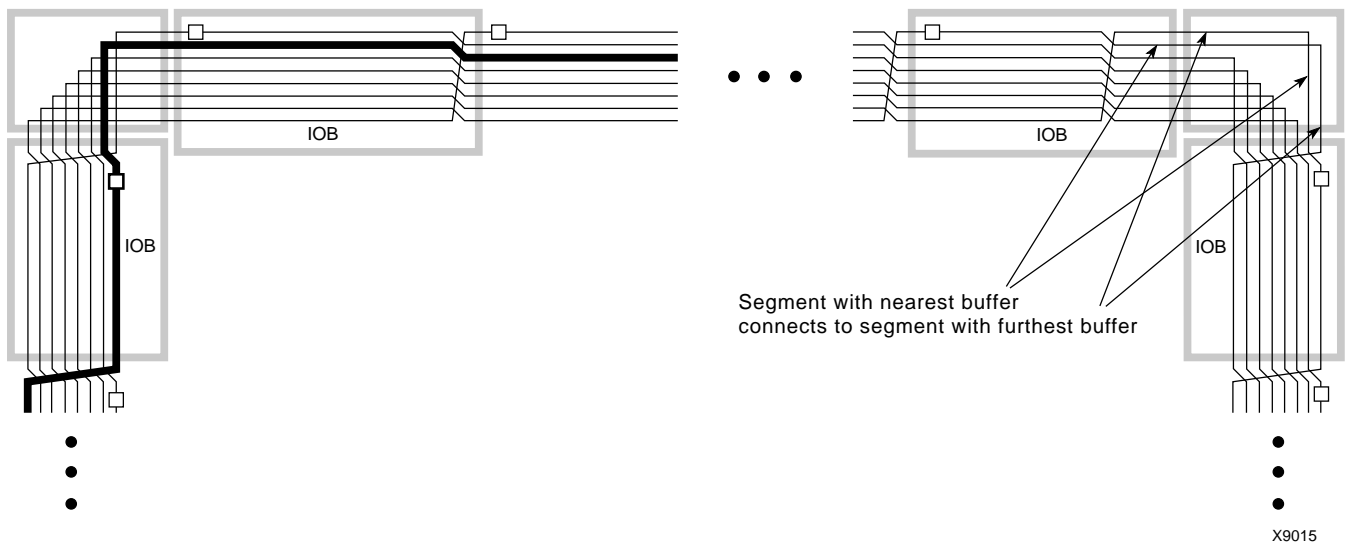
Between the XC4000X CLB array and the pad ring, eight interconnect tracks provide for versatility in pin assignment and fixed pinout flexibility. (See [Figure 32 on page 33](#).)

These routing tracks are called octals, because they can be broken every eight CLBs (sixteen IOBs) by a programmable buffer that also functions as a splitter switch. The buffers are staggered, so each line goes through a buffer at every eighth CLB location around the device edge.

The octal lines bend around the corners of the device. The lines cross at the corners in such a way that the segment most recently buffered before the turn has the farthest distance to travel before the next buffer, as shown in [Figure 32](#).



**Figure 31: High-Level Routing Diagram of XC4000 Series VersaRing (Left Edge)**  
WED = Wide Edge Decoder, IOB = I/O Block (shaded arrows indicate XC4000X only)



**Figure 32: XC4000X Octal I/O Routing**

IOB inputs and outputs interface with the octal lines via the single-length interconnect lines. Single-length lines are also used for communication between the octals and double-length lines, quads, and longlines within the CLB array.

Segmentation into buffered octals was found to be optimal for distributing signals over long distances around the device.

### Global Nets and Buffers

Both the XC4000E and the XC4000X have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew. The global buffers are described in detail in the following sections. The text descriptions and diagrams are summarized in [Table 15](#). The table shows which CLB and IOB clock pins can be sourced by which global buffers.

In both XC4000E and XC4000X devices, placement of a library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. The detailed information in these sections is included only for reference.

#### Global Nets and Buffers (XC4000E only)

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. The four global lines can be driven by either of two types of global buffers. The clock pins of every CLB and IOB can also be sourced from local interconnect.

Two different types of clock buffers are available in the XC4000E:

- Primary Global Buffers (BUFGP)
- Secondary Global Buffers (BUFGS)

Four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs.

The Primary Global buffers must be driven by the semi-dedicated pads. The Secondary Global buffers can be sourced by either semi-dedicated pads or internal nets.

Each CLB column has four dedicated vertical Global lines. Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in [Figure 34](#). Each corner of the device has one Primary buffer and one Secondary buffer.

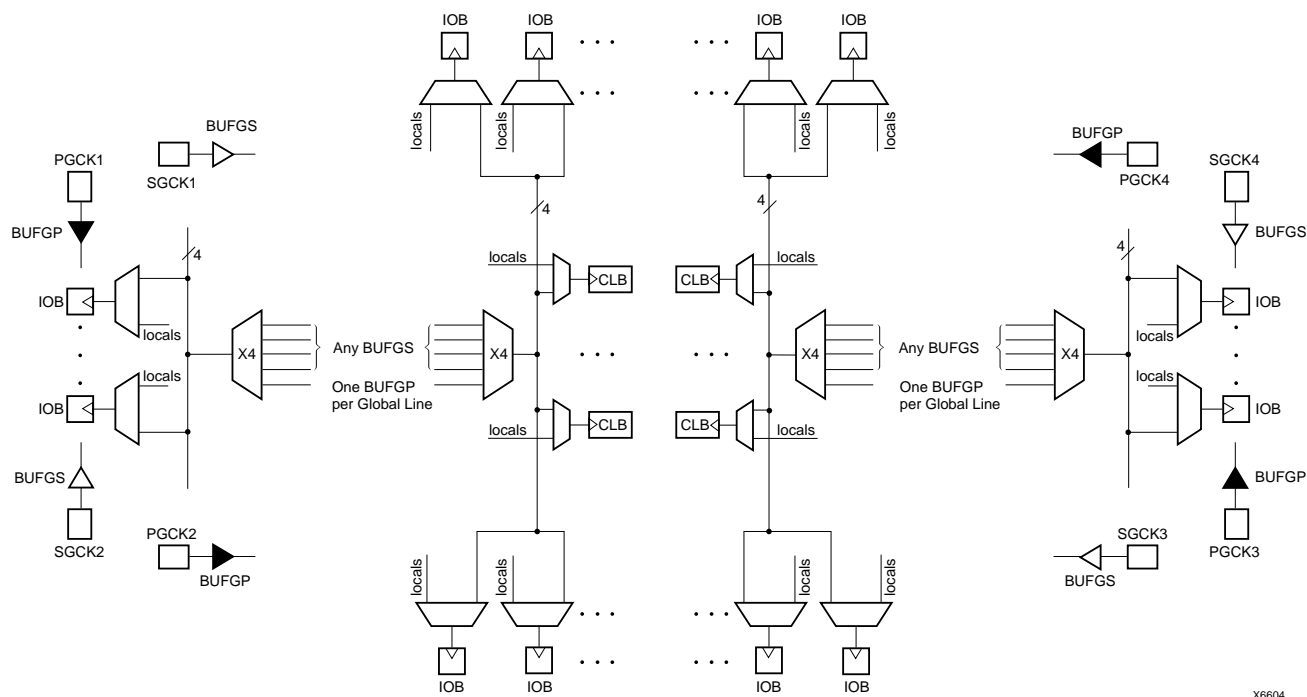
IOBs along the left and right edges have four vertical global longlines. Top and bottom IOBs can be clocked from the global lines in the adjacent CLB column.

A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), or BUFG (either primary or secondary buffer) element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=L attribute or property to a BUFGS symbol to direct that a buffer be placed in one of the two Secondary Global buffers on the left edge of the device, or a LOC=BL to indicate the Secondary Global buffer on the bottom edge of the device, on the left.

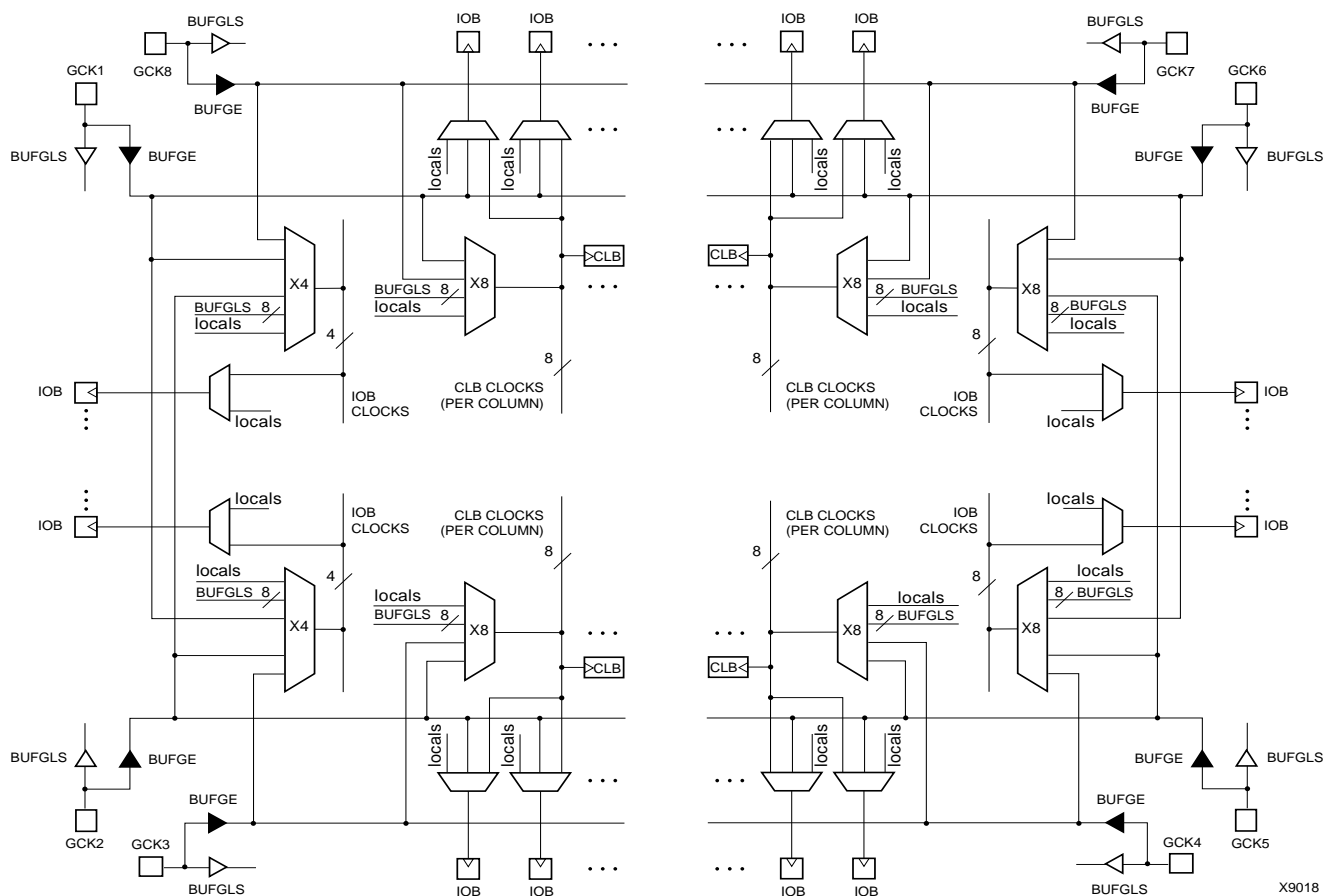
**Table 15: Clock Pin Access**

|                                                             | XC4000E |       | XC4000X |             |             | Local Inter-connect |
|-------------------------------------------------------------|---------|-------|---------|-------------|-------------|---------------------|
|                                                             | BUFGP   | BUFGS | BUFGLS  | L & R BUFGE | T & B BUFGE |                     |
| All CLBs in Quadrant                                        | √       | √     | √       | √           | √           | √                   |
| All CLBs in Device                                          | √       | √     | √       |             |             | √                   |
| IOBs on Adjacent Vertical Half Edge                         | √       | √     | √       | √           | √           | √                   |
| IOBs on Adjacent Vertical Full Edge                         | √       | √     | √       | √           |             | √                   |
| IOBs on Adjacent Horizontal Half Edge (Direct)              |         |       |         | √           |             | √                   |
| IOBs on Adjacent Horizontal Half Edge (through CLB globals) | √       | √     | √       | √           | √           | √                   |
| IOBs on Adjacent Horizontal Full Edge (through CLB globals) | √       | √     | √       |             |             | √                   |

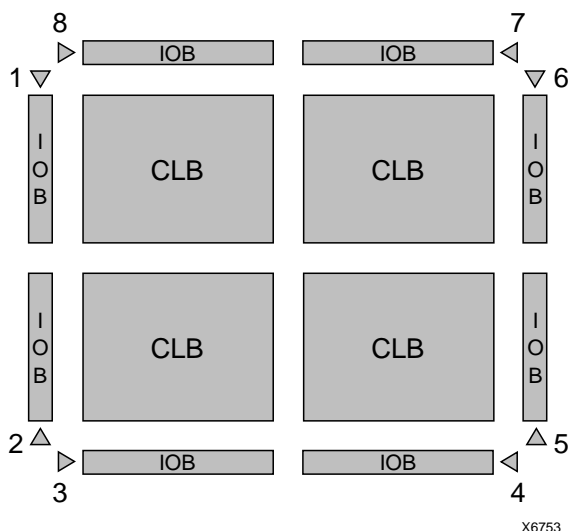
L = Left, R = Right, T = Top, B = Bottom



**Figure 34: XC4000E Global Net Distribution**



**Figure 35: XC4000X Global Net Distribution**



**Figure 36: Any BUFGLS (GCK1 - GCK8) Can Drive Any or All Clock Inputs on the Device**

### Global Early Buffers

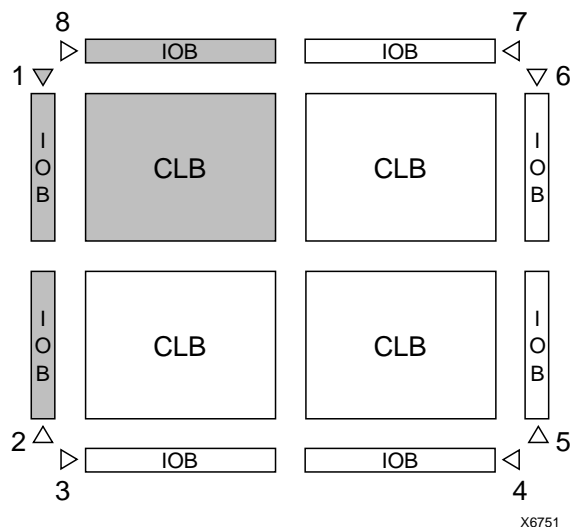
Each corner of the XC4000X device has two Global Early buffers. The primary purpose of the Global Early buffers is to provide an earlier clock access than the potentially heavily-loaded Global Low-Skew buffers. A clock source applied to both buffers will result in the Global Early clock edge occurring several nanoseconds earlier than the Global Low-Skew buffer clock edge, due to the lighter loading.

Global Early buffers also facilitate the fast capture of device inputs, using the Fast Capture latches described in “**IOB Input Signals**” on page 20. For Fast Capture, take a single clock signal, and route it through both a Global Early buffer and a Global Low-Skew buffer. (The two buffers share an input pad.) Use the Global Early buffer to clock the Fast Capture latch, and the Global Low-Skew buffer to clock the normal input flip-flop or latch, as shown in **Figure 17** on page 23.

The Global Early buffers can also be used to provide a fast Clock-to-Out on device output pins. However, an early clock in the output flip-flop IOB must be taken into consideration when calculating the internal clock speed for the design.

The Global Early buffers at the left and right edges of the chip have slightly different capabilities than the ones at the top and bottom. Refer to **Figure 37**, **Figure 38**, and **Figure 35** on page 36 while reading the following explanation.

Each Global Early buffer can access the eight vertical Global lines for all CLBs in the quadrant. Therefore, only one-fourth of the CLB clock pins can be accessed. This restriction is in large part responsible for the faster speed of the buffers, relative to the Global Low-Skew buffers.

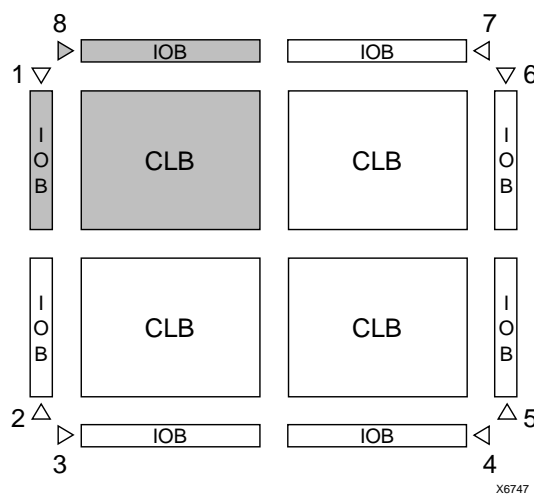


**Figure 37: Left and Right BUFGEs Can Drive Any or All Clock Inputs in Same Quadrant or Edge (GCK1 is shown. GCK2, GCK5 and GCK6 are similar.)**

The left-side Global Early buffers can each drive two of the four vertical lines accessing the IOBs on the entire left edge of the device. The right-side Global Early buffers can each drive two of the eight vertical lines accessing the IOBs on the entire right edge of the device. (See **Figure 37**.)

Each left and right Global Early buffer can also drive half of the IOBs along either the top or bottom edge of the device, using a dedicated line that can only be accessed through the Global Early buffers.

The top and bottom Global Early buffers can drive half of the IOBs along either the left or right edge of the device, as shown in **Figure 38**. They can only access the top and bottom IOBs via the CLB global lines.



**Figure 38: Top and Bottom BUFGEs Can Drive Any or All Clock Inputs in Same Quadrant (GCK8 is shown. GCK3, GCK4 and GCK7 are similar.)**

**Figure 41 on page 44** is a diagram of the XC4000 Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

XC4000 Series devices can also be configured through the boundary scan logic. See “Readback” on page 55.

## Data Registers

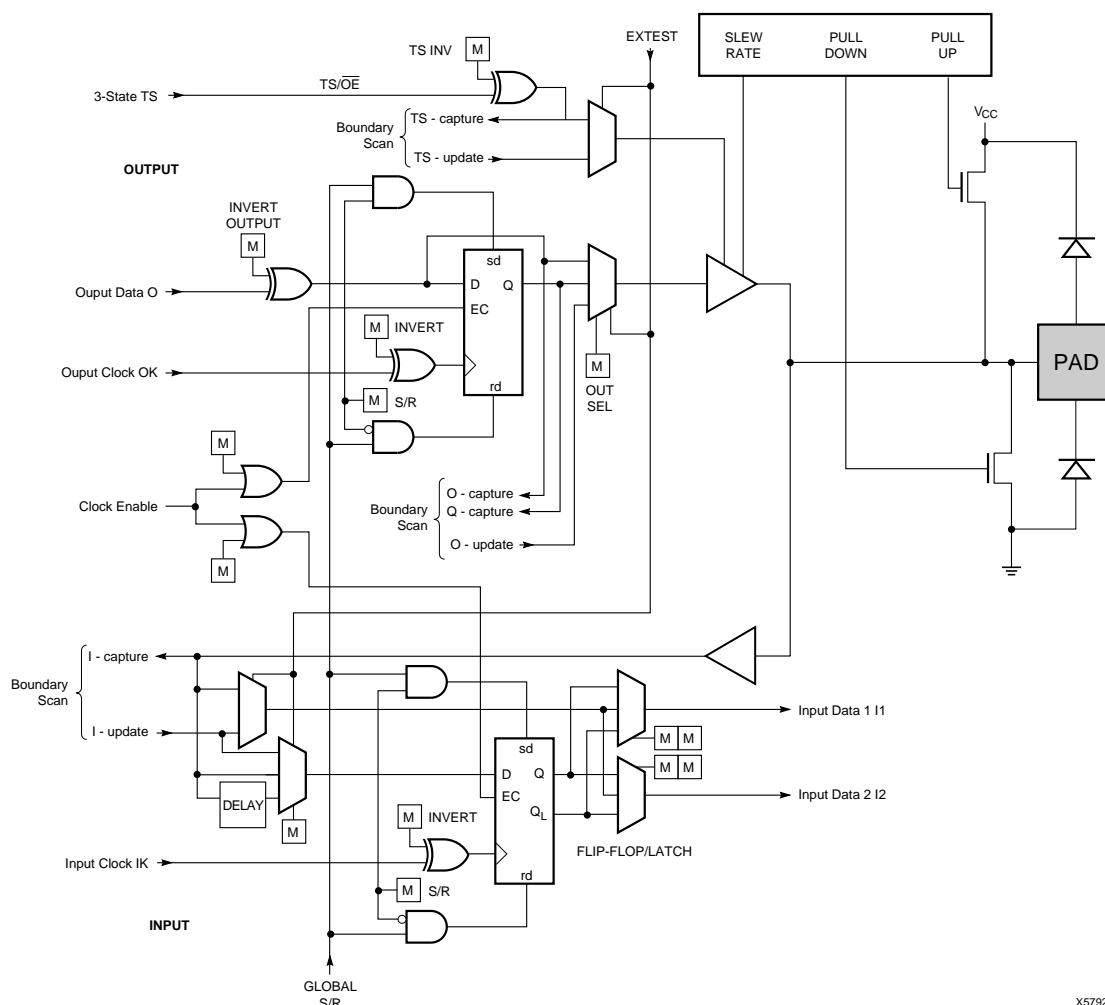
The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-State Control. Non-IOB pins have appropriate partial bit population for In or Out only.  $\overline{\text{PROGRAM}}$ , CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the

data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).



**Figure 40: Block Diagram of XC4000E IOB with Boundary Scan (some details not shown). XC4000X Boundary Scan Logic is Identical.**

is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received. **Figure 47 on page 53** shows the start-up timing for an XC4000 Series device.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM file formatter must be used to combine the bitstreams for a daisy-chained configuration.

### Multi-Family Daisy Chain

All Xilinx FPGAs of the XC2000, XC3000, and XC4000 Series use a compatible bitstream format and can, therefore, be connected in a daisy chain in an arbitrary sequence. There is, however, one limitation. The lead device must belong to the highest family in the chain. If the chain contains XC4000 Series devices, the master normally cannot be an XC2000 or XC3000 device.

The reason for this rule is shown in **Figure 47 on page 53**. Since all devices in the chain store the same length count value and generate or receive one common sequence of CCLK pulses, they all recognize length-count match on the same CCLK edge, as indicated on the left edge of **Figure 47**. The master device then generates additional CCLK pulses until it reaches its finish point F. The different families generate or require different numbers of additional CCLK pulses until they reach F. Not reaching F means that the device does not really finish its configuration, although DONE may have gone High, the outputs became active, and the internal reset was released. For the XC4000 Series device, not reaching F means that readback cannot be ini-

tiated and most boundary scan instructions cannot be used.

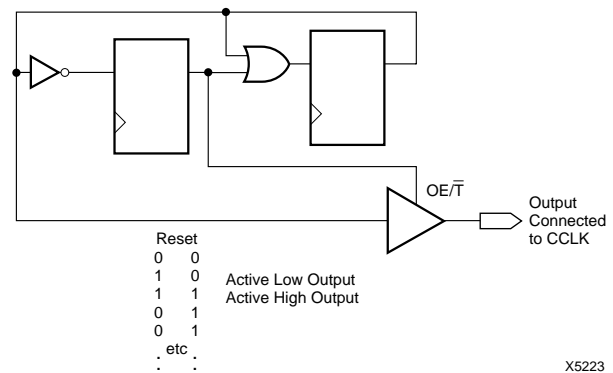
The user has some control over the relative timing of these events and can, therefore, make sure that they occur at the proper time and the finish point F is reached. Timing is controlled using options in the bitstream generation software.

### XC3000 Master with an XC4000 Series Slave

Some designers want to use an inexpensive lead device in peripheral mode and have the more precious I/O pins of the XC4000 Series devices all available for user I/O. **Figure 44** provides a solution for that case.

This solution requires one CLB, one IOB and pin, and an internal oscillator with a frequency of up to 5 MHz as a clock source. The XC3000 master device must be configured with late Internal Reset, which is the default option.

One CLB and one IOB in the lead XC3000-family device are used to generate the additional CCLK pulse required by the XC4000 Series devices. When the lead device removes the internal RESET signal, the 2-bit shift register responds to its clock input and generates an active Low output signal for the duration of the subsequent clock period. An external connection between this output and CCLK thus creates the extra CCLK pulse.



**Figure 44: CCLK Generation for XC3000 Master Driving an XC4000 Series Slave**



**Table 22: Pin Functions During Configuration**

| CONFIGURATION MODE <M2:M1:M0> |                          |                              |                               |                                 |                               | USER OPERATION |
|-------------------------------|--------------------------|------------------------------|-------------------------------|---------------------------------|-------------------------------|----------------|
| SLAVE SERIAL<br><1:1:1>       | MASTER SERIAL<br><0:0:0> | SYNCH. PERIPHERAL<br><0:1:1> | ASYNCH. PERIPHERAL<br><1:0:1> | MASTER PARALLEL DOWN<br><1:1:0> | MASTER PARALLEL UP<br><1:0:0> |                |
| M2(HIGH) (I)                  | M2(LOW) (I)              | M2(LOW) (I)                  | M2(HIGH) (I)                  | M2(HIGH) (I)                    | M2(HIGH) (I)                  | (I)            |
| M1(HIGH) (I)                  | M1(LOW) (I)              | M1(HIGH) (I)                 | M1(LOW) (I)                   | M1(HIGH) (I)                    | M1(LOW) (I)                   | (O)            |
| M0(HIGH) (I)                  | M0(LOW) (I)              | M0(HIGH) (I)                 | M0(HIGH) (I)                  | M0(LOW) (I)                     | M0(LOW) (I)                   | (I)            |
| HDC (HIGH)                    | HDC (HIGH)               | HDC (HIGH)                   | HDC (HIGH)                    | HDC (HIGH)                      | HDC (HIGH)                    | I/O            |
| LDC (LOW)                     | LDC (LOW)                | LDC (LOW)                    | LDC (LOW)                     | LDC (LOW)                       | LDC (LOW)                     | I/O            |
| INIT                          | INIT                     | INIT                         | INIT                          | INIT                            | INIT                          | I/O            |
| DONE                          | DONE                     | DONE                         | DONE                          | DONE                            | DONE                          | DONE           |
| PROGRAM (I)                   | PROGRAM (I)              | PROGRAM (I)                  | PROGRAM (I)                   | PROGRAM (I)                     | PROGRAM (I)                   | PROGRAM        |
| CCLK (I)                      | CCLK (O)                 | CCLK (I)                     | CCLK (O)                      | CCLK (O)                        | CCLK (O)                      | CCLK (I)       |
|                               |                          | RDY/BUSY (O)                 | RDY/BUSY (O)                  | RCLK (O)                        | RCLK (O)                      | I/O            |
|                               |                          |                              | RS (I)                        |                                 |                               | I/O            |
|                               |                          |                              | CS0 (I)                       |                                 |                               | I/O            |
|                               |                          | DATA 7 (I)                   | DATA 7 (I)                    | DATA 7 (I)                      | DATA 7 (I)                    | I/O            |
|                               |                          | DATA 6 (I)                   | DATA 6 (I)                    | DATA 6 (I)                      | DATA 6 (I)                    | I/O            |
|                               |                          | DATA 5 (I)                   | DATA 5 (I)                    | DATA 5 (I)                      | DATA 5 (I)                    | I/O            |
|                               |                          | DATA 4 (I)                   | DATA 4 (I)                    | DATA 4 (I)                      | DATA 4 (I)                    | I/O            |
|                               |                          | DATA 3 (I)                   | DATA 3 (I)                    | DATA 3 (I)                      | DATA 3 (I)                    | I/O            |
|                               |                          | DATA 2 (I)                   | DATA 2 (I)                    | DATA 2 (I)                      | DATA 2 (I)                    | I/O            |
|                               |                          | DATA 1 (I)                   | DATA 1 (I)                    | DATA 1 (I)                      | DATA 1 (I)                    | I/O            |
| DIN (I)                       | DIN (I)                  | DATA 0 (I)                   | DATA 0 (I)                    | DATA 0 (I)                      | DATA 0 (I)                    | I/O            |
| DOUT                          | DOUT                     | DOUT                         | DOUT                          | DOUT                            | DOUT                          | SGCK4-GCK6-I/O |
| TDI                           | TDI                      | TDI                          | TDI                           | TDI                             | TDI                           | TDI-I/O        |
| TCK                           | TCK                      | TCK                          | TCK                           | TCK                             | TCK                           | TCK-I/O        |
| TMS                           | TMS                      | TMS                          | TMS                           | TMS                             | TMS                           | TMS-I/O        |
| TDO                           | TDO                      | TDO                          | TDO                           | TDO                             | TDO                           | TDO-(O)        |
|                               |                          |                              | WS (I)                        | A0                              | A0                            | I/O            |
|                               |                          |                              |                               | A1                              | A1                            | PGCK4-GCK7-I/O |
|                               |                          |                              | CS1                           | A2                              | A2                            | I/O            |
|                               |                          |                              |                               | A3                              | A3                            | I/O            |
|                               |                          |                              |                               | A4                              | A4                            | I/O            |
|                               |                          |                              |                               | A5                              | A5                            | I/O            |
|                               |                          |                              |                               | A6                              | A6                            | I/O            |
|                               |                          |                              |                               | A7                              | A7                            | I/O            |
|                               |                          |                              |                               | A8                              | A8                            | I/O            |
|                               |                          |                              |                               | A9                              | A9                            | I/O            |
|                               |                          |                              |                               | A10                             | A10                           | I/O            |
|                               |                          |                              |                               | A11                             | A11                           | I/O            |
|                               |                          |                              |                               | A12                             | A12                           | I/O            |
|                               |                          |                              |                               | A13                             | A13                           | I/O            |
|                               |                          |                              |                               | A14                             | A14                           | I/O            |
|                               |                          |                              |                               | A15                             | A15                           | SGCK1-GCK8-I/O |
|                               |                          |                              |                               | A16                             | A16                           | PGCK1-GCK1-I/O |
|                               |                          |                              |                               | A17                             | A17                           | I/O            |
|                               |                          |                              |                               | A18*                            | A18*                          | I/O            |
|                               |                          |                              |                               | A19*                            | A19*                          | I/O            |
|                               |                          |                              |                               | A20*                            | A20*                          | I/O            |
|                               |                          |                              |                               | A21*                            | A21*                          | I/O            |
|                               |                          |                              |                               |                                 |                               | ALL OTHERS     |



## Synchronous Peripheral Mode

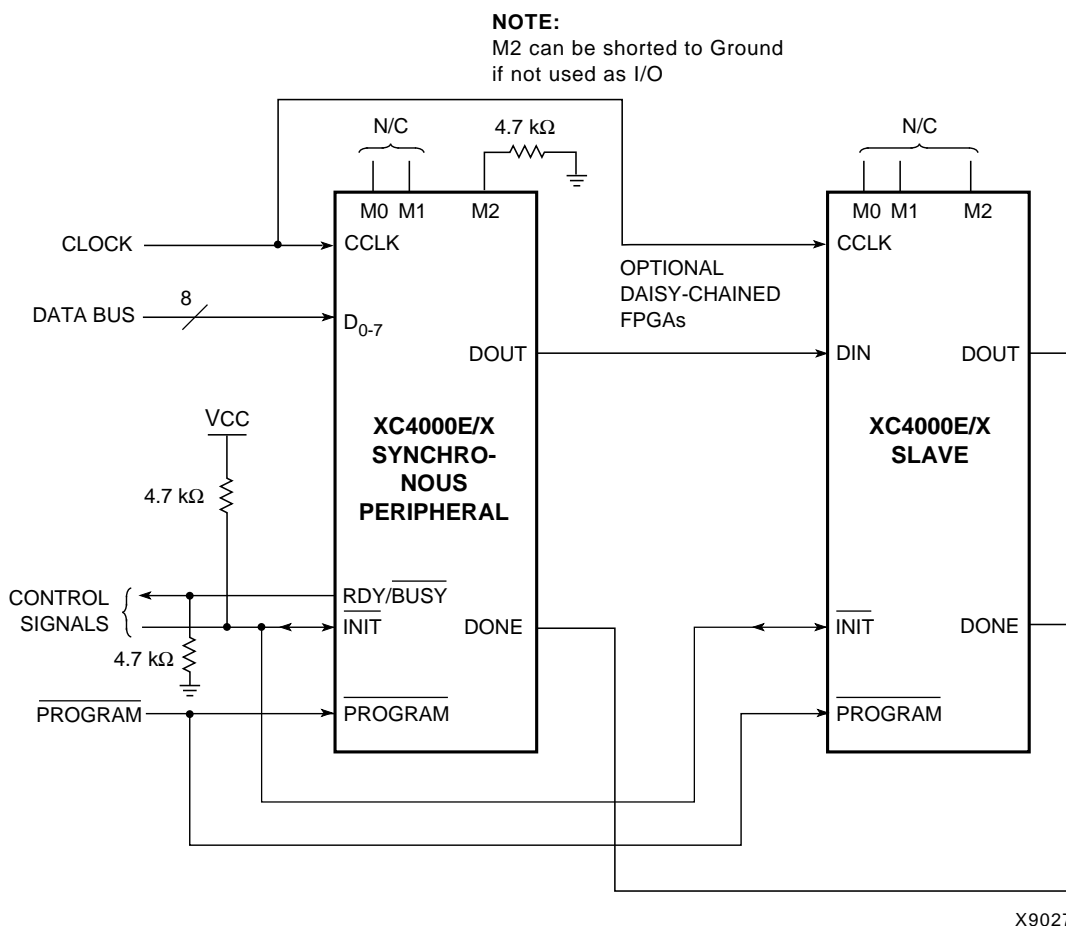
Synchronous Peripheral mode can also be considered Slave Parallel mode. An external signal drives the CCLK input(s) of the FPGA(s). The first byte of parallel configuration data must be available at the Data inputs of the lead FPGA a short setup time before the rising CCLK edge. Subsequent data bytes are clocked in on every eighth consecutive rising CCLK edge.

The same CCLK edge that accepts data, also causes the RDY/ $\overline{\text{BUSY}}$  output to go High for one CCLK period. The pin name is a misnomer. In Synchronous Peripheral mode it is really an ACKNOWLEDGE signal. Synchronous operation does not require this response, but it is a meaningful signal for test purposes. Note that RDY/ $\overline{\text{BUSY}}$  is pulled High with a high-impedance pullup prior to  $\overline{\text{INIT}}$  going High.

The lead FPGA serializes the data and presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

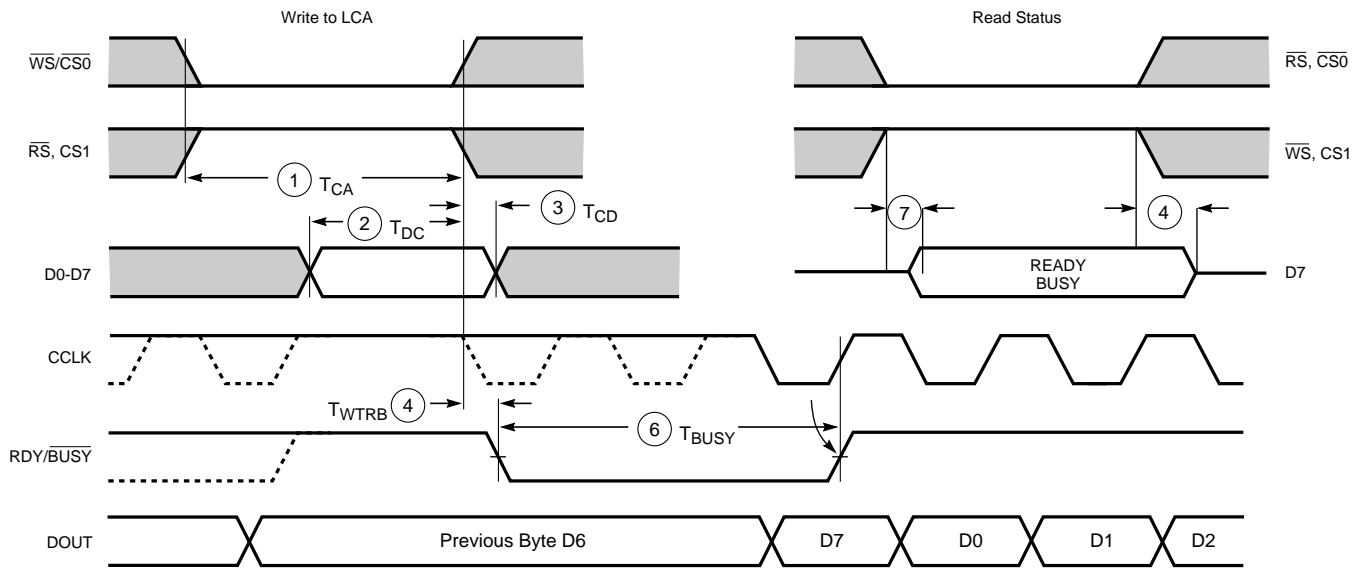
In order to complete the serial shift operation, 10 additional CCLK rising edges are required after the last data byte has been loaded, plus one more CCLK cycle for each daisy-chained device.

Synchronous Peripheral mode is selected by a <011> on the mode pins (M2, M1, M0).



X9027

**Figure 56: Synchronous Peripheral Mode Circuit Diagram**



X6097

|       | Description                                      | Symbol       | Min | Max | Units        |
|-------|--------------------------------------------------|--------------|-----|-----|--------------|
| Write | Effective Write time (CS0, WS=Low; RS, CS1=High) | 1 $T_{CA}$   | 100 |     | ns           |
|       | DIN setup time                                   | 2 $T_{DC}$   | 60  |     | ns           |
|       | DIN hold time                                    | 3 $T_{CD}$   | 0   |     | ns           |
| RDY   | RDY/BUSY delay after end of Write or Read        | 4 $T_{WTRB}$ |     | 60  | ns           |
|       | RDY/BUSY active after beginning of Read          | 7            |     | 60  | ns           |
|       | RDY/BUSY Low output (Note 4)                     | 6 $T_{BUSY}$ | 2   | 9   | CCLK periods |

- Notes:
1. Configuration must be delayed until the  $\overline{INIT}$  pins of all daisy-chained FPGAs are High.
  2. The time from the end of  $\overline{WS}$  to CCLK cycle for the new byte of data depends on the completion of previous byte processing and the phase of the internal timing generator for CCLK.
  3. CCLK and DOUT timing is tested in slave mode.
  4.  $T_{BUSY}$  indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest  $T_{BUSY}$  occurs when a byte is loaded into an empty parallel-to-serial converter. The longest  $T_{BUSY}$  occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

This timing diagram shows very relaxed requirements. Data need not be held beyond the rising edge of  $\overline{WS}$ . RDY/BUSY will go active within 60 ns after the end of  $\overline{WS}$ . A new write may be asserted immediately after RDY/BUSY goes Low, but write may not be terminated until RDY/BUSY has been High for one CCLK period.

**Figure 59: Asynchronous Peripheral Mode Programming Switching Characteristics**

## Product Availability

Table 24, Table 25, and Table 26 show the planned packages and speed grades for XC4000-Series devices. Call your local sales office for the latest availability information, or see the Xilinx website at <http://www.xilinx.com> for the latest revision of the specifications.

**Table 24: Component Availability Chart for XC4000XL FPGAs**

|          | PINS | TYPE | CODE | 84          | 100         | 100         | 144         | 144             | 160            | 160         | 176         | 176             | 208            | 208         | 240            | 240         | 256        | 299        | 304            | 352        | 411        | 432        | 475        | 559        | 560        |
|----------|------|------|------|-------------|-------------|-------------|-------------|-----------------|----------------|-------------|-------------|-----------------|----------------|-------------|----------------|-------------|------------|------------|----------------|------------|------------|------------|------------|------------|------------|
|          |      |      |      | Plast. PLOC | Plast. PQFP | Plast. VQFP | Plast. TQFP | High-Perf. TQFP | High-Perf. QFP | Plast. PQFP | Plast. TQFP | High-Perf. TQFP | High-Perf. QFP | Plast. PQFP | High-Perf. QFP | Plast. PQFP | Plast. BGA | Ceram. PGA | High-Perf. QFP | Plast. BGA | Ceram. PGA | Plast. BGA | Ceram. PGA | Ceram. PGA | Plast. BGA |
|          |      |      |      | PC84        | PQ100       | VQ100       | TQ144       | HT144           | HQ160          | PQ160       | TQ176       | HT176           | HQ208          | PQ208       | HQ240          | PQ240       | BG256      | PG299      | HQ304          | BG352      | PG411      | BG432      | PG475      | PG559      | BG560      |
| XC4002XL | -3   | C I  | C I  | C I         |             |             |             |                 |                |             |             |                 |                |             |                |             |            |            |                |            |            |            |            |            |            |
|          | -2   | C I  | C I  | C I         |             |             |             |                 |                |             |             |                 |                |             |                |             |            |            |                |            |            |            |            |            |            |
|          | -1   | C I  | C I  | C I         |             |             |             |                 |                |             |             |                 |                |             |                |             |            |            |                |            |            |            |            |            |            |
|          | -09C | C    | C    | C           |             |             |             |                 |                |             |             |                 |                |             |                |             |            |            |                |            |            |            |            |            |            |
| XC4005XL | -3   | C I  | C I  | C I         | C I         |             |             |                 |                | C I         |             |                 |                | C I         |                |             |            |            |                |            |            |            |            |            |            |
|          | -2   | C I  | C    | C I         | C I         |             |             |                 |                | C I         |             |                 |                | C I         |                |             |            |            |                |            |            |            |            |            |            |
|          | -1   | C I  | C I  | C I         | C I         |             |             |                 |                | C I         |             |                 |                | C I         |                |             |            |            |                |            |            |            |            |            |            |
|          | -09C | C    | C    | C           | C           |             |             |                 |                | C           |             |                 |                | C           |                |             |            |            |                |            |            |            |            |            |            |
| XC4010XL | -3   | C I  | C I  |             | C I         |             |             |                 |                | C I         | C I         |                 |                | C I         |                |             | C I        |            |                |            |            |            |            |            |            |
|          | -2   | C I  | C I  |             | C I         |             |             |                 |                | C I         | C I         |                 |                | C I         |                |             | C I        |            |                |            |            |            |            |            |            |
|          | -1   | C I  | C I  |             | C I         |             |             |                 |                | C I         | C I         |                 |                | C I         |                |             | C I        |            |                |            |            |            |            |            |            |
|          | -09C | C    | C    |             | C           |             |             |                 |                | C           | C           |                 |                | C           |                |             | C          |            |                |            |            |            |            |            |            |
| XC4013XL | -3   |      |      |             |             |             | C I         |                 |                | C I         |             | C I             |                | C I         |                | C I         | C I        |            |                |            |            |            |            |            |            |
|          | -2   |      |      |             |             |             | C I         |                 |                | C I         |             | C I             |                | C I         |                | C I         | C I        |            |                |            |            |            |            |            |            |
|          | -1   |      |      |             |             |             | C I         |                 |                | C I         |             | C I             |                | C I         |                | C I         | C I        |            |                |            |            |            |            |            |            |
|          | -09C |      |      |             |             |             | C           |                 |                | C           |             | C               |                | C           |                | C           | C          |            |                |            |            |            |            |            |            |
| XC4020XL | -3   |      |      |             |             |             | C I         |                 |                | C I         |             | C I             |                | C I         |                | C I         | C I        |            |                |            |            |            |            |            |            |
|          | -2   |      |      |             |             |             | C I         |                 |                | C I         |             | C I             |                | C I         |                | C I         | C I        |            |                |            |            |            |            |            |            |
|          | -1   |      |      |             |             |             | C I         |                 |                | C I         |             | C I             |                | C I         |                | C I         | C I        |            |                |            |            |            |            |            |            |
|          | -09C |      |      |             |             |             | C           |                 |                | C           |             | C               |                | C           |                | C           | C          |            |                |            |            |            |            |            |            |
| XC4028XL | -3   |      |      |             |             |             |             |                 | C I            |             |             |                 | C I            |             | C I            |             | C I        | C I        | C I            | C I        |            |            |            |            |            |
|          | -2   |      |      |             |             |             |             |                 | C I            |             |             |                 | C I            |             | C I            |             | C I        | C I        | C I            | C I        |            |            |            |            |            |
|          | -1   |      |      |             |             |             |             |                 | C I            |             |             |                 | C I            |             | C I            |             | C I        | C I        | C I            | C I        |            |            |            |            |            |
|          | -09C |      |      |             |             |             |             |                 | C              |             |             |                 | C              |             | C              |             | C          | C          | C              | C          |            |            |            |            |            |
| XC4036XL | -3   |      |      |             |             |             |             |                 | C I            |             |             |                 | C I            |             | C I            |             |            |            | C I            | C I        | C I        | C I        |            |            |            |
|          | -2   |      |      |             |             |             |             |                 | C I            |             |             |                 | C I            |             | C              |             |            |            | C I            | C I        | C I        | C I        |            |            |            |
|          | -1   |      |      |             |             |             |             |                 | C I            |             |             |                 | C I            |             | C I            |             |            |            | C I            | C I        | C I        | C I        |            |            |            |
|          | -09C |      |      |             |             |             |             |                 | C              |             |             |                 | C              |             | C              |             |            |            | C              | C          | C          | C          |            |            |            |
| XC4044XL | -3   |      |      |             |             |             |             |                 | C I            |             |             |                 | C I            |             | C I            |             |            |            | C I            | C I        | C I        | C I        |            |            |            |
|          | -2   |      |      |             |             |             |             |                 | C I            |             |             |                 | C I            |             | C I            |             |            |            | C I            | C I        | C I        | C I        |            |            |            |
|          | -1   |      |      |             |             |             |             |                 | C I            |             |             |                 | C I            |             | C I            |             |            |            | C I            | C I        | C I        | C I        |            |            |            |
|          | -09C |      |      |             |             |             |             |                 | C              |             |             |                 | C              |             | C              |             |            |            | C              | C          | C          | C          |            |            |            |
| XC4052XL | -3   |      |      |             |             |             |             |                 |                |             |             |                 |                |             | C I            |             |            |            | C I            |            | C I        | C I        |            |            | C I        |
|          | -2   |      |      |             |             |             |             |                 |                |             |             |                 |                |             | C I            |             |            |            | C I            |            | C I        | C I        |            |            | C I        |
|          | -1   |      |      |             |             |             |             |                 |                |             |             |                 |                |             | C I            |             |            |            | C I            |            | C I        | C I        |            |            | C I        |
|          | -09C |      |      |             |             |             |             |                 |                |             |             |                 |                |             | C              |             |            |            | C              |            | C          | C          |            |            | C          |
| XC4062XL | -3   |      |      |             |             |             |             |                 |                |             |             |                 |                |             | C I            |             |            |            | C I            |            |            | C I        | C I        |            | C I        |
|          | -2   |      |      |             |             |             |             |                 |                |             |             |                 |                |             | C I            |             |            |            | C I            |            |            | C I        | C I        |            | C I        |
|          | -1   |      |      |             |             |             |             |                 |                |             |             |                 |                |             | C I            |             |            |            | C I            |            |            | C I        | C I        |            | C I        |
|          | -09C |      |      |             |             |             |             |                 |                |             |             |                 |                |             | C              |             |            |            | C              |            |            | C          | C          |            | C          |
| XC4085XL | -3   |      |      |             |             |             |             |                 |                |             |             |                 |                |             |                |             |            |            |                |            |            | C I        |            | C I        | C I        |
|          | -2   |      |      |             |             |             |             |                 |                |             |             |                 |                |             |                |             |            |            |                |            |            | C I        |            | C I        | C I        |
|          | -1   |      |      |             |             |             |             |                 |                |             |             |                 |                |             |                |             |            |            |                |            |            | C I        |            | C I        | C I        |
|          | -09C |      |      |             |             |             |             |                 |                |             |             |                 |                |             |                |             |            |            |                |            |            | C          |            | C          | C          |

1/29/99

C = Commercial  $T_J = 0^\circ$  to  $+85^\circ\text{C}$

I = Industrial  $T_J = -40^\circ\text{C}$  to  $+100^\circ\text{C}$

**Table 25: Component Availability Chart for XC4000E FPGAs**

|         | PINS | TYPE | CODE | 84          | 100         | 100         | 120        | 144         | 156        | 160         | 191        | 208            | 208         | 223        | 225        | 240            | 240         | 299        | 304           |
|---------|------|------|------|-------------|-------------|-------------|------------|-------------|------------|-------------|------------|----------------|-------------|------------|------------|----------------|-------------|------------|---------------|
|         |      |      |      | Plast. PLCC | Plast. PQFP | Plast. VQFP | Ceram. PGA | Plast. TQFP | Ceram. PGA | Plast. PQFP | Ceram. PGA | High-Perf. QFP | Plast. PQFP | Ceram. PGA | Plast. BGA | High-Perf. QFP | Plast. PQFP | Ceram. PGA | High-Perf. QF |
|         |      |      |      | PC84        | PQ100       | VQ100       | PG120      | TQ144       | PG156      | PQ160       | PG191      | HQ208          | PQ208       | PG223      | BG225      | HQ240          | PQ240       | PG299      | HQ304         |
| XC4003E | -4   | C I  | C I  | C I         | C I         |             |            |             |            |             |            |                |             |            |            |                |             |            |               |
|         | -3   | C I  | C I  | C I         | C I         |             |            |             |            |             |            |                |             |            |            |                |             |            |               |
|         | -2   | C I  | C I  | C I         | C I         |             |            |             |            |             |            |                |             |            |            |                |             |            |               |
|         | -1   | C    | C    | C           | C           |             |            |             |            |             |            |                |             |            |            |                |             |            |               |
| XC4005E | -4   | C I  | C I  |             |             |             |            | C I         | C I        | C I         |            |                | C I         |            |            |                |             |            |               |
|         | -3   | C I  | C I  |             |             |             |            | C I         | C I        | C I         |            |                | C I         |            |            |                |             |            |               |
|         | -2   | C I  | C I  |             |             |             |            | C I         | C I        | C I         |            |                | C I         |            |            |                |             |            |               |
|         | -1   | C    | C    |             |             |             |            | C           | C          | C           |            |                | C           |            |            |                |             |            |               |
| XC4006E | -4   | C I  |      |             |             |             |            | C I         | C I        | C I         |            |                | C I         |            |            |                |             |            |               |
|         | -3   | C I  |      |             |             |             |            | C I         | C I        | C I         |            |                | C I         |            |            |                |             |            |               |
|         | -2   | C I  |      |             |             |             |            | C I         | C I        | C I         |            |                | C I         |            |            |                |             |            |               |
|         | -1   | C    |      |             |             |             |            | C           | C          | C           |            |                | C           |            |            |                |             |            |               |
| XC4008E | -4   | C I  |      |             |             |             |            |             |            | C I         | C I        |                | C I         |            |            |                |             |            |               |
|         | -3   | C I  |      |             |             |             |            |             |            | C I         | C I        |                | C I         |            |            |                |             |            |               |
|         | -2   | C I  |      |             |             |             |            |             |            | C I         | C I        |                | C I         |            |            |                |             |            |               |
|         | -1   | C    |      |             |             |             |            |             |            | C           | C          |                | C           |            |            |                |             |            |               |
| XC4010E | -4   | C I  |      |             |             |             |            |             |            | C I         | C I        | C I            | C I         |            |            | C I            |             |            |               |
|         | -3   | C I  |      |             |             |             |            |             |            | C I         | C I        | C I            | C I         |            |            | C I            |             |            |               |
|         | -2   | C I  |      |             |             |             |            |             |            | C I         | C I        | C I            | C I         |            |            | C I            |             |            |               |
|         | -1   | C    |      |             |             |             |            |             |            | C           | C          | C              | C           |            |            | C              |             |            |               |
| XC4013E | -4   |      |      |             |             |             |            |             |            | C I         |            | C I            | C I         | C I        | C I        | C I            | C I         |            |               |
|         | -3   |      |      |             |             |             |            |             |            | C I         |            | C I            | C I         | C I        | C I        | C I            | C I         |            |               |
|         | -2   |      |      |             |             |             |            |             |            | C I         |            | C I            | C I         | C I        | C I        | C I            | C I         |            |               |
|         | -1   |      |      |             |             |             |            |             |            | C           |            | C              | C           | C          | C          | C              | C           |            |               |
| XC4020E | -4   |      |      |             |             |             |            |             |            |             |            | C I            |             | C I        |            | C I            |             |            |               |
|         | -3   |      |      |             |             |             |            |             |            |             |            | C I            |             | C I        |            | C I            |             |            |               |
|         | -2   |      |      |             |             |             |            |             |            |             |            | C I            |             | C I        |            | C I            |             |            |               |
|         | -1   |      |      |             |             |             |            |             |            |             |            | C              |             | C          |            | C              |             |            |               |
| XC4025E | -4   |      |      |             |             |             |            |             |            |             |            |                |             | C I        |            | C I            |             | C I        | C I           |
|         | -3   |      |      |             |             |             |            |             |            |             |            |                |             | C I        |            | C I            |             | C I        | C I           |
|         | -2   |      |      |             |             |             |            |             |            |             |            |                |             | C          |            | C              |             | C          | C             |

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C = Commercial  $T_J = 0^\circ$  to  $+85^\circ\text{C}$

I = Industrial  $T_J = -40^\circ\text{C}$  to  $+100^\circ\text{C}$

**Table 26: Component Availability Chart for XC4000EX FPGAs**

|          | PINS | TYPE | CODE | 208            | 240            | 299        | 304            | 352        | 411        | 432        |
|----------|------|------|------|----------------|----------------|------------|----------------|------------|------------|------------|
|          |      |      |      | High-Perf. QFP | High-Perf. QFP | Ceram. PGA | High-Perf. QFP | Plast. BGA | Ceram. PGA | Plast. BGA |
|          |      |      |      | HQ208          | HQ240          | PG299      | HQ304          | BG352      | PG411      | BG432      |
| XC4028EX | -4   | C I  |      | C I            | C I            | C I        | C I            | C I        |            |            |
|          | -3   | C I  |      | C I            | C I            | C I        | C I            | C I        |            |            |
|          | -2   | C    |      | C              | C              | C          | C              | C          |            |            |
| XC4036EX | -4   |      |      |                | C I            |            | C I            | C I        | C I        | C I        |
|          | -3   |      |      |                | C I            |            | C I            | C I        | C I        | C I        |
|          | -2   |      |      |                | C              |            | C              | C          | C          | C          |

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C = Commercial  $T_J = 0^\circ$  to  $+85^\circ\text{C}$

I = Industrial  $T_J = -40^\circ\text{C}$  to  $+100^\circ\text{C}$

## User I/O Per Package

Table 27, Table 28, and Table 29 show the number of user I/Os available in each package for XC4000-Series devices. Call your local sales office for the latest availability information, or see the Xilinx website at <http://www.xilinx.com> for the latest revision of the specifications.

**Table 27: User I/O Chart for XC4000XL FPGAs**

| Device   | Max I/O | Maximum User Accessible I/O by Package Type |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
|----------|---------|---------------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
|          |         | PC84                                        | PQ100 | VQ100 | TQ144 | HT144 | HQ160 | PQ160 | TQ176 | HT176 | HQ208 | PQ208 | HQ240 | PQ240 | BG256 | PG299 | HQ304 | BG352 | PG411 | BG432 | PG475 | PG559 | BG560 |
| XC4002XL | 64      | 61                                          | 64    | 64    |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
| XC4005XL | 112     | 61                                          | 77    | 77    | 112   |       |       | 112   |       |       | 112   |       |       |       |       |       |       |       |       |       |       |       |       |
| XC4010XL | 160     | 61                                          | 77    |       | 113   |       |       | 129   | 145   |       | 160   |       |       | 160   |       |       |       |       |       |       |       |       |       |
| XC4013XL | 192     |                                             |       |       |       | 113   |       | 129   |       | 145   |       | 160   |       | 192   | 192   |       |       |       |       |       |       |       |       |
| XC4020XL | 224     |                                             |       |       |       | 113   |       | 129   |       | 145   |       | 160   |       | 192   | 205   |       |       |       |       |       |       |       |       |
| XC4028XL | 256     |                                             |       |       |       |       | 129   |       |       |       | 160   |       | 193   |       | 205   | 256   | 256   | 256   |       |       |       |       |       |
| XC4036XL | 288     |                                             |       |       |       |       | 129   |       |       |       | 160   |       | 193   |       |       |       | 256   | 288   | 288   | 288   |       |       |       |
| XC4044XL | 320     |                                             |       |       |       |       | 129   |       |       |       | 160   |       | 193   |       |       |       | 256   | 289   | 320   | 320   |       |       |       |
| XC4052XL | 352     |                                             |       |       |       |       |       |       |       |       |       | 193   |       |       |       |       | 256   |       | 352   | 352   |       |       | 352   |
| XC4062XL | 384     |                                             |       |       |       |       |       |       |       |       |       | 193   |       |       |       |       | 256   |       |       | 352   | 384   |       | 384   |
| XC4085XL | 448     |                                             |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       | 352   |       | 448   | 448   |

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**Table 28: User I/O Chart for XC4000E FPGAs**

| Device  | Max I/O | Maximum User Accessible I/O by Package Type |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
|---------|---------|---------------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
|         |         | PC84                                        | PQ100 | VQ100 | PG120 | TQ144 | PG156 | PQ160 | PG191 | HQ208 | PQ208 | PG223 | BG225 | HQ240 | PQ240 | PG299 | HQ304 |
| XC4003E | 80      | 61                                          | 77    | 77    | 80    |       |       |       |       |       |       |       |       |       |       |       |       |
| XC4005E | 112     | 61                                          | 77    |       |       | 112   | 112   | 112   |       |       | 112   |       |       |       |       |       |       |
| XC4006E | 128     | 61                                          |       |       |       | 113   | 125   | 128   |       |       | 128   |       |       |       |       |       |       |
| XC4008E | 144     | 61                                          |       |       |       |       |       | 129   | 144   |       | 144   |       |       |       |       |       |       |
| XC4010E | 160     | 61                                          |       |       |       |       |       | 129   | 160   | 160   | 160   |       | 160   |       |       |       |       |
| XC4013E | 192     |                                             |       |       |       |       |       | 129   |       | 160   | 160   | 192   | 192   | 192   | 192   |       |       |
| XC4020E | 224     |                                             |       |       |       |       |       |       |       | 160   |       | 192   |       | 193   |       |       |       |
| XC4025E | 256     |                                             |       |       |       |       |       |       |       |       |       | 192   |       | 193   |       | 256   | 256   |

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**Table 29: User I/O Chart for XC4000EX FPGAs**

| Device   | Max I/O | Maximum User Accessible I/O by Package Type |       |       |       |       |       |       |
|----------|---------|---------------------------------------------|-------|-------|-------|-------|-------|-------|
|          |         | HQ208                                       | HQ240 | PG299 | HQ304 | BG352 | PG411 | BG432 |
| XC4028EX | 256     | 160                                         | 193   | 256   | 256   | 256   |       |       |
| XC4036EX | 288     |                                             | 193   |       | 256   | 288   | 288   | 288   |

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