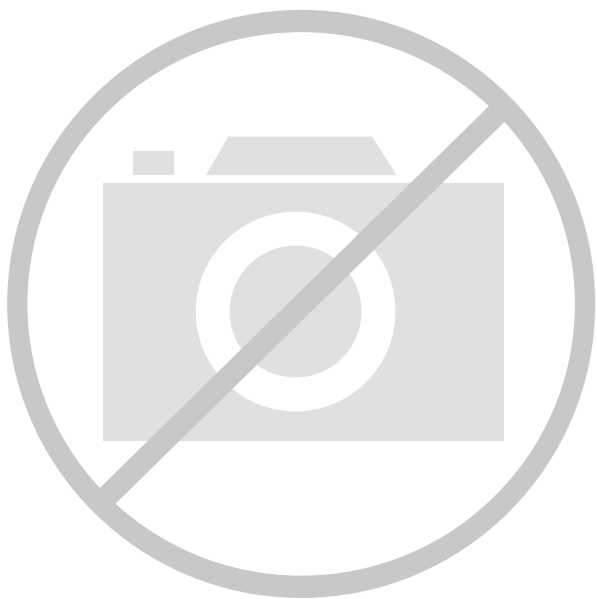




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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

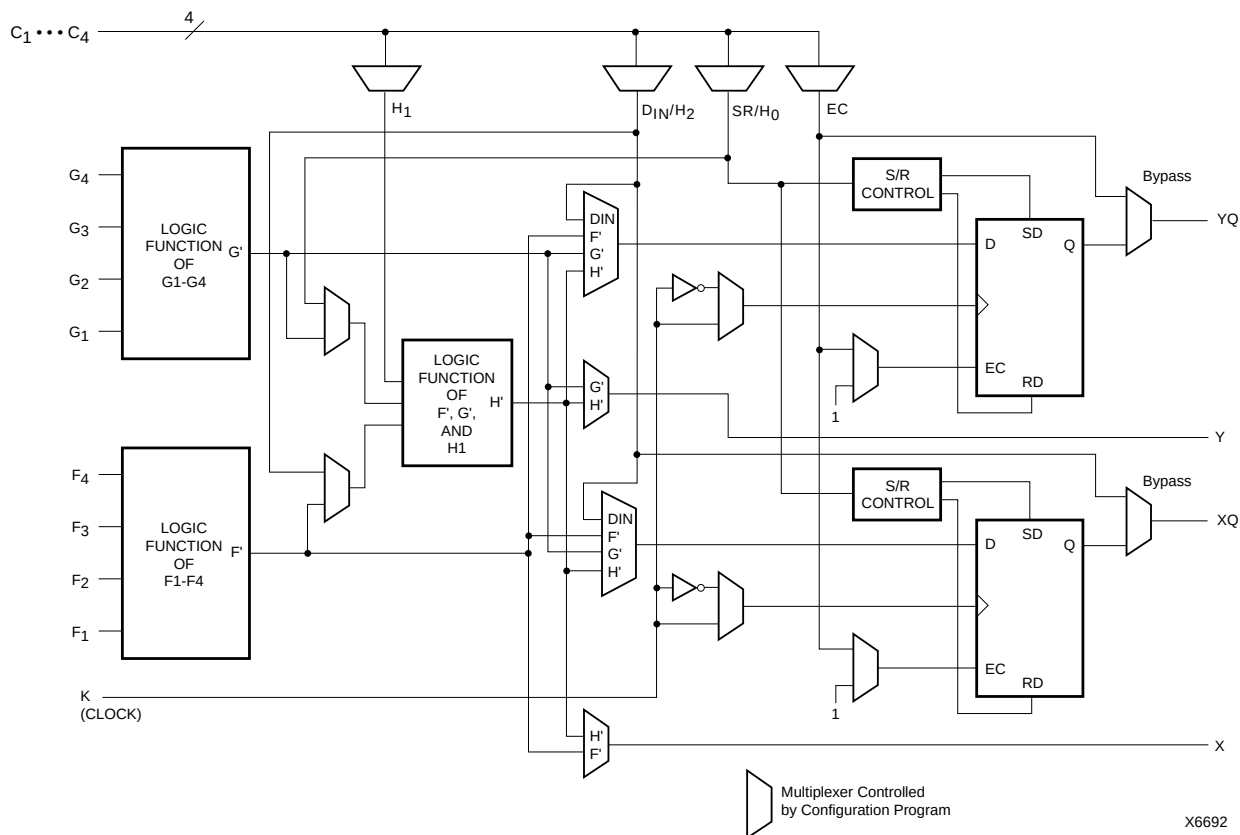
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                       |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                              |
| Number of LABs/CLBs            | 256                                                                                                                                   |
| Number of Logic Elements/Cells | 608                                                                                                                                   |
| Total RAM Bits                 | 8192                                                                                                                                  |
| Number of I/O                  | 128                                                                                                                                   |
| Number of Gates                | 6000                                                                                                                                  |
| Voltage - Supply               | 4.75V ~ 5.25V                                                                                                                         |
| Mounting Type                  | Surface Mount                                                                                                                         |
| Operating Temperature          | 0°C ~ 85°C (TJ)                                                                                                                       |
| Package / Case                 | 160-BQFP                                                                                                                              |
| Supplier Device Package        | 160-PQFP (28x28)                                                                                                                      |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/xilinx/xc4006e-1pq160c">https://www.e-xfl.com/product-detail/xilinx/xc4006e-1pq160c</a> |



**Figure 1: Simplified Block Diagram of XC4000 Series CLB (RAM and Carry Logic functions not shown)**

### Flip-Flops

The CLB can pass the combinational output(s) to the interconnect network, but can also store the combinational results or other incoming data in one or two flip-flops, and connect their outputs to the interconnect network as well.

The two edge-triggered D-type flip-flops have common clock (K) and clock enable (EC) inputs. Either or both clock inputs can also be permanently enabled. Storage element functionality is described in [Table 2](#).

### Latches (XC4000X only)

The CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Storage element functionality is described in [Table 2](#).

### Clock Input

Each flip-flop can be triggered on either the rising or falling clock edge. The clock pin is shared by both storage elements. However, the clock is individually invertible for each storage element. Any inverter placed on the clock input is automatically absorbed into the CLB.

### Clock Enable

The clock enable signal (EC) is active High. The EC pin is shared by both storage elements. If left unconnected for either, the clock enable for that storage element defaults to the active state. EC is not invertible within the CLB.

**Table 2: CLB Storage Element Functionality (active rising edge is shown)**

| Mode            | K                      | EC | SR | D | Q  |
|-----------------|------------------------|----|----|---|----|
| Power-Up or GSR | X                      | X  | X  | X | SR |
| Flip-Flop       | X                      | X  | 1  | X | SR |
|                 | $\overline{\text{SR}}$ | 1* | 0* | D | D  |
| Latch           | 0                      | X  | 0* | X | Q  |
|                 | 1                      | 1* | 0* | X | Q  |
| Both            | 0                      | 1* | 0* | D | D  |
|                 | X                      | 0  | 0* | X | Q  |

Legend:

X

$\overline{\text{SR}}$

0\*

1\*

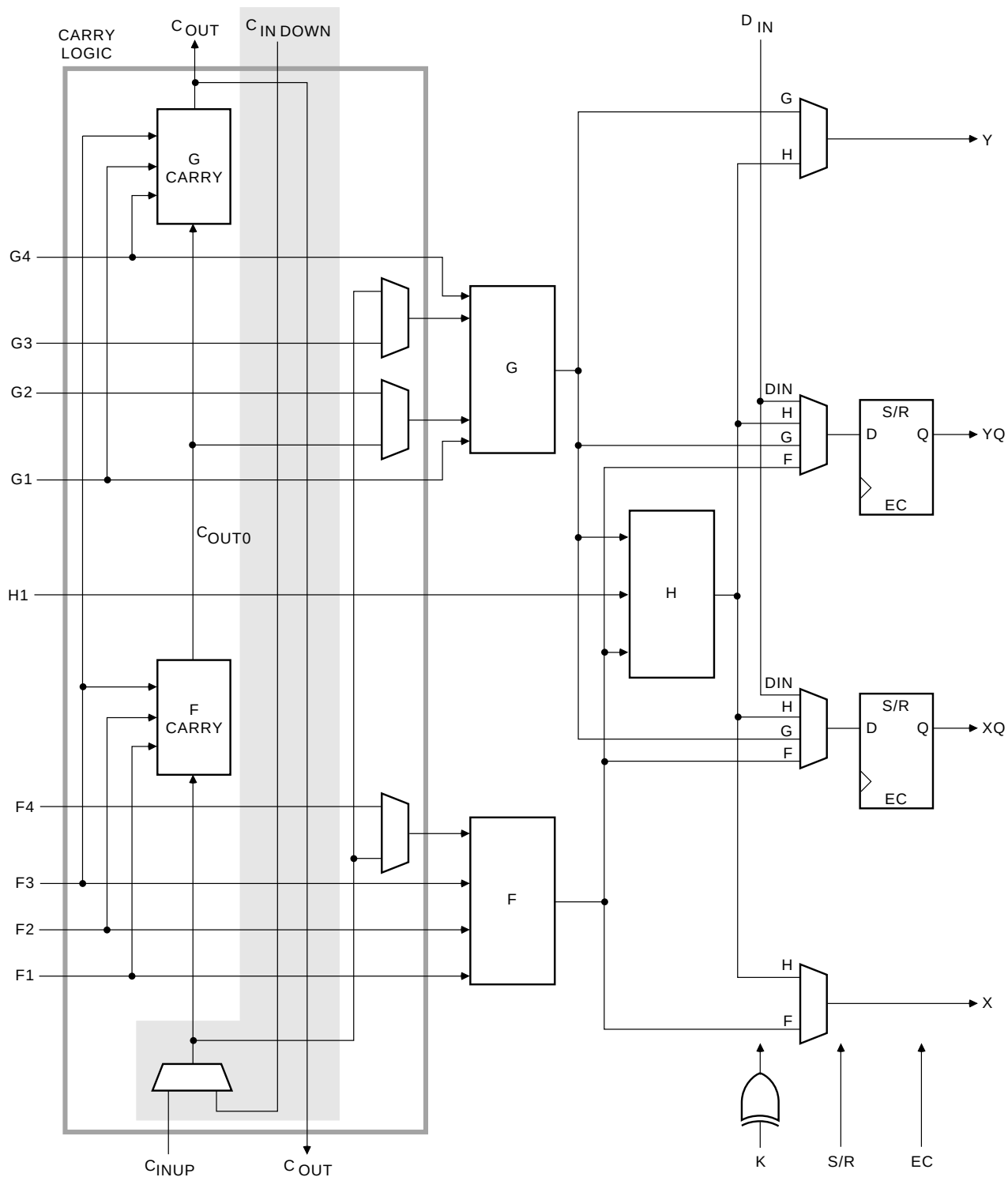
Don't care

Rising edge

Set or Reset value. Reset is default.

Input is Low or unconnected (default value)

Input is High or unconnected (default value)



X6699

**Figure 13: Fast Carry Logic in XC4000E CLB (shaded area not present in XC4000X)**

### Additional Input Latch for Fast Capture (XC4000X only)

The XC4000X IOB has an additional optional latch on the input. This latch, as shown in [Figure 16](#), is clocked by the output clock — the clock used for the output flip-flop — rather than the input clock. Therefore, two different clocks can be used to clock the two input storage elements. This additional latch allows the very fast capture of input data, which is then synchronized to the internal clock by the IOB flip-flop or latch.

To use this Fast Capture technique, drive the output clock pin (the Fast Capture latching signal) from the output of one of the Global Early buffers supplied in the XC4000X. The second storage element should be clocked by a Global Low-Skew buffer, to synchronize the incoming data to the internal logic. (See [Figure 17](#).) These special buffers are described in “Global Nets and Buffers (XC4000X only)” on [page 37](#).

The Fast Capture latch (FCL) is designed primarily for use with a Global Early buffer. For Fast Capture, a single clock signal is routed through both a Global Early buffer and a Global Low-Skew buffer. (The two buffers share an input pad.) The Fast Capture latch is clocked by the Global Early buffer, and the standard IOB flip-flop or latch is clocked by the Global Low-Skew buffer. This mode is the safest way to use the Fast Capture latch, because the clock buffers on both storage elements are driven by the same pad. There is no external skew between clock pads to create potential problems.

To place the Fast Capture latch in a design, use one of the special library symbols, ILFFX or ILFLX. ILFFX is a transparent-Low Fast Capture latch followed by an active-High input flip-flop. ILFLX is a transparent-Low Fast Capture latch followed by a transparent-High input latch. Any of the clock inputs can be inverted before driving the library element, and the inverter is absorbed into the IOB. If a single BUFG output is used to drive both clock inputs, the software automatically runs the clock through both a Global Low-Skew buffer and a Global Early buffer, and clocks the Fast Capture latch appropriately.

[Figure 16 on page 21](#) also shows a two-tap delay on the input. By default, if the Fast Capture latch is used, the Xilinx software assumes a Global Early buffer is driving the clock, and selects MEDDELAY to ensure a zero hold time. Select

the desired delay based on the discussion in the previous subsection.

### IOB Output Signals

Output signals can be optionally inverted within the IOB, and can pass directly to the pad or be stored in an edge-triggered flip-flop. The functionality of this flip-flop is shown in [Table 11](#).

An active-High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (OUT) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB.

The 4-mA maximum output current specification of many FPGAs often forces the user to add external buffers, which are especially cumbersome on bidirectional I/O lines. The XC4000E and XC4000EX/XL devices solve many of these problems by providing a guaranteed output sink current of 12 mA. Two adjacent outputs can be interconnected externally to sink up to 24 mA. The XC4000E and XC4000EX/XL FPGAs can thus directly drive buses on a printed circuit board.

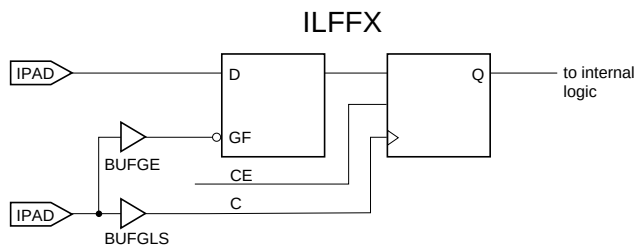
By default, the output pull-up structure is configured as a TTL-like totem-pole. The High driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below Vcc. Alternatively, the outputs can be globally configured as CMOS drivers, with p-channel pull-up transistors pulling to Vcc. This option, applied using the bitstream generation software, applies to all outputs on the device. It is not individually programmable. In the XC4000XL, all outputs are pulled to the positive supply rail.

**Table 11: Output Flip-Flop Functionality (active rising edge is shown)**

| Mode            | Clock                                                                               | Clock Enable | T  | D | Q  |
|-----------------|-------------------------------------------------------------------------------------|--------------|----|---|----|
| Power-Up or GSR | X                                                                                   | X            | 0* | X | SR |
| Flip-Flop       | X                                                                                   | 0            | 0* | X | Q  |
|                 |  | 1*           | 0* | D | D  |
|                 | X                                                                                   | X            | 1  | X | Z  |
|                 | 0                                                                                   | X            | 0* | X | Q  |

Legend:

X Don't care  
 Rising edge  
 SR Set or Reset value. Reset is default.  
 0\* Input is Low or unconnected (default value)  
 1\* Input is High or unconnected (default value)  
 Z 3-state



X9013

**Figure 17: Examples Using XC4000X FCL**

or clear on reset and after configuration. Other than the global GSR net, no user-controlled set/reset signal is available to the I/O flip-flops. The choice of set or clear applies to both the initial state of the flip-flop and the response to the Global Set/Reset pulse. See [“Global Set/Reset” on page 11](#) for a description of how to use GSR.

### JTAG Support

Embedded logic attached to the IOBs contains test structures compatible with IEEE Standard 1149.1 for boundary scan testing, permitting easy chip and board-level testing. More information is provided in [“Boundary Scan” on page 42](#).

### Three-State Buffers

A pair of 3-state buffers is associated with each CLB in the array. (See [Figure 27 on page 30](#).) These 3-state buffers can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal longlines, saving logic resources. Programmable pull-up resistors attached to these longlines help to implement a wide wired-AND function.

The buffer enable is an active-High 3-state (i.e. an active-Low enable), as shown in [Table 13](#).

Another 3-state buffer with similar access is located near each I/O block along the right and left edges of the array. (See [Figure 33 on page 34](#).)

The horizontal longlines driven by the 3-state buffers have a weak keeper at each end. This circuit prevents undefined floating levels. However, it is overridden by any driver, even a pull-up resistor.

Special longlines running along the perimeter of the array can be used to wire-AND signals coming from nearby IOBs or from internal longlines. These longlines form the wide edge decoders discussed in [“Wide Edge Decoders” on page 27](#).

### Three-State Buffer Modes

The 3-state buffers can be configured in three modes:

- Standard 3-state buffer
- Wired-AND with input on the I pin
- Wired OR-AND

### Standard 3-State Buffer

All three pins are used. Place the library element BUFT. Connect the input to the I pin and the output to the O pin. The T pin is an active-High 3-state (i.e. an active-Low enable). Tie the T pin to Ground to implement a standard buffer.

### Wired-AND with Input on the I Pin

The buffer can be used as a Wired-AND. Use the WAND1 library symbol, which is essentially an open-drain buffer. WAND4, WAND8, and WAND16 are also available. See the *XACT Libraries Guide* for further information.

The T pin is internally tied to the I pin. Connect the input to the I pin and the output to the O pin. Connect the outputs of all the WAND1s together and attach a PULLUP symbol.

### Wired OR-AND

The buffer can be configured as a Wired OR-AND. A High level on either input turns off the output. Use the WOR2AND library symbol, which is essentially an open-drain 2-input OR gate. The two input pins are functionally equivalent. Attach the two inputs to the I0 and I1 pins and tie the output to the O pin. Tie the outputs of all the WOR2ANDs together and attach a PULLUP symbol.

### Three-State Buffer Examples

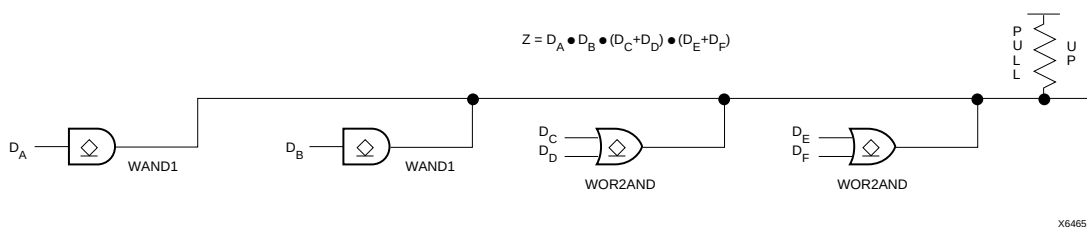
[Figure 21](#) shows how to use the 3-state buffers to implement a wired-AND function. When all the buffer inputs are High, the pull-up resistor(s) provide the High output.

[Figure 22](#) shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active-High 3-state (T) is identical to an active-Low output enable, as shown in [Table 13](#).

**Table 13: Three-State Buffer Functionality**

| IN | T | OUT |
|----|---|-----|
| X  | 1 | Z   |
| IN | 0 | IN  |



**Figure 21: Open-Drain Buffers Implement a Wired-AND Function**

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8 MHz clock, plus any two of 500 kHz, 16kHz, 490Hz and 15Hz (up to 10% lower for low-voltage devices). These frequencies can vary by as much as -50% or +25%.

These signals can be accessed by placing the OSC4 library element in a schematic or in HDL code (see [Figure 24](#)).

The oscillator is automatically disabled after configuration if the OSC4 symbol is not used in the design.

## Programmable Interconnect

All internal connections are composed of metal segments with programmable switching points and switching matrices to implement the desired routing. A structured, hierarchical matrix of routing resources is provided to achieve efficient automated routing.

The XC4000E and XC4000X share a basic interconnect structure. XC4000X devices, however, have additional routing not available in the XC4000E. The extra routing resources allow high utilization in high-capacity devices. All XC4000X-specific routing resources are clearly identified throughout this section. Any resources not identified as XC4000X-specific are present in all XC4000 Series devices.

This section describes the varied routing resources available in XC4000 Series devices. The implementation software automatically assigns the appropriate resources based on the density and timing requirements of the design.

## Interconnect Overview

There are several types of interconnect.

- CLB routing is associated with each row and column of the CLB array.
- IOB routing forms a ring (called a VersaRing) around the outside of the CLB array. It connects the I/O with the internal logic blocks.

- Global routing consists of dedicated networks primarily designed to distribute clocks throughout the device with minimum delay and skew. Global routing can also be used for other high-fanout signals.

Five interconnect types are distinguished by the relative length of their segments: single-length lines, double-length lines, quad and octal lines (XC4000X only), and longlines. In the XC4000X, direct connects allow fast data flow between adjacent CLBs, and between IOBs and CLBs.

Extra routing is included in the IOB pad ring. The XC4000X also includes a ring of octal interconnect lines near the IOBs to improve pin-swapping and routing to locked pins.

XC4000E/X devices include two types of global buffers. These global buffers have different properties, and are intended for different purposes. They are discussed in detail later in this section.

## CLB Routing Connections

A high-level diagram of the routing resources associated with one CLB is shown in [Figure 25](#). The shaded arrows represent routing present only in XC4000X devices.

[Table 14](#) shows how much routing of each type is available in XC4000E and XC4000X CLB arrays. Clearly, very large designs, or designs with a great deal of interconnect, will route more easily in the XC4000X. Smaller XC4000E designs, typically requiring significantly less interconnect, do not require the additional routing.

[Figure 27 on page 30](#) is a detailed diagram of both the XC4000E and the XC4000X CLB, with associated routing. The shaded square is the programmable switch matrix, present in both the XC4000E and the XC4000X. The L-shaped shaded area is present only in XC4000X devices. As shown in the figure, the XC4000X block is essentially an XC4000E block with additional routing.

CLB inputs and outputs are distributed on all four sides, providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation.

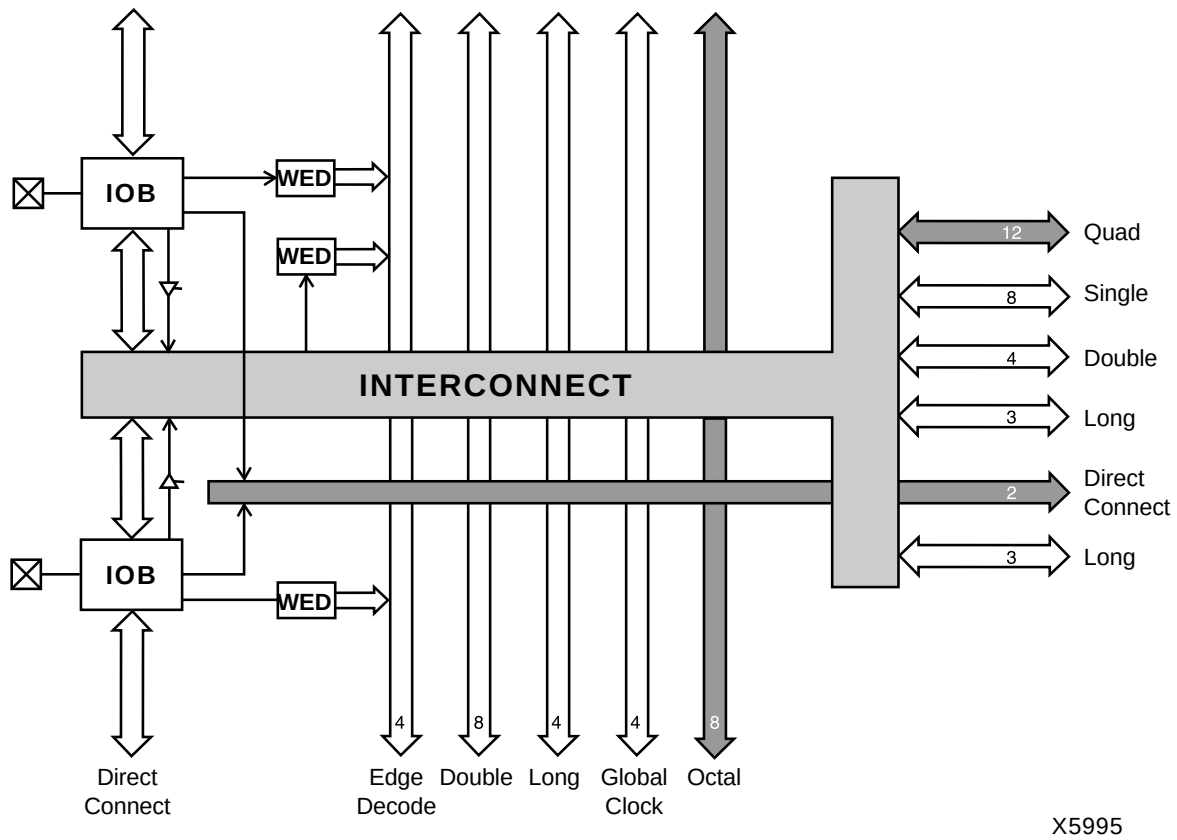


Figure 31: High-Level Routing Diagram of XC4000 Series VersaRing (Left Edge)  
WED = Wide Edge Decoder, IOB = I/O Block (shaded arrows indicate XC4000X only)

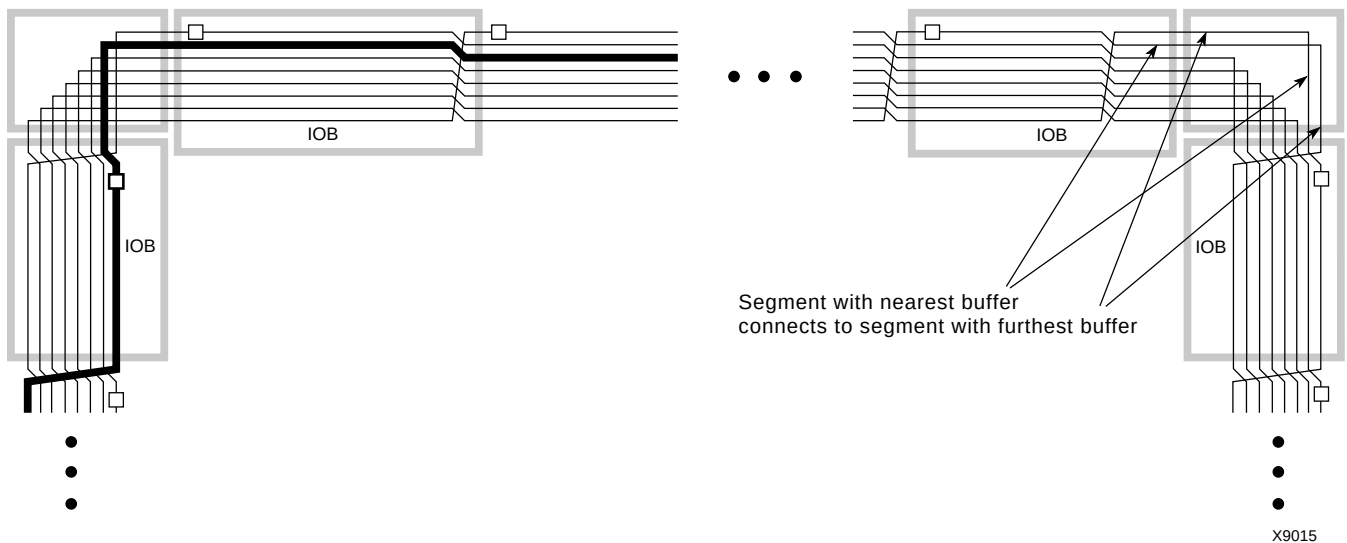


Figure 32: XC4000X Octal I/O Routing



IOB inputs and outputs interface with the octal lines via the single-length interconnect lines. Single-length lines are also used for communication between the octals and double-length lines, quads, and longlines within the CLB array.

Segmentation into buffered octals was found to be optimal for distributing signals over long distances around the device.

### Global Nets and Buffers

Both the XC4000E and the XC4000X have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew. The global buffers are described in detail in the following sections. The text descriptions and diagrams are summarized in [Table 15](#). The table shows which CLB and IOB clock pins can be sourced by which global buffers.

In both XC4000E and XC4000X devices, placement of a library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. The detailed information in these sections is included only for reference.

#### Global Nets and Buffers (XC4000E only)

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. The four global lines can be driven by either of two types of global buffers. The clock pins of every CLB and IOB can also be sourced from local interconnect.

Two different types of clock buffers are available in the XC4000E:

- Primary Global Buffers (BUFGP)
- Secondary Global Buffers (BUFGS)

Four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs.

The Primary Global buffers must be driven by the semi-dedicated pads. The Secondary Global buffers can be sourced by either semi-dedicated pads or internal nets.

Each CLB column has four dedicated vertical Global lines. Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in [Figure 34](#). Each corner of the device has one Primary buffer and one Secondary buffer.

IOBs along the left and right edges have four vertical global longlines. Top and bottom IOBs can be clocked from the global lines in the adjacent CLB column.

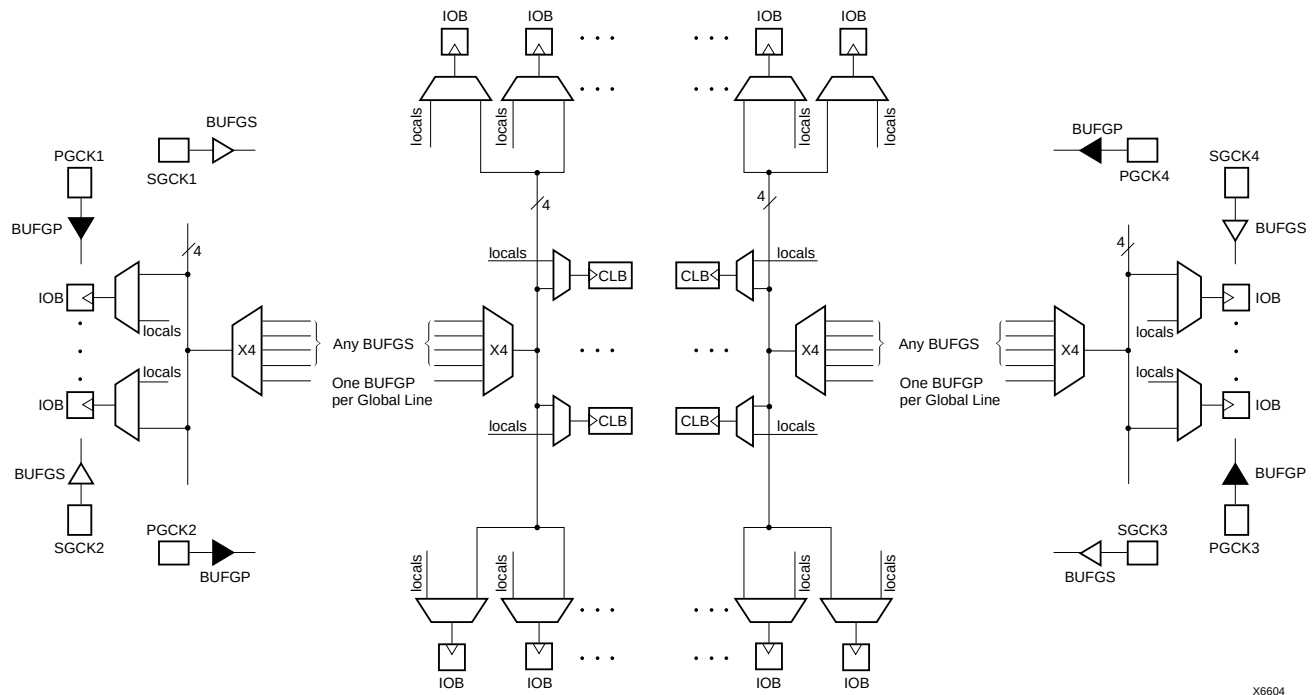
A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), or BUFG (either primary or secondary buffer) element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=L attribute or property to a BUFGS symbol to direct that a buffer be placed in one of the two Secondary Global buffers on the left edge of the device, or a LOC=BL to indicate the Secondary Global buffer on the bottom edge of the device, on the left.

**Table 15: Clock Pin Access**

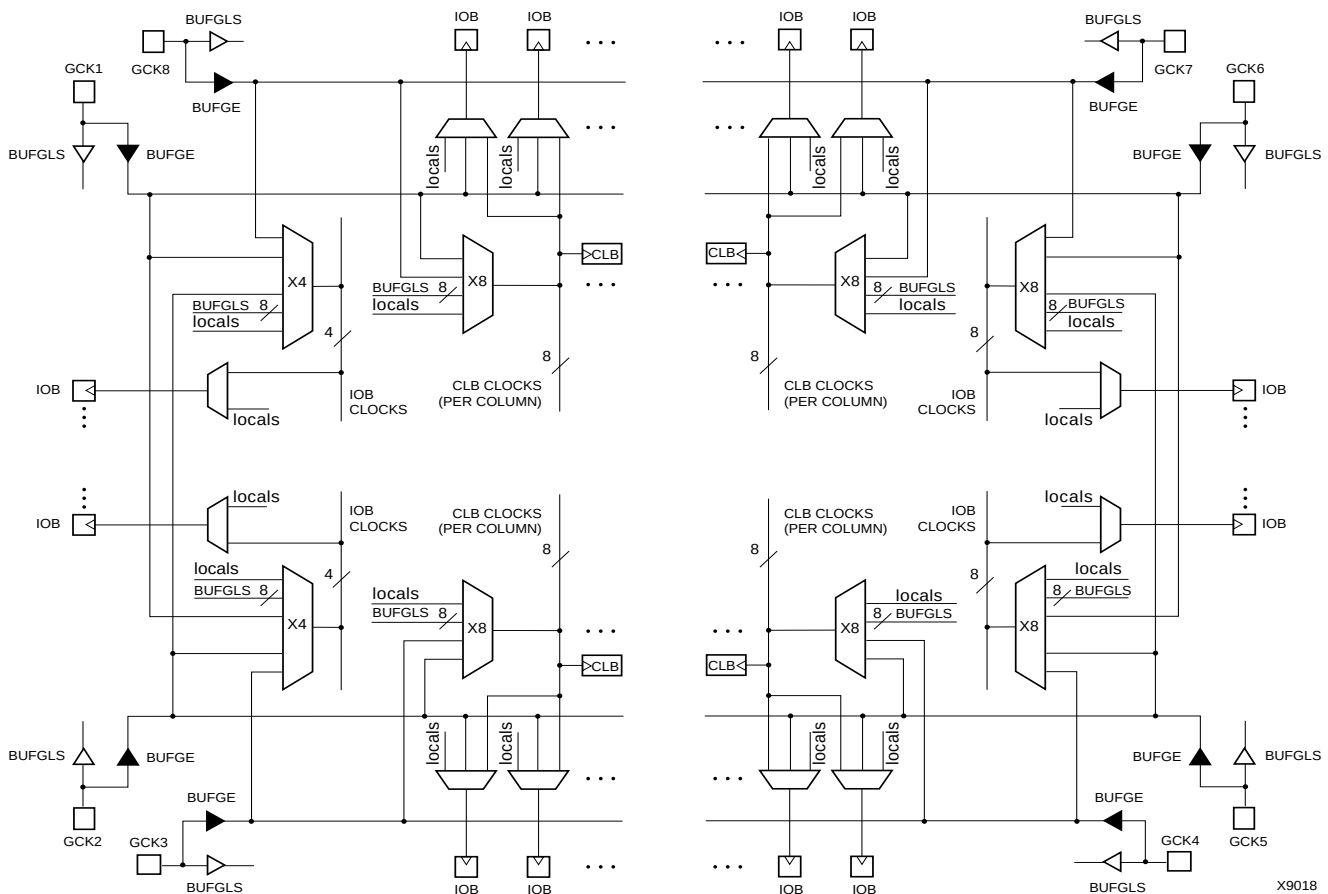
|                                                             | XC4000E |       | XC4000X |             |             | Local Inter-connect |
|-------------------------------------------------------------|---------|-------|---------|-------------|-------------|---------------------|
|                                                             | BUFGP   | BUFGS | BUFGLS  | L & R BUFGE | T & B BUFGE |                     |
| All CLBs in Quadrant                                        | √       | √     | √       | √           | √           | √                   |
| All CLBs in Device                                          | √       | √     | √       |             |             | √                   |
| IOBs on Adjacent Vertical Half Edge                         | √       | √     | √       | √           | √           | √                   |
| IOBs on Adjacent Vertical Full Edge                         | √       | √     | √       | √           |             | √                   |
| IOBs on Adjacent Horizontal Half Edge (Direct)              |         |       |         | √           |             | √                   |
| IOBs on Adjacent Horizontal Half Edge (through CLB globals) | √       | √     | √       | √           | √           | √                   |
| IOBs on Adjacent Horizontal Full Edge (through CLB globals) | √       | √     | √       |             |             | √                   |

L = Left, R = Right, T = Top, B = Bottom





**Figure 34: XC4000E Global Net Distribution**



**Figure 35: XC4000X Global Net Distribution**

**Table 16: Pin Descriptions**

| Pin Name                                             | I/O During Config. | I/O After Config.            | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------------------------------------------------------|--------------------|------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Permanently Dedicated Pins</b>                    |                    |                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| VCC                                                  | I                  | I                            | Eight or more (depending on package) connections to the nominal +5 V supply voltage (+3.3 V for low-voltage devices). All must be connected, and each must be decoupled with a 0.01 - 0.1 $\mu$ F capacitor to Ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| GND                                                  | I                  | I                            | Eight or more (depending on package type) connections to Ground. All must be connected.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| CCLK                                                 | I or O             | I                            | During configuration, Configuration Clock (CCLK) is an output in Master modes or Asynchronous Peripheral mode, but is an input in Slave mode and Synchronous Peripheral mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High or Low time restriction on XC4000 Series devices, except during Readback. See <a href="#">“Violating the Maximum High and Low Time Specification for the Readback Clock” on page 56</a> for an explanation of this exception.                                                                                                                                                                                                                                                                                                                                                            |
| DONE                                                 | I/O                | O                            | DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in the XACTstep program that creates the configuration bitstream. The resistor is included by default.                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| $\overline{\text{PROGRAM}}$                          | I                  | I                            | PROGRAM is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When PROGRAM goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases INIT.<br>The PROGRAM pin has a permanent weak pull-up, so it need not be externally pulled up to Vcc.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>User I/O Pins That Can Have Special Functions</b> |                    |                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| RDY/ $\overline{\text{BUSY}}$                        | O                  | I/O                          | During Peripheral mode configuration, this pin indicates when it is appropriate to write another byte of data into the FPGA. The same status is also available on D7 in Asynchronous Peripheral mode, if a read operation is performed when the device is selected. After configuration, RDY/ $\overline{\text{BUSY}}$ is a user-programmable I/O pin. RDY/ $\overline{\text{BUSY}}$ is pulled High with a high-impedance pull-up prior to $\overline{\text{INIT}}$ going High.                                                                                                                                                                                                                                                                                                                                                                                                               |
| $\overline{\text{RCLK}}$                             | O                  | I/O                          | During Master Parallel configuration, each change on the A0-A17 outputs (A0 - A21 for XC4000X) is preceded by a rising edge on $\overline{\text{RCLK}}$ , a redundant output signal. $\overline{\text{RCLK}}$ is useful for clocked PROMs. It is rarely used during configuration. After configuration, $\overline{\text{RCLK}}$ is a user-programmable I/O pin.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| M0, M1, M2                                           | I                  | I (M0),<br>O (M1),<br>I (M2) | As Mode inputs, these pins are sampled after $\overline{\text{INIT}}$ goes High to determine the configuration mode to be used. After configuration, M0 and M2 can be used as inputs, and M1 can be used as a 3-state output. These three pins have no associated input or output registers.<br>During configuration, these pins have weak pull-up resistors. For the most popular configuration mode, Slave Serial, the mode pins can thus be left unconnected. The three mode inputs can be individually configured with or without weak pull-up or pull-down resistors. A pull-down resistor value of 4.7 k $\Omega$ is recommended.<br>These pins can only be used as inputs or outputs when called out by special schematic definitions. To use these pins, place the library components MD0, MD1, and MD2 instead of the usual pad symbols. Input or output buffers must still be used. |
| TDO                                                  | O                  | O                            | If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed.<br>This pin can be user output only when called out by special schematic definitions. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

Figure 41 on page 44 is a diagram of the XC4000 Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

XC4000 Series devices can also be configured through the boundary scan logic. See “Readback” on page 55.

## Data Registers

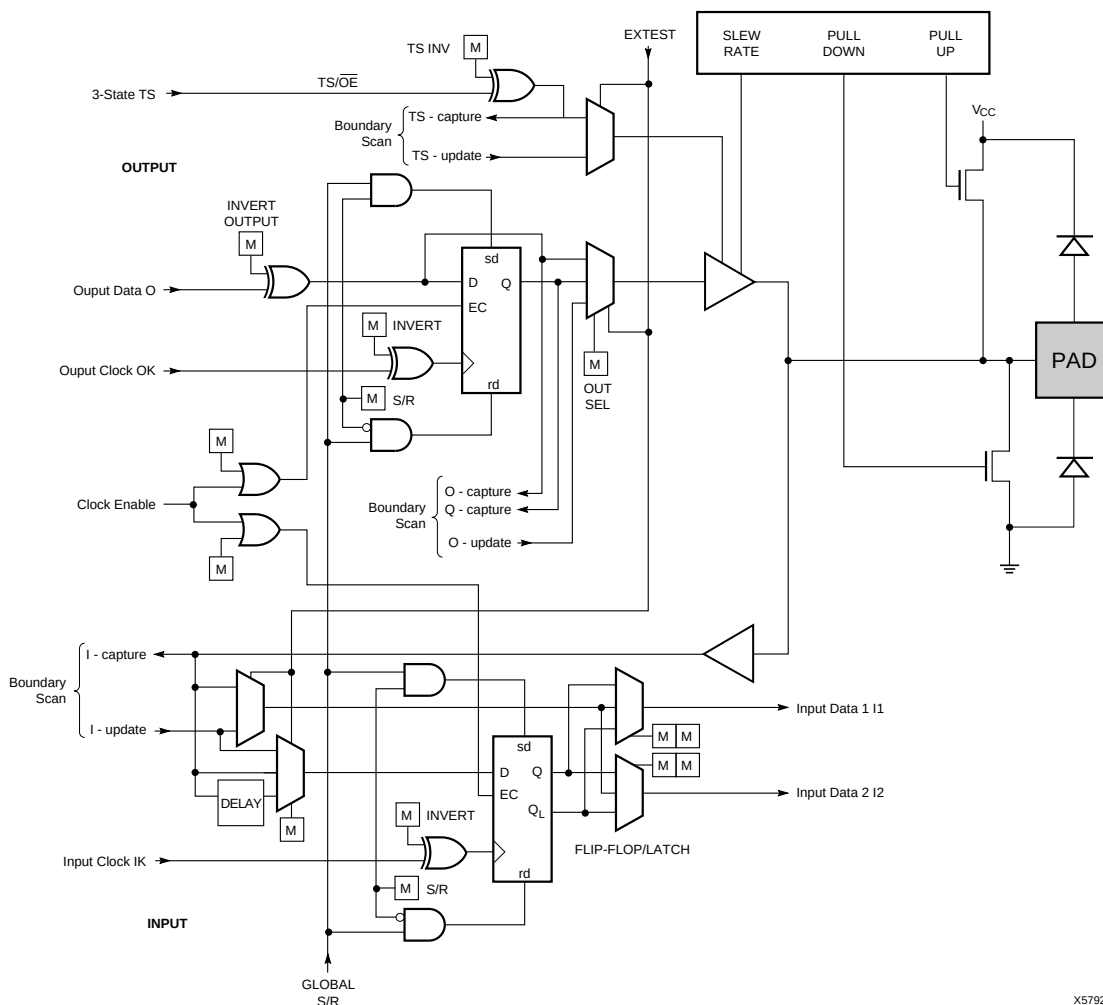
The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-State Control. Non-IOB pins have appropriate partial bit population for In or Out only. PROGRAM, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the

data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).



**Figure 40: Block Diagram of XC4000E IOB with Boundary Scan (some details not shown). XC4000X Boundary Scan Logic is Identical.**

## Configuration Modes

XC4000E devices have six configuration modes. XC4000X devices have the same six modes, plus an additional configuration mode. These modes are selected by a 3-bit input code applied to the M2, M1, and M0 inputs. There are three self-loading Master modes, two Peripheral modes, and a Serial Slave mode, which is used primarily for daisy-chained devices. The coding for mode selection is shown in [Table 18](#).

**Table 18: Configuration Modes**

| Mode                    | M2 | M1 | M0 | CCLK   | Data                            |
|-------------------------|----|----|----|--------|---------------------------------|
| Master Serial           | 0  | 0  | 0  | output | Bit-Serial                      |
| Slave Serial            | 1  | 1  | 1  | input  | Bit-Serial                      |
| Master Parallel Up      | 1  | 0  | 0  | output | Byte-Wide, increment from 00000 |
| Master Parallel Down    | 1  | 1  | 0  | output | Byte-Wide, decrement from 3FFFF |
| Peripheral Synchronous* | 0  | 1  | 1  | input  | Byte-Wide                       |
| Peripheral Asynchronous | 1  | 0  | 1  | output | Byte-Wide                       |
| Reserved                | 0  | 1  | 0  | —      | —                               |
| Reserved                | 0  | 0  | 1  | —      | —                               |

\* Can be considered byte-wide Slave Parallel

A detailed description of each configuration mode, with timing information, is included later in this data sheet. During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during configuration are shown in [Table 22 on page 58](#).

### Master Modes

The three Master modes use an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices. They also generate address and timing for external PROM(s) containing the configuration data.

Master Parallel (Up or Down) modes generate the CCLK signal and PROM addresses and receive byte parallel data. The data is internally serialized into the FPGA data-frame format. The up and down selection generates starting addresses at either zero or 3FFFF (3FFFFFF when 22 address lines are used), for compatibility with different microprocessor addressing conventions. The Master Serial mode generates CCLK and receives the configuration data in serial form from a Xilinx serial-configuration PROM.

CCLK speed is selectable as either 1 MHz (default) or 8 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to +25%.

### Additional Address lines in XC4000 devices

The XC4000X devices have additional address lines (A18-A21) allowing the additional address space required to daisy-chain several large devices.

The extra address lines are programmable in XC4000EX devices. By default these address lines are not activated. In the default mode, the devices are compatible with existing XC4000 and XC4000E products. If desired, the extra address lines can be used by specifying the address lines option in bitgen as 22 (bitgen -g AddressLines:22). The lines (A18-A21) are driven when a master device detects, via the bitstream, that it should be using all 22 address lines. Because these pins will initially be pulled high by internal pull-ups, designers using Master Parallel Up mode should use external pull down resistors on pins A18-A21. If Master Parallel Down mode is used external resistors are not necessary.

All 22 address lines are always active in Master Parallel modes with XC4000XL devices. The additional address lines behave identically to the lower order address lines. If the Address Lines option in bitgen is set to 18, it will be ignored by the XC4000XL device.

The additional address lines (A18-A21) are not available in the PC84 package.

### Peripheral Modes

The two Peripheral modes accept byte-wide data from a bus. A RDY/BUSY status is available as a handshake signal. In Asynchronous Peripheral mode, the internal oscillator generates a CCLK burst signal that serializes the byte-wide data. CCLK can also drive slave devices. In the synchronous mode, an externally supplied clock input to CCLK serializes the data.

### Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

### Serial Daisy Chain

Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in [Figure 51 on page 60](#). Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count,

Low. During this time delay, or as long as the  $\overline{\text{PROGRAM}}$  input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator.

At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the  $\overline{\text{PROGRAM}}$  pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the  $\overline{\text{INIT}}$  input.

### Initialization

During initialization and configuration, user pins  $\text{HDC}$ ,  $\overline{\text{LDC}}$ ,  $\overline{\text{INIT}}$  and  $\text{DONE}$  provide status outputs for the system interface. The outputs  $\overline{\text{LDC}}$ ,  $\overline{\text{INIT}}$  and  $\text{DONE}$  are held Low and  $\text{HDC}$  is held High starting at the initial application of power.

The open drain  $\overline{\text{INIT}}$  pin is released after the final initialization pass through the frame addresses. There is a deliberate delay of 50 to 250  $\mu\text{s}$  (up to 10% longer for low-voltage devices) before a Master-mode device recognizes an inactive  $\overline{\text{INIT}}$ . Two internal clocks after the  $\overline{\text{INIT}}$  pin is recognized as High, the FPGA samples the three mode lines to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded. Configuration

The 0010 preamble code indicates that the following 24 bits represent the length count. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to all devices in the daisy chain,  $\text{DOUT}$  is held High to prevent frame start bits from reaching any daisy-chained devices.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain  $\overline{\text{INIT}}$  pin Low. After all configuration frames have been loaded into an FPGA,  $\text{DOUT}$  again follows the input data so that the remaining data is passed on to the next device.

### Delaying Configuration After Power-Up

There are two methods of delaying configuration after power-up: put a logic Low on the  $\overline{\text{PROGRAM}}$  input, or pull the bidirectional  $\overline{\text{INIT}}$  pin Low, using an open-collector (open-drain) driver. (See [Figure 46 on page 50](#).)

A Low on the  $\overline{\text{PROGRAM}}$  input is the more radical approach, and is recommended when the power-supply

rise time is excessive or poorly defined. As long as  $\overline{\text{PROGRAM}}$  is Low, the FPGA keeps clearing its configuration memory. When  $\overline{\text{PROGRAM}}$  goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the  $\overline{\text{INIT}}$  input is not externally held Low. Note that a Low on the  $\overline{\text{PROGRAM}}$  input automatically forces a Low on the  $\overline{\text{INIT}}$  output. The XC4000 Series  $\overline{\text{PROGRAM}}$  pin has a permanent weak pull-up.

Using an open-collector or open-drain driver to hold  $\overline{\text{INIT}}$  Low before the beginning of configuration causes the FPGA to wait after completing the configuration memory clear operation. When  $\overline{\text{INIT}}$  is no longer held Low externally, the device determines its configuration mode by capturing its mode pins, and is ready to start the configuration process. A master device waits up to an additional 250  $\mu\text{s}$  to make sure that any slaves in the optional daisy chain have seen that  $\overline{\text{INIT}}$  is High.

### Start-Up

Start-up is the transition from the configuration process to the intended user operation. This transition involves a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user-system. Start-up must make sure that the user-logic 'wakes up' gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the global Reset or Set at the right time.

[Figure 47](#) describes start-up timing for the three Xilinx families in detail. The configuration modes can use any of the four timing sequences.

To access the internal start-up signals, place the  $\text{STARTUP}$  library symbol.

### Start-up Timing

Different FPGA families have different start-up sequences.

The XC2000 family goes through a fixed sequence.  $\text{DONE}$  goes High and the internal global Reset is de-activated one CCLK period after the I/O become active.

The XC3000A family offers some flexibility.  $\text{DONE}$  can be programmed to go High one CCLK period before or after the I/O become active. Independent of  $\text{DONE}$ , the internal global Reset is de-activated one CCLK period before or after the I/O become active.

The XC4000 Series offers additional flexibility. The three events —  $\text{DONE}$  going High, the internal Set/Reset being de-activated, and the user I/O going active — can all occur in any arbitrary sequence. Each of them can occur one CCLK period before or after, or simultaneous with, any of the others. This relative timing is selected by means of software options in the bitstream generation software.



### **Start-up from a User Clock (STARTUP.CLK)**

When, instead of CCLK, a user-supplied start-up clock is selected, Q1 is used to bridge the unknown phase relationship between CCLK and the user clock. This arbitration causes an unavoidable one-cycle uncertainty in the timing of the rest of the start-up sequence.

### **DONE Goes High to Signal End of Configuration**

XC4000 Series devices read the expected length count from the bitstream and store it in an internal register. The length count varies according to the number of devices and the composition of the daisy chain. Each device also counts the number of CCLKs during configuration.

Two conditions have to be met in order for the DONE pin to go high:

- the chip's internal memory must be full, and
- the configuration length count must be met, *exactly*.

This is important because the counter that determines when the length count is met begins with the very first CCLK, not the first one after the preamble.

Therefore, if a stray bit is inserted before the preamble, or the data source is not ready at the time of the first CCLK, the internal counter that holds the number of CCLKs will be one ahead of the actual number of data bits read. At the end of configuration, the configuration memory will be full, but the number of bits in the internal counter will not match the expected length count.

As a consequence, a Master mode device will continue to send out CCLKs until the internal counter turns over to zero, and then reaches the correct length count a second time. This will take several seconds [ $2^{24} * \text{CCLK period}$ ] — which is sometimes interpreted as the device not configuring at all.

If it is not possible to have the data ready at the time of the first CCLK, the problem can be avoided by increasing the number in the length count by the appropriate value. The *XACT User Guide* includes detailed information about manually altering the length count.

Note that DONE is an open-drain output and does not go High unless an internal pull-up is activated or an external pull-up is attached. The internal pull-up is activated as the default by the bitstream generation software.

### **Release of User I/O After DONE Goes High**

By default, the user I/O are released one CCLK cycle after the DONE pin goes High. If CCLK is not clocked after DONE goes High, the outputs remain in their initial state — 3-stated, with a 50 k $\Omega$  - 100 k $\Omega$  pull-up. The delay from DONE High to active user I/O is controlled by an option to the bitstream generation software.

### **Release of Global Set/Reset After DONE Goes High**

By default, Global Set/Reset (GSR) is released two CCLK cycles after the DONE pin goes High. If CCLK is not clocked twice after DONE goes High, all flip-flops are held in their initial set or reset state. The delay from DONE High to GSR inactive is controlled by an option to the bitstream generation software.

### **Configuration Complete After DONE Goes High**

Three full CCLK cycles are required after the DONE pin goes High, as shown in [Figure 47 on page 53](#). If CCLK is not clocked three times after DONE goes High, readback cannot be initiated and most boundary scan instructions cannot be used.

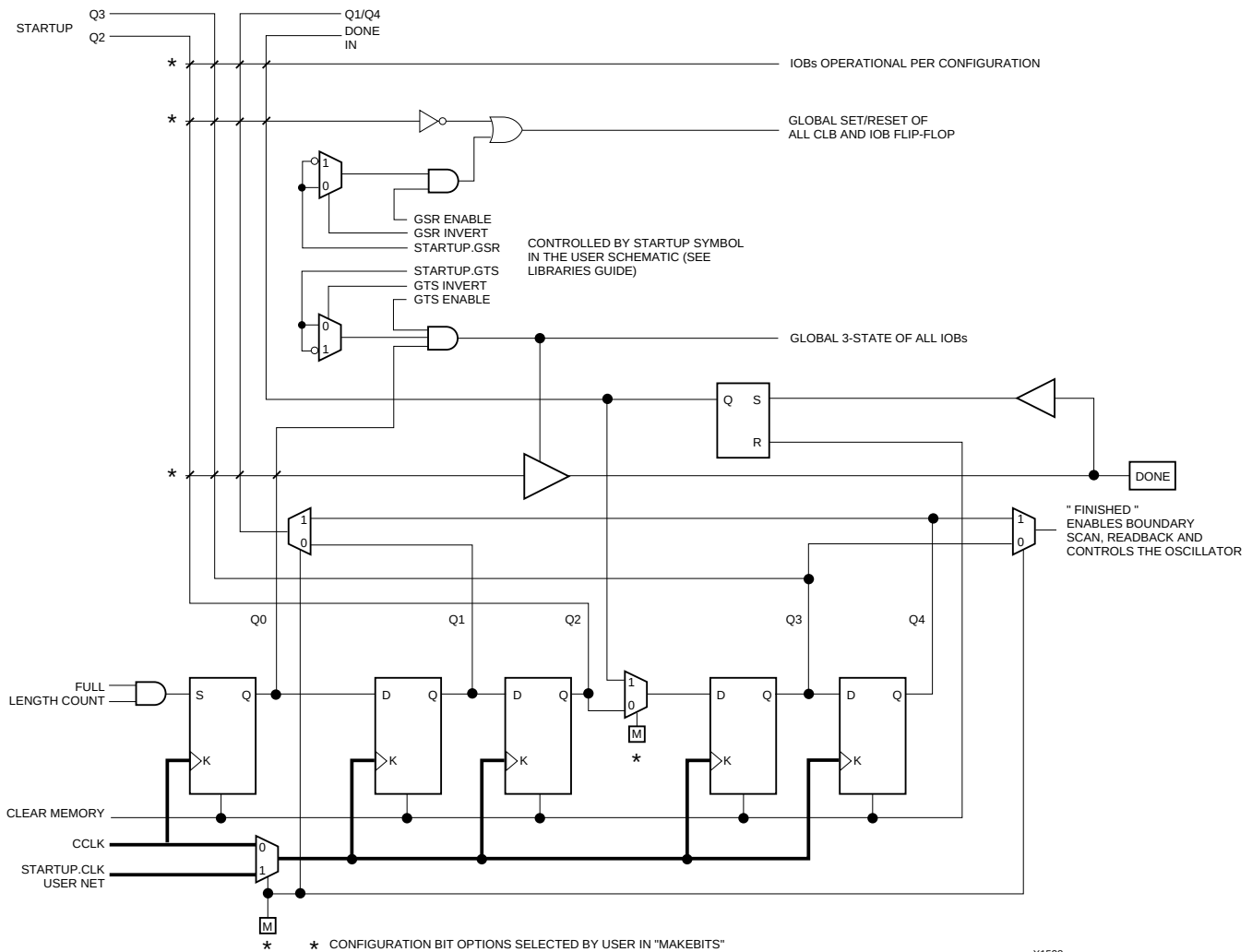
### **Configuration Through the Boundary Scan Pins**

XC4000 Series devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with  $\overline{\text{INIT}}$  held Low (or drive the  $\overline{\text{PROGRAM}}$  pin Low for more than 300 ns followed by a High while holding  $\overline{\text{INIT}}$  Low). Holding  $\overline{\text{INIT}}$  Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold  $\overline{\text{INIT}}$  Low.
- Issue the CONFIG command to the TMS input
- Wait for  $\overline{\text{INIT}}$  to go High
- Sequence the boundary scan Test Access Port to the SHIFT-DR state
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after INIT goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note XAPP017, “*Boundary Scan in XC4000 Devices*.” This application note also applies to XC4000E and XC4000X devices.



**Figure 48: Start-up Logic**

## Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Note that in XC4000 Series devices, configuration data is *not* inverted with respect to configuration as it is in XC2000 and XC3000 families.

XC4000 Series Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, place the READ-

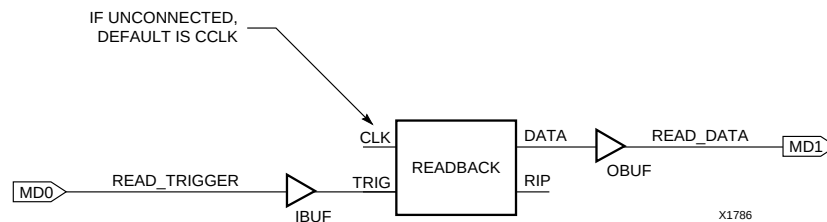
BACK library symbol and attach the appropriate pad symbols, as shown in [Figure 49](#).

After Readback has been initiated by a High level on RDBK.TRIG after configuration, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.





**Figure 49: Readback Schematic Example**

## Readback Options

Readback options are: Read Capture, Read Abort, and Clock Select. They are set with the bitstream generation software.

### Read Capture

When the Read Capture option is selected, the readback data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals *are* inverted.

When the Read Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations.

If the RAM capability of the CLBs is used, RAM data are available in readback, since they directly overwrite the F and G function-table configuration of the CLB.

RDBK.TRIG is located in the lower-left corner of the device, as shown in [Figure 50](#).

### Read Abort

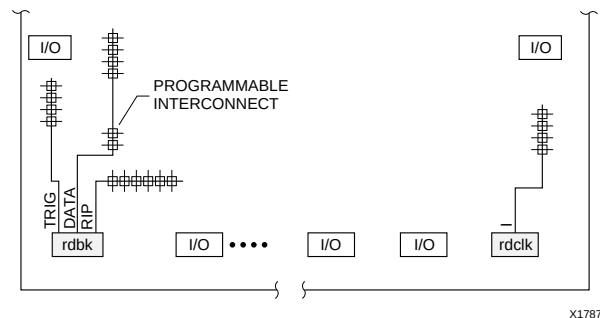
When the Read Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the readback operation and prepares the logic to accept another trigger.

After an aborted readback, additional clocks (up to one readback clock per configuration frame) may be required to re-initialize the control logic. The status of readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

### Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If readback must be inhibited for security reasons, the readback control nets are simply not connected.

RDBK.CLK is located in the lower right chip corner, as shown in [Figure 50](#).



**Figure 50: READBACK Symbol in Graphical Editor**

## Violating the Maximum High and Low Time Specification for the Readback Clock

The readback clock has a maximum High and Low time specification. In some cases, this specification cannot be met. For example, if a processor is controlling readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in [Table 19](#), [Table 20](#) and [Table 21](#).

## Readback with the XChecker Cable

The XChecker Universal Download/Readback Cable and Logic Probe uses the readback feature for bitstream verification. It can also display selected internal signals on the PC or workstation screen, functioning as a low-cost in-circuit emulator.

**Table 22: Pin Functions During Configuration**

| CONFIGURATION MODE <M2:M1:M0> |                             |                                 |                                  |                                    |                                  | USER<br>OPERATION |
|-------------------------------|-----------------------------|---------------------------------|----------------------------------|------------------------------------|----------------------------------|-------------------|
| SLAVE<br>SERIAL<br><1:1:1>    | MASTER<br>SERIAL<br><0:0:0> | SYNCH.<br>PERIPHERAL<br><0:1:1> | ASYNCH.<br>PERIPHERAL<br><1:0:1> | MASTER<br>PARALLEL DOWN<br><1:1:0> | MASTER<br>PARALLEL UP<br><1:0:0> |                   |
| M2(HIGH) (I)                  | M2(LOW) (I)                 | M2(LOW) (I)                     | M2(HIGH) (I)                     | M2(HIGH) (I)                       | M2(HIGH) (I)                     | (I)               |
| M1(HIGH) (I)                  | M1(LOW) (I)                 | M1(HIGH) (I)                    | M1(LOW) (I)                      | M1(HIGH) (I)                       | M1(LOW) (I)                      | (O)               |
| M0(HIGH) (I)                  | M0(LOW) (I)                 | M0(HIGH) (I)                    | M0(HIGH) (I)                     | M0(LOW) (I)                        | M0(LOW) (I)                      | (I)               |
| HDC (HIGH)                    | HDC (HIGH)                  | HDC (HIGH)                      | HDC (HIGH)                       | HDC (HIGH)                         | HDC (HIGH)                       | I/O               |
| LDC (LOW)                     | LDC (LOW)                   | LDC (LOW)                       | LDC (LOW)                        | LDC (LOW)                          | LDC (LOW)                        | I/O               |
| INIT                          | INIT                        | INIT                            | INIT                             | INIT                               | INIT                             | I/O               |
| DONE                          | DONE                        | DONE                            | DONE                             | DONE                               | DONE                             | DONE              |
| PROGRAM (I)                   | PROGRAM (I)                 | PROGRAM (I)                     | PROGRAM (I)                      | PROGRAM (I)                        | PROGRAM (I)                      | PROGRAM           |
| CCLK (I)                      | CCLK (O)                    | CCLK (I)                        | CCLK (O)                         | CCLK (O)                           | CCLK (O)                         | CCLK (I)          |
|                               |                             | RDY/BUSY (O)                    | RDY/BUSY (O)                     | RCLK (O)                           | RCLK (O)                         | I/O               |
|                               |                             |                                 | RS (I)                           |                                    |                                  | I/O               |
|                               |                             |                                 | CS0 (I)                          |                                    |                                  | I/O               |
|                               |                             | DATA 7 (I)                      | DATA 7 (I)                       | DATA 7 (I)                         | DATA 7 (I)                       | I/O               |
|                               |                             | DATA 6 (I)                      | DATA 6 (I)                       | DATA 6 (I)                         | DATA 6 (I)                       | I/O               |
|                               |                             | DATA 5 (I)                      | DATA 5 (I)                       | DATA 5 (I)                         | DATA 5 (I)                       | I/O               |
|                               |                             | DATA 4 (I)                      | DATA 4 (I)                       | DATA 4 (I)                         | DATA 4 (I)                       | I/O               |
|                               |                             | DATA 3 (I)                      | DATA 3 (I)                       | DATA 3 (I)                         | DATA 3 (I)                       | I/O               |
|                               |                             | DATA 2 (I)                      | DATA 2 (I)                       | DATA 2 (I)                         | DATA 2 (I)                       | I/O               |
|                               |                             | DATA 1 (I)                      | DATA 1 (I)                       | DATA 1 (I)                         | DATA 1 (I)                       | I/O               |
| DIN (I)                       | DIN (I)                     | DATA 0 (I)                      | DATA 0 (I)                       | DATA 0 (I)                         | DATA 0 (I)                       | I/O               |
| DOUT                          | DOUT                        | DOUT                            | DOUT                             | DOUT                               | DOUT                             | SGCK4-GCK6-I/O    |
| TDI                           | TDI                         | TDI                             | TDI                              | TDI                                | TDI                              | TDI-I/O           |
| TCK                           | TCK                         | TCK                             | TCK                              | TCK                                | TCK                              | TCK-I/O           |
| TMS                           | TMS                         | TMS                             | TMS                              | TMS                                | TMS                              | TMS-I/O           |
| TDO                           | TDO                         | TDO                             | TDO                              | TDO                                | TDO                              | TDO-(O)           |
|                               |                             |                                 | WS (I)                           | A0                                 | A0                               | I/O               |
|                               |                             |                                 |                                  | A1                                 | A1                               | PGCK4-GCK7-I/O    |
|                               |                             |                                 | CS1                              | A2                                 | A2                               | I/O               |
|                               |                             |                                 |                                  | A3                                 | A3                               | I/O               |
|                               |                             |                                 |                                  | A4                                 | A4                               | I/O               |
|                               |                             |                                 |                                  | A5                                 | A5                               | I/O               |
|                               |                             |                                 |                                  | A6                                 | A6                               | I/O               |
|                               |                             |                                 |                                  | A7                                 | A7                               | I/O               |
|                               |                             |                                 |                                  | A8                                 | A8                               | I/O               |
|                               |                             |                                 |                                  | A9                                 | A9                               | I/O               |
|                               |                             |                                 |                                  | A10                                | A10                              | I/O               |
|                               |                             |                                 |                                  | A11                                | A11                              | I/O               |
|                               |                             |                                 |                                  | A12                                | A12                              | I/O               |
|                               |                             |                                 |                                  | A13                                | A13                              | I/O               |
|                               |                             |                                 |                                  | A14                                | A14                              | I/O               |
|                               |                             |                                 |                                  | A15                                | A15                              | SGCK1-GCK8-I/O    |
|                               |                             |                                 |                                  | A16                                | A16                              | PGCK1-GCK1-I/O    |
|                               |                             |                                 |                                  | A17                                | A17                              | I/O               |
|                               |                             |                                 |                                  | A18*                               | A18*                             | I/O               |
|                               |                             |                                 |                                  | A19*                               | A19*                             | I/O               |
|                               |                             |                                 |                                  | A20*                               | A20*                             | I/O               |
|                               |                             |                                 |                                  | A21*                               | A21*                             | I/O               |
|                               |                             |                                 |                                  |                                    |                                  | ALL OTHERS        |

**Table 23: Pin Functions During Configuration**

| CONFIGURATION MODE <M2:M1:M0> |                          |                              |                               |                                 |                               | USER OPERATION |
|-------------------------------|--------------------------|------------------------------|-------------------------------|---------------------------------|-------------------------------|----------------|
| SLAVE SERIAL<br><1:1:1>       | MASTER SERIAL<br><0:0:0> | SYNCH. PERIPHERAL<br><0:1:1> | ASYNCH. PERIPHERAL<br><1:0:1> | MASTER PARALLEL DOWN<br><1:1:0> | MASTER PARALLEL UP<br><1:0:0> |                |
| M2(HIGH) (I)                  | M2(LOW) (I)              | M2(LOW) (I)                  | M2(HIGH) (I)                  | M2(HIGH) (I)                    | M2(HIGH) (I)                  | (I)            |
| M1(HIGH) (I)                  | M1(LOW) (I)              | M1(HIGH) (I)                 | M1(LOW) (I)                   | M1(HIGH) (I)                    | M1(LOW) (I)                   | (O)            |
| M0(HIGH) (I)                  | M0(LOW) (I)              | M0(HIGH) (I)                 | M0(HIGH) (I)                  | M0(LOW) (I)                     | M0(LOW) (I)                   | (I)            |
| HDC (HIGH)                    | HDC (HIGH)               | HDC (HIGH)                   | HDC (HIGH)                    | HDC (HIGH)                      | HDC (HIGH)                    | I/O            |
| LDC (LOW)                     | LDC (LOW)                | LDC (LOW)                    | LDC (LOW)                     | LDC (LOW)                       | LDC (LOW)                     | I/O            |
| INIT                          | INIT                     | INIT                         | INIT                          | INIT                            | INIT                          | I/O            |
| DONE                          | DONE                     | DONE                         | DONE                          | DONE                            | DONE                          | DONE           |
| PROGRAM (I)                   | PROGRAM (I)              | PROGRAM (I)                  | PROGRAM (I)                   | PROGRAM (I)                     | PROGRAM (I)                   | PROGRAM        |
| CCLK (I)                      | CCLK (O)                 | CCLK (I)                     | CCLK (O)                      | CCLK (O)                        | CCLK (O)                      | CCLK (I)       |
|                               |                          | RDY/BUSY (O)                 | RDY/BUSY (O)                  | RCLK (O)                        | RCLK (O)                      | I/O            |
|                               |                          |                              | RS (I)                        |                                 |                               | I/O            |
|                               |                          |                              | CS0 (I)                       |                                 |                               | I/O            |
|                               |                          | DATA 7 (I)                   | DATA 7 (I)                    | DATA 7 (I)                      | DATA 7 (I)                    | I/O            |
|                               |                          | DATA 6 (I)                   | DATA 6 (I)                    | DATA 6 (I)                      | DATA 6 (I)                    | I/O            |
|                               |                          | DATA 5 (I)                   | DATA 5 (I)                    | DATA 5 (I)                      | DATA 5 (I)                    | I/O            |
|                               |                          | DATA 4 (I)                   | DATA 4 (I)                    | DATA 4 (I)                      | DATA 4 (I)                    | I/O            |
|                               |                          | DATA 3 (I)                   | DATA 3 (I)                    | DATA 3 (I)                      | DATA 3 (I)                    | I/O            |
|                               |                          | DATA 2 (I)                   | DATA 2 (I)                    | DATA 2 (I)                      | DATA 2 (I)                    | I/O            |
|                               |                          | DATA 1 (I)                   | DATA 1 (I)                    | DATA 1 (I)                      | DATA 1 (I)                    | I/O            |
| DIN (I)                       | DIN (I)                  | DATA 0 (I)                   | DATA 0 (I)                    | DATA 0 (I)                      | DATA 0 (I)                    | I/O            |
| DOUT                          | DOUT                     | DOUT                         | DOUT                          | DOUT                            | DOUT                          | SGCK4-GCK6-I/O |
| TDI                           | TDI                      | TDI                          | TDI                           | TDI                             | TDI                           | TDI-I/O        |
| TCK                           | TCK                      | TCK                          | TCK                           | TCK                             | TCK                           | TCK-I/O        |
| TMS                           | TMS                      | TMS                          | TMS                           | TMS                             | TMS                           | TMS-I/O        |
| TDO                           | TDO                      | TDO                          | TDO                           | TDO                             | TDO                           | TDO-(O)        |
|                               |                          |                              | WS (I)                        | A0                              | A0                            | I/O            |
|                               |                          |                              |                               | A1                              | A1                            | PGCK4-GCK7-I/O |
|                               |                          |                              | CS1                           | A2                              | A2                            | I/O            |
|                               |                          |                              |                               | A3                              | A3                            | I/O            |
|                               |                          |                              |                               | A4                              | A4                            | I/O            |
|                               |                          |                              |                               | A5                              | A5                            | I/O            |
|                               |                          |                              |                               | A6                              | A6                            | I/O            |
|                               |                          |                              |                               | A7                              | A7                            | I/O            |
|                               |                          |                              |                               | A8                              | A8                            | I/O            |
|                               |                          |                              |                               | A9                              | A9                            | I/O            |
|                               |                          |                              |                               | A10                             | A10                           | I/O            |
|                               |                          |                              |                               | A11                             | A11                           | I/O            |
|                               |                          |                              |                               | A12                             | A12                           | I/O            |
|                               |                          |                              |                               | A13                             | A13                           | I/O            |
|                               |                          |                              |                               | A14                             | A14                           | I/O            |
|                               |                          |                              |                               | A15                             | A15                           | SGCK1-GCK8-I/O |
|                               |                          |                              |                               | A16                             | A16                           | PGCK1-GCK1-I/O |
|                               |                          |                              |                               | A17                             | A17                           | I/O            |
|                               |                          |                              |                               | A18*                            | A18*                          | I/O            |
|                               |                          |                              |                               | A19*                            | A19*                          | I/O            |
|                               |                          |                              |                               | A20*                            | A20*                          | I/O            |
|                               |                          |                              |                               | A21*                            | A21*                          | I/O            |
|                               |                          |                              |                               |                                 |                               | ALL OTHERS     |

\* XC4000X only

- Notes
1. A shaded table cell represents a 50 kΩ - 100 kΩ pull-up before and during configuration.
  2. (I) represents an input; (O) represents an output.
  3. INIT is an open-drain output during configuration.

## Configuration Timing

The seven configuration modes are discussed in detail in this section. Timing specifications are included.

## Slave Serial Mode

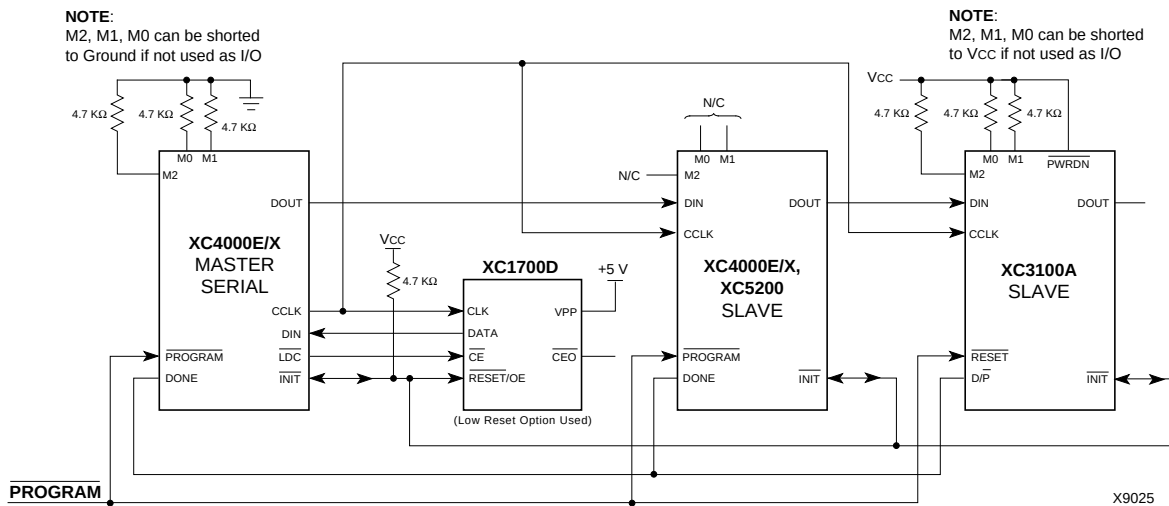
In Slave Serial mode, an external signal drives the CCLK input of the FPGA. The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin.

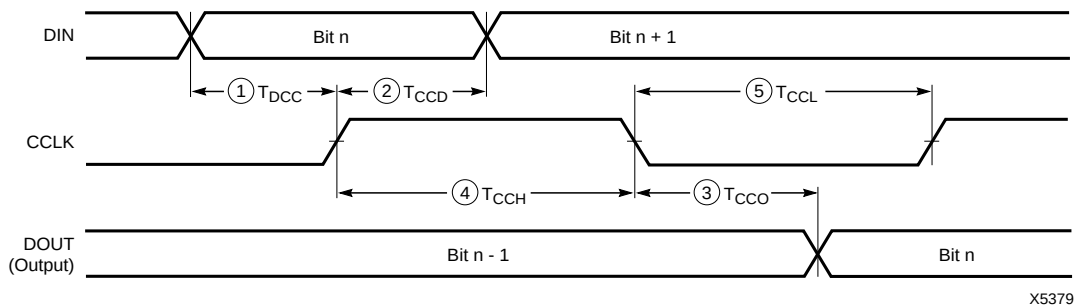
There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

**Figure 51** shows a full master/slave system. An XC4000 Series device in Slave Serial mode should be connected as shown in the third device from the left.

Slave Serial mode is selected by a <111> on the mode pins (M2, M1, M0). Slave Serial is the default mode if the mode pins are left unconnected, as they have weak pull-up resistors during configuration.



**Figure 51: Master/Slave Serial Mode Circuit Diagram**



|      | Description | Symbol |                  | Min | Max | Units |
|------|-------------|--------|------------------|-----|-----|-------|
| CCLK | DIN setup   | 1      | T <sub>DCC</sub> | 20  |     | ns    |
|      | DIN hold    | 2      | T <sub>CCD</sub> | 0   |     | ns    |
|      | DIN to DOUT | 3      | T <sub>CCO</sub> |     | 30  | ns    |
|      | High time   | 4      | T <sub>CCH</sub> | 45  |     | ns    |
|      | Low time    | 5      | T <sub>CCL</sub> | 45  |     | ns    |
|      | Frequency   |        | F <sub>CC</sub>  |     | 10  | MHz   |

Note: Configuration must be delayed until the  $\overline{\text{INIT}}$  pins of all daisy-chained FPGAs are High.

### Figure 52: Slave Serial Mode Programming Switching Characteristics

## Asynchronous Peripheral Mode

### Write to FPGA

Asynchronous Peripheral mode uses the trailing edge of the logic AND condition of  $\overline{WS}$  and  $\overline{CS0}$  being Low and  $\overline{RS}$  and  $\overline{CS1}$  being High to accept byte-wide data from a microprocessor bus. In the lead FPGA, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic.

The lead FPGA presents the preamble data (and all data that overflows the lead device) on its DOUT pin. The RDY/BUSY output from the lead FPGA acts as a handshake signal to the microprocessor. RDY/BUSY goes Low when a byte has been received, and goes High again when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. A new write may be started immediately, as soon as the RDY/BUSY output has gone Low, acknowledging receipt of the previous data. Write may not be terminated until RDY/BUSY is High again for one CCLK period. Note that RDY/BUSY is pulled High with a high-impedance pull-up prior to  $\overline{INIT}$  going High.

The length of the  $\overline{BUSY}$  signal depends on the activity in the UART. If the shift register was empty when the new byte was received, the  $\overline{BUSY}$  signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the  $\overline{BUSY}$  signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with DOUT equal to bit 6 (the next-to-last bit) of the last byte entered.

The RDY/ $\overline{BUSY}$  handshake can be ignored if the delay from any one Write to the end of the next Write is guaranteed to be longer than 10 CCLK periods.

### Status Read

The logic AND condition of the  $\overline{CS0}$ ,  $\overline{CS1}$  and  $\overline{RS}$  inputs puts the device status on the Data bus.

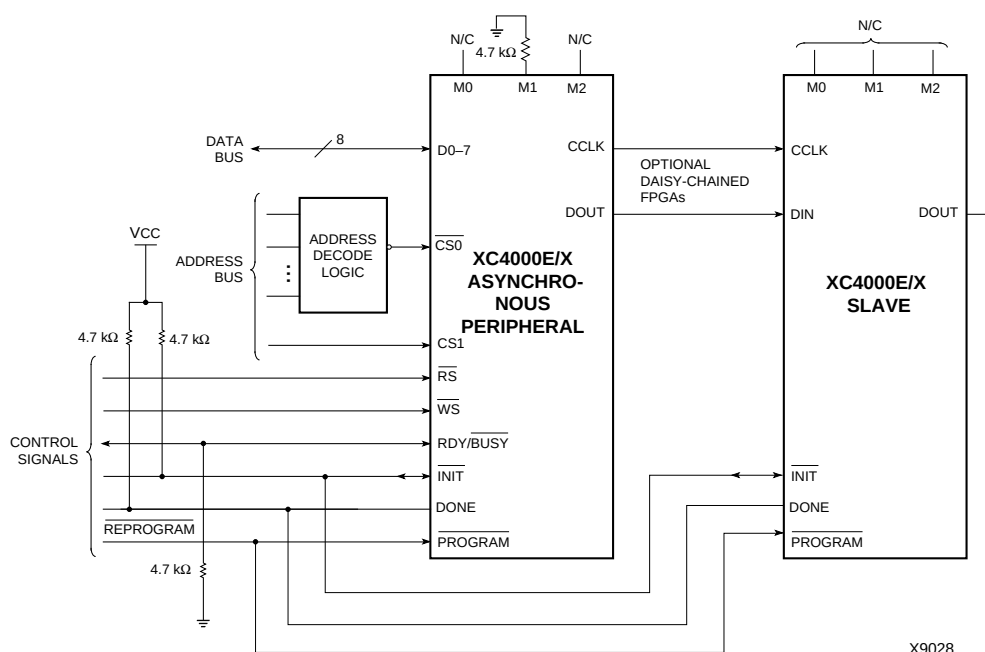
- D7 High indicates Ready
- D7 Low indicates Busy
- D0 through D6 go unconditionally High

It is mandatory that the whole start-up sequence be started and completed by one byte-wide input. Otherwise, the pins used as Write Strobe or Chip Enable might become active outputs and interfere with the final byte transfer. If this transfer does not occur, the start-up sequence is not completed all the way to the finish (point F in [Figure 47 on page 53](#)).

In this case, at worst, the internal reset is not released. At best, Readback and Boundary Scan are inhibited. The length-count value, as generated by the XACTstep software, ensures that these problems never occur.

Although RDY/ $\overline{BUSY}$  is brought out as a separate signal, microprocessors can more easily read this information on one of the data lines. For this purpose, D7 represents the RDY/ $\overline{BUSY}$  status when  $\overline{RS}$  is Low,  $\overline{WS}$  is High, and the two chip select lines are both active.

Asynchronous Peripheral mode is selected by a <101> on the mode pins (M2, M1, M0).



**Figure 58: Asynchronous Peripheral Mode Circuit Diagram**

## XC4000 Series Electrical Characteristics and Device-Specific Pinout Table

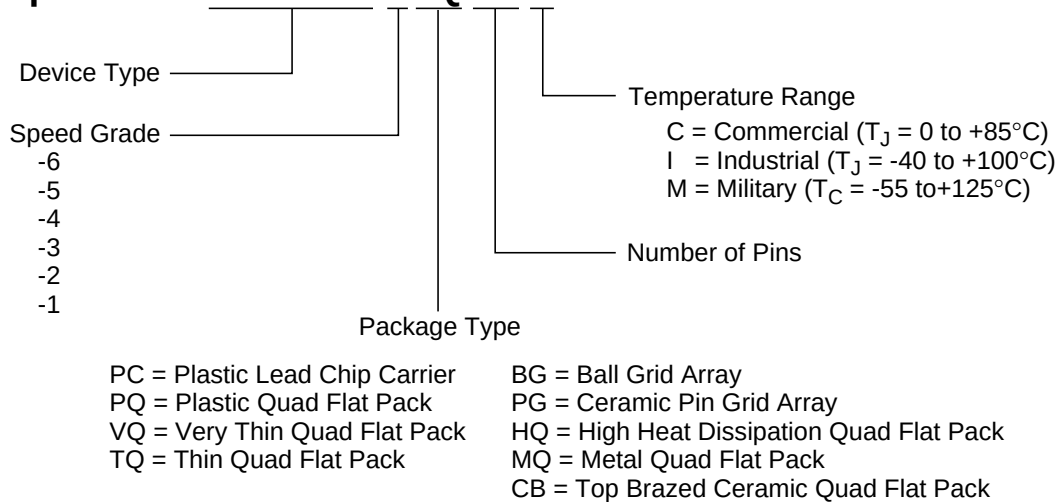
For the latest Electrical Characteristics and package/pinout information for each XC4000 Family, see the Xilinx web site at

[http://www.xilinx.com/xlnx/xweb/xil\\_publications\\_index.jsp](http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp)

## Ordering Information

### Example:

# XC4013E-3HQ240C



X9020

## Revision Control

| Version       | Description                                                                                                                                                                |
|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3/30/98 (1.5) | Updated XC4000XL timing and added XC4002XL                                                                                                                                 |
| 1/29/99 (1.5) | Updated pin diagrams                                                                                                                                                       |
| 5/14/99 (1.6) | Replaced Electrical Specification and pinout pages for E, EX, and XL families with separate updates and added URL link for electrical specifications/pinouts for Web users |