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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 256 |
| Number of Logic Elements/Cells | 608 |
| Total RAM Bits | 8192 |
| Number of I/O | 61 |
| Number of Gates | 6000 |
| Voltage - Supply | 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 84-LCC (J-Lead) |
| Supplier Device Package | 84-PLCC (29.31x29.31) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc4006e-3pc84i |

### *Input Thresholds*

The input thresholds of 5V devices can be globally configured for either TTL (1.2 V threshold) or CMOS (2.5 V threshold), just like XC2000 and XC3000 inputs. The two global adjustments of input threshold and output level are independent of each other. The XC4000XL family has an input threshold of 1.6V, compatible with both 3.3V CMOS and TTL levels.

### *Global Signal Access to Logic*

There is additional access from global clocks to the F and G function generator inputs.

### *Configuration Pin Pull-Up Resistors*

During configuration, these pins have weak pull-up resistors. For the most popular configuration mode, Slave Serial, the mode pins can thus be left unconnected. The three mode inputs can be individually configured with or without weak pull-up or pull-down resistors. A pull-down resistor value of 4.7 kΩ is recommended.

The three mode inputs can be individually configured with or without weak pull-up or pull-down resistors after configuration.

The $\overline{\text{PROGRAM}}$ input pin has a permanent weak pull-up.

### *Soft Start-up*

Like the XC3000A, XC4000 Series devices have “Soft Start-up.” When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. This feature avoids potential ground bounce when all outputs are turned on simultaneously. Immediately after start-up, the slew rate of the individual outputs is, as in the XC4000 family, determined by the individual configuration option.

### *XC4000 and XC4000A Compatibility*

Existing XC4000 bitstreams can be used to configure an XC4000E device. XC4000A bitstreams must be recompiled for use with the XC4000E due to improved routing resources, although the devices are pin-for-pin compatible.

## Additional Improvements in XC4000X Only

### *Increased Routing*

New interconnect in the XC4000X includes twenty-two additional vertical lines in each column of CLBs and twelve new horizontal lines in each row of CLBs. The twelve “Quad Lines” in each CLB row and column include optional repowering buffers for maximum speed. Additional high-performance routing near the IOBs enhances pin flexibility.

### *Faster Input and Output*

A fast, dedicated early clock sourced by global clock buffers is available for the IOBs. To ensure synchronization with the regular global clocks, a Fast Capture latch driven by the early clock is available. The input data can be initially loaded into the Fast Capture latch with the early clock, then transferred to the input flip-flop or latch with the low-skew global clock. A programmable delay on the input can be used to avoid hold-time requirements. See “IOB Input Signals” on page 20 for more information.

### *Latch Capability in CLBs*

Storage elements in the XC4000X CLB can be configured as either flip-flops or latches. This capability makes the FPGA highly synthesis-compatible.

### *IOB Output MUX From Output Clock*

A multiplexer in the IOB allows the output clock to select either the output data or the IOB clock enable as the output to the pad. Thus, two different data signals can share a single output pad, effectively doubling the number of device outputs without requiring a larger, more expensive package. This multiplexer can also be configured as an AND-gate to implement a very fast pin-to-pin path. See “IOB Output Signals” on page 23 for more information.

### *Additional Address Bits*

Larger devices require more bits of configuration data. A daisy chain of several large XC4000X devices may require a PROM that cannot be addressed by the eighteen address bits supported in the XC4000E. The XC4000X Series therefore extends the addressing in Master Parallel configuration mode to 22 bits.

# Detailed Functional Description

XC4000 Series devices achieve high speed through advanced semiconductor technology and improved architecture. The XC4000E and XC4000X support system clock rates of up to 80 MHz and internal performance in excess of 150 MHz. Compared to older Xilinx FPGA families, XC4000 Series devices are more powerful. They offer on-chip edge-triggered and dual-port RAM, clock enables on I/O flip-flops, and wide-input decoders. They are more versatile in many applications, especially those involving RAM. Design cycles are faster due to a combination of increased routing resources and more sophisticated software.

## Basic Building Blocks

Xilinx user-programmable gate arrays include two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing the user's logic.
- IOBs provide the interface between the package pins and internal signal lines.

Three other types of circuits are also available:

- 3-State buffers (TBUFs) driving horizontal longlines are associated with each CLB.
- Wide edge decoders are available around the periphery of each device.
- An on-chip oscillator is provided.

Programmable interconnect resources provide routing paths to connect the inputs and outputs of these configurable elements to the appropriate networks.

The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA. Each of these available circuits is described in this section.

## Configurable Logic Blocks (CLBs)

Configurable Logic Blocks implement most of the logic in an FPGA. The principal CLB elements are shown in Figure 1. Two 4-input function generators (F and G) offer unrestricted versatility. Most combinatorial logic functions need four or fewer inputs. However, a third function generator (H) is provided. The H function generator has three inputs. Either zero, one, or two of these inputs can be the outputs of F and G; the other input(s) are from outside the CLB. The CLB can, therefore, implement certain functions of up to nine variables, like parity check or expandable-identity comparison of two sets of four inputs.

Each CLB contains two storage elements that can be used to store the function generator outputs. However, the storage elements and function generators can also be used independently. These storage elements can be configured as flip-flops in both XC4000E and XC4000X devices; in the XC4000X they can optionally be configured as latches. DIN can be used as a direct input to either of the two storage elements. H1 can drive the other through the H function generator. Function generator outputs can also drive two outputs independent of the storage element outputs. This versatility increases logic capacity and simplifies routing.

Thirteen CLB inputs and four CLB outputs provide access to the function generators and storage elements. These inputs and outputs connect to the programmable interconnect resources outside the block.

### *Function Generators*

Four independent inputs are provided to each of two function generators (F1 - F4 and G1 - G4). These function generators, with outputs labeled F' and G', are each capable of implementing any arbitrarily defined Boolean function of four inputs. The function generators are implemented as memory look-up tables. The propagation delay is therefore independent of the function implemented.

A third function generator, labeled H', can implement any Boolean function of its three inputs. Two of these inputs can optionally be the F' and G' functional generator outputs. Alternatively, one or both of these inputs can come from outside the CLB (H2, H0). The third input must come from outside the block (H1).

Signals from the function generators can exit the CLB on two outputs. F' or H' can be connected to the X output. G' or H' can be connected to the Y output.

A CLB can be used to implement any of the following functions:

- any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables[1]
- any single function of five variables
- any function of four variables together with some functions of six variables
- some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

1. When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.

Supported CLB memory configurations and timing modes for single- and dual-port modes are shown in Table 3.

XC4000 Series devices are the first programmable logic devices with edge-triggered (synchronous) and dual-port RAM accessible to the user. Edge-triggered RAM simplifies system timing. Dual-port RAM doubles the effective throughput of FIFO applications. These features can be individually programmed in any XC4000 Series CLB.

### Advantages of On-Chip and Edge-Triggered RAM

The on-chip RAM is extremely fast. The read access time is the same as the logic delay. The write access time is slightly slower. Both access times are much faster than any off-chip solution, because they avoid I/O delays.

Edge-triggered RAM, also called synchronous RAM, is a feature never before available in a Field Programmable Gate Array. The simplicity of designing with edge-triggered RAM, and the markedly higher achievable performance, add up to a significant improvement over existing devices with on-chip RAM.

Three application notes are available from Xilinx that discuss edge-triggered RAM: "*XC4000E Edge-Triggered and Dual-Port RAM Capability*," "*Implementing FIFOs in XC4000E RAM*," and "*Synchronous and Asynchronous FIFO Designs*." All three application notes apply to both XC4000E and XC4000X RAM.

**Table 3: Supported RAM Modes**

| | 16 x 1 | 16 x 2 | 32 x 1 | Edge-Triggered Timing | Level-Sensitive Timing |
|---|---|---|---|---|---|
| Single-Port | √ | √ | √ | √ | √ |
| Dual-Port | √ | | | √ | |

### RAM Configuration Options

The function generators in any CLB can be configured as RAM arrays in the following sizes:

- Two 16x1 RAMs: two data inputs and two data outputs with identical or, if preferred, different addressing for each RAM
- One 32x1 RAM: one data input and one data output.

One F or G function generator can be configured as a 16x1 RAM while the other function generators are used to implement any function of up to 5 inputs.

Additionally, the XC4000 Series RAM may have either of two timing modes:

- Edge-Triggered (Synchronous): data written by the designated edge of the CLB clock. WE acts as a true clock enable.
- Level-Sensitive (Asynchronous): an external WE signal acts as the write strobe.

The selected timing mode applies to both function generators within a CLB when both are configured as RAM.

The number of read ports is also programmable:

- Single Port: each function generator has a common read and write port
- Dual Port: both function generators are configured together as a single 16x1 dual-port RAM with one write port and two read ports. Simultaneous read and write operations to the same or different addresses are supported.

RAM configuration options are selected by placing the appropriate library symbol.

### Choosing a RAM Configuration Mode

The appropriate choice of RAM mode for a given design should be based on timing and resource requirements, desired functionality, and the simplicity of the design process. Recommended usage is shown in Table 4.

The difference between level-sensitive, edge-triggered, and dual-port RAM is only in the write operation. Read operation and timing is identical for all modes of operation.

**Table 4: RAM Mode Selection**

| | Level-Sensitive | Edge-Triggered | Dual-Port Edge-Triggered |
|---|---|---|---|
| Use for New Designs? | No | Yes | Yes |
| Size (16x1, Registered) | 1/2 CLB | 1/2 CLB | 1 CLB |
| Simultaneous Read/Write | No | No | Yes |
| Relative Performance | X | 2X | 2X (4X effective) |

### RAM Inputs and Outputs

The F1-F4 and G1-G4 inputs to the function generators act as address lines, selecting a particular memory cell in each look-up table.

The functionality of the CLB control signals changes when the function generators are configured as RAM. The DIN/H2, H1, and SR/H0 lines become the two data inputs (D0, D1) and the Write Enable (WE) input for the 16x2 memory. When the 32x1 configuration is selected, D1 acts as the fifth address bit and D0 is the data input.

The contents of the memory cell(s) being addressed are available at the F' and G' function-generator outputs. They can exit the CLB through its X and Y outputs, or can be captured in the CLB flip-flop(s).

Configuring the CLB function generators as Read/Write memory does not affect the functionality of the other por-

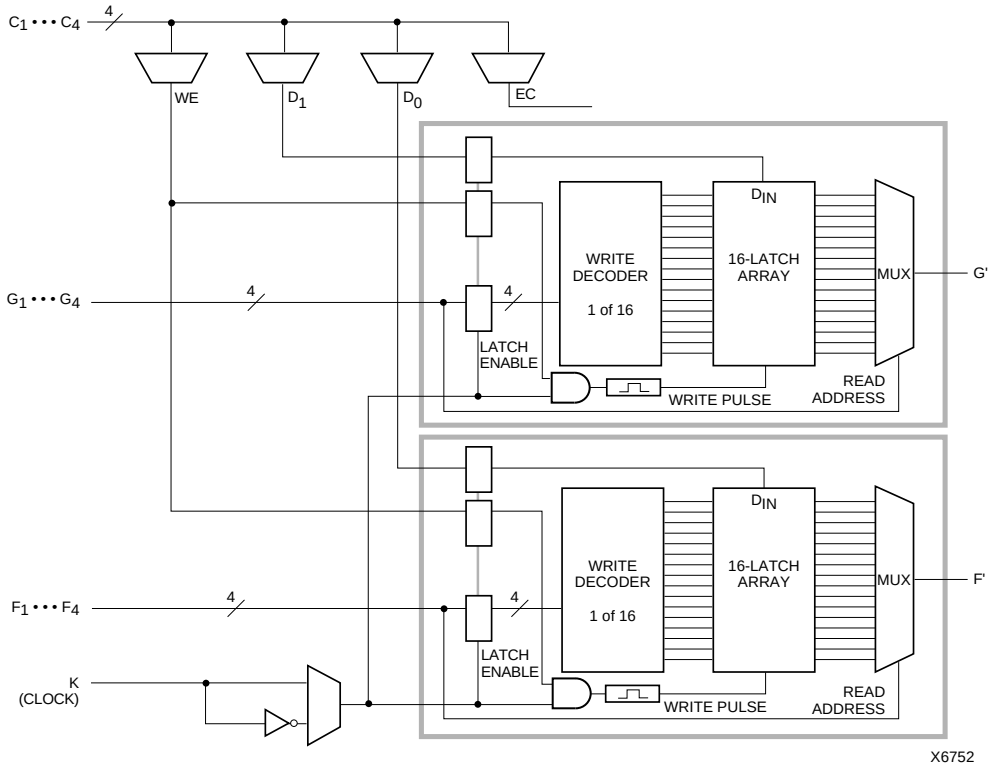



**Figure 4: 16x2 (or 16x1) Edge-Triggered Single-Port RAM**

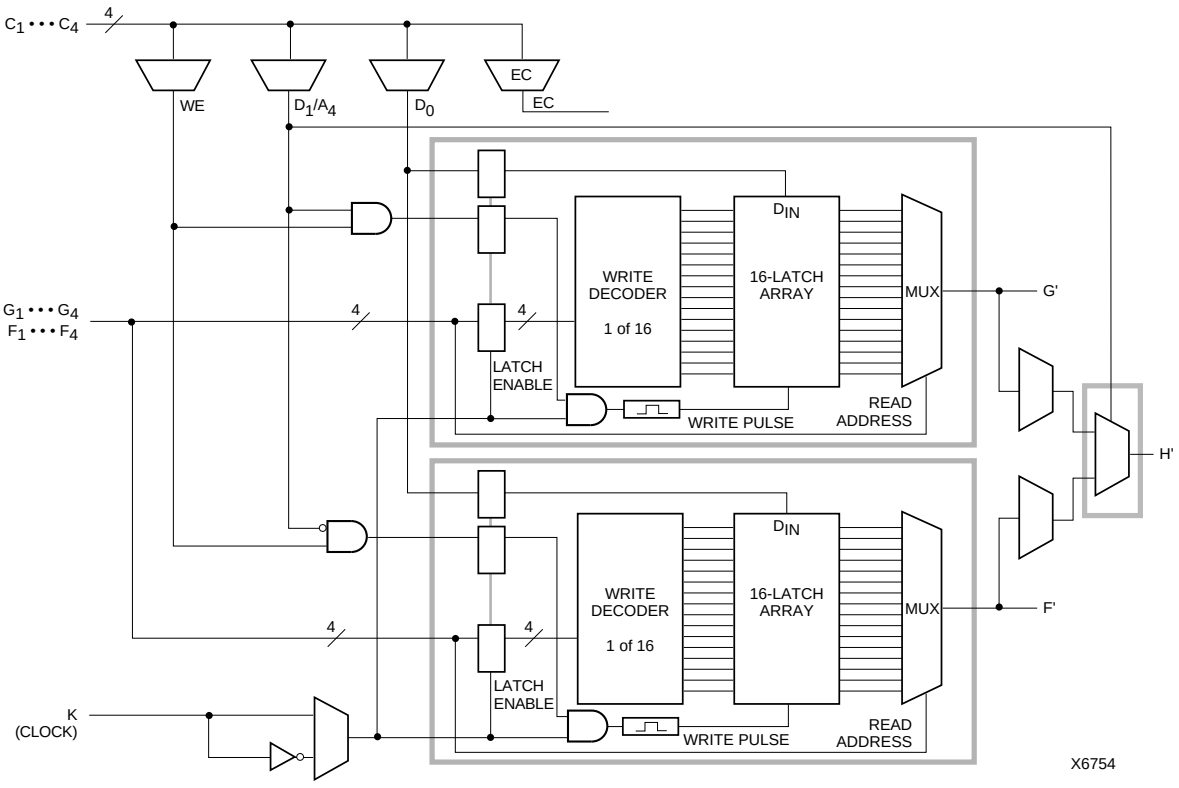



**Figure 5: 32x1 Edge-Triggered Single-Port RAM (F and G addresses are identical)**

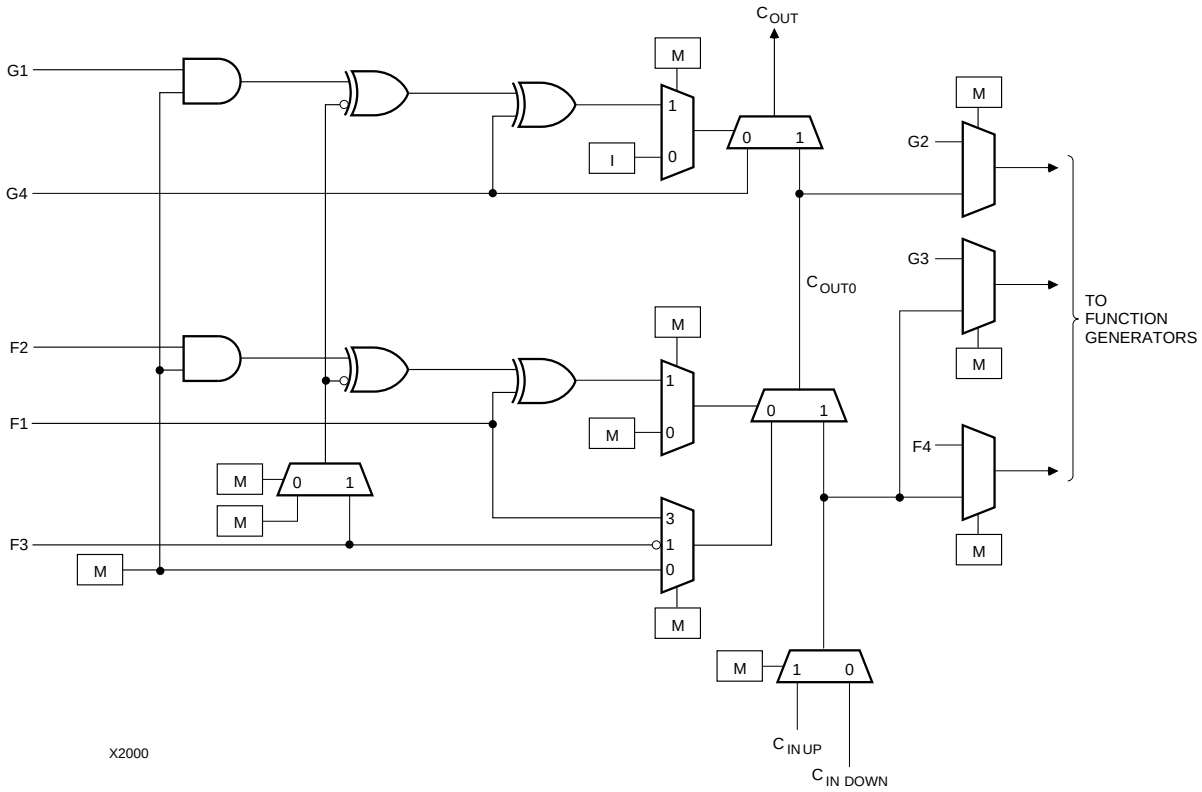



**Figure 14: Detail of XC4000E Dedicated Carry Logic**

## Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals.

Figure 15 shows a simplified block diagram of the XC4000E IOB. A more complete diagram which includes the boundary scan logic of the XC4000E IOB can be found in Figure 40 on page 43, in the “Boundary Scan” section.

The XC4000X IOB contains some special features not included in the XC4000E IOB. These features are highlighted in a simplified block diagram found in Figure 16, and discussed throughout this section. When XC4000X special features are discussed, they are clearly identified in the text. Any feature not so identified is present in both XC4000E and XC4000X devices.

### *IOB Input Signals*

Two paths, labeled I1 and I2 in Figure 15 and Figure 16, bring input signals into the array. Inputs also connect to an input register that can be programmed as either an edge-triggered flip-flop or a level-sensitive latch.

The choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are available, and some combinations of latches and flip-flops can be implemented in a single IOB, as described in the *XACT Libraries Guide*.

The XC4000E inputs can be globally configured for either TTL (1.2V) or 5.0 volt CMOS thresholds, using an option in the bitstream generation software. There is a slight input hysteresis of about 300mV. The XC4000E output levels are also configurable; the two global adjustments of input threshold and output level are independent.

Inputs on the XC4000XL are TTL compatible and 3.3V CMOS compatible. Outputs on the XC4000XL are pulled to the 3.3V positive supply.

The inputs of XC4000 Series 5-Volt devices can be driven by the outputs of any 3.3-Volt device, if the 5-Volt inputs are in TTL mode.

Supported sources for XC4000 Series device inputs are shown in Table 8.

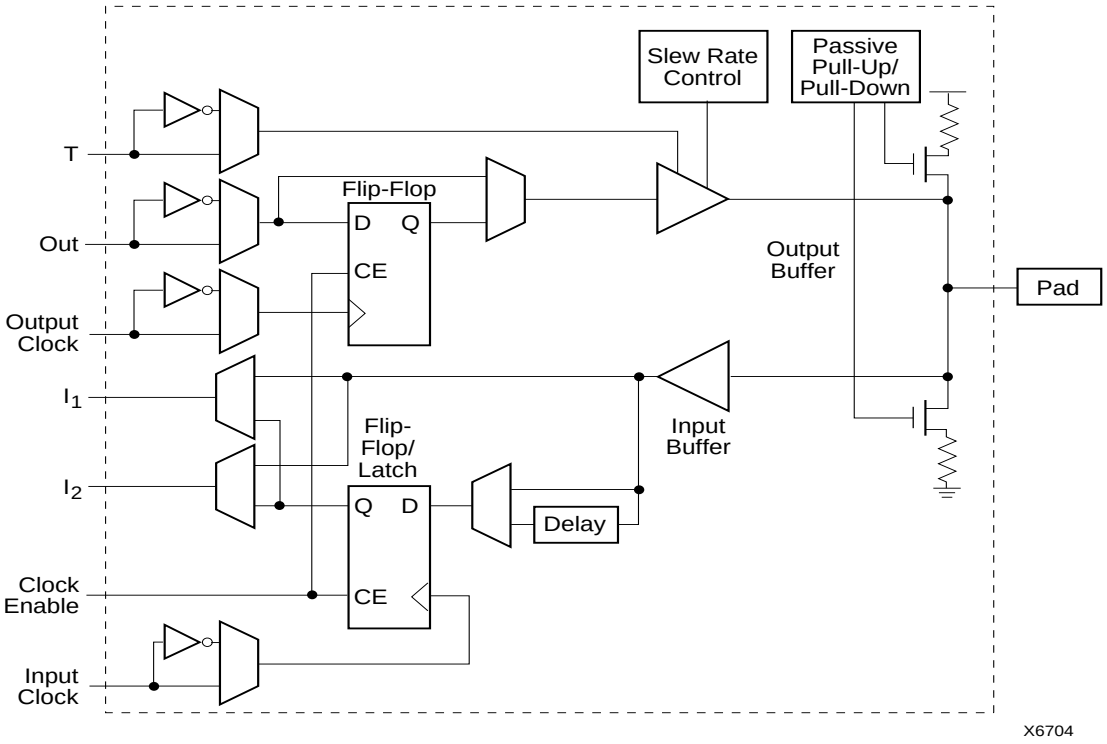



**Figure 15: Simplified Block Diagram of XC4000E IOB**

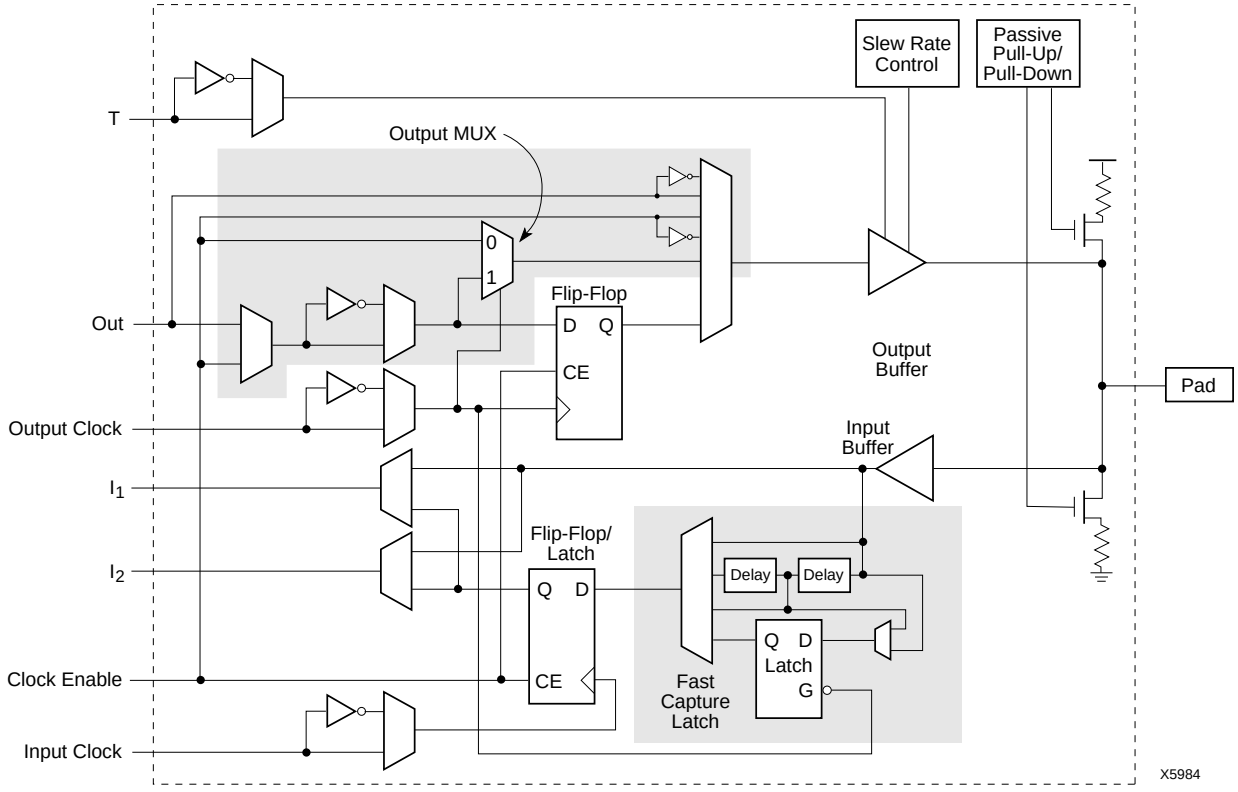



**Figure 16: Simplified Block Diagram of XC4000X IOB (shaded areas indicate differences from XC4000E)**

Any XC4000 Series 5-Volt device with its outputs configured in TTL mode can drive the inputs of any typical 3.3-Volt device. (For a detailed discussion of how to interface between 5 V and 3.3 V devices, see the 3V Products section of *The Programmable Logic Data Book*.)

Supported destinations for XC4000 Series device outputs are shown in Table 12.

An output can be configured as open-drain (open-collector) by placing an OBUFT symbol in a schematic or HDL code, then tying the 3-state pin (T) to the output signal, and the input pin (I) to Ground. (See Figure 18.)

**Table 12: Supported Destinations for XC4000 Series Outputs**

| Destination | XC4000 Series Outputs | | |
|---|---|---|---|
| | 3.3 V, CMOS | 5 V, TTL | 5 V, CMOS |
| Any typical device, Vcc = 3.3 V, CMOS-threshold inputs | √ | √ | some[1] |
| Any device, Vcc = 5 V, TTL-threshold inputs | √ | √ | √ |
| Any device, Vcc = 5 V, CMOS-threshold inputs | **Unreliable Data** | | √ |

1. Only if destination device has 5-V tolerant inputs

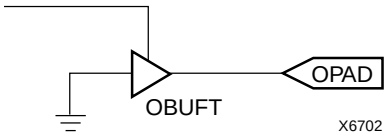



**Figure 18: Open-Drain Output**

### Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop.

For XC4000E devices, maximum total capacitive load for simultaneous fast mode switching in the same direction is 200 pF for all package pins between each Power/Ground pin pair. For XC4000X devices, additional internal Power/Ground pin pairs are connected to special Power and Ground planes within the packages, to reduce ground bounce. Therefore, the maximum total capacitive load is 300 pF between each external Power/Ground pin pair. Maximum loading may vary for the low-voltage devices.

For slew-rate limited outputs this total is two times larger for each device type: 400 pF for XC4000E devices and 600 pF for XC4000X devices. This maximum capacitive load should not be exceeded, as it can result in ground bounce of greater than 1.5 V amplitude and more than 5 ns duration. This level of ground bounce may cause undesired transient behavior on an output, or in the internal logic. This restriction is common to all high-speed digital ICs, and is not particular to Xilinx or the XC4000 Series.

XC4000 Series devices have a feature called “Soft Start-up,” designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

### Global Three-State

A separate Global 3-State line (not shown in Figure 15 or Figure 16) forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. This global net (GTS) does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-State signal. Using GTS is similar to GSR. See Figure 2 on page 11 for details.

Alternatively, GTS can be driven from any internal node.

or clear on reset and after configuration. Other than the global GSR net, no user-controlled set/reset signal is available to the I/O flip-flops. The choice of set or clear applies to both the initial state of the flip-flop and the response to the Global Set/Reset pulse. See "Global Set/Reset" on page 11 for a description of how to use GSR.

### JTAG Support

Embedded logic attached to the IOBs contains test structures compatible with IEEE Standard 1149.1 for boundary scan testing, permitting easy chip and board-level testing. More information is provided in "Boundary Scan" on page 42.

## Three-State Buffers

A pair of 3-state buffers is associated with each CLB in the array. (See Figure 27 on page 30.) These 3-state buffers can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal longlines, saving logic resources. Programmable pull-up resistors attached to these longlines help to implement a wide wired-AND function.

The buffer enable is an active-High 3-state (i.e. an active-Low enable), as shown in Table 13.

Another 3-state buffer with similar access is located near each I/O block along the right and left edges of the array. (See Figure 33 on page 34.)

The horizontal longlines driven by the 3-state buffers have a weak keeper at each end. This circuit prevents undefined floating levels. However, it is overridden by any driver, even a pull-up resistor.

Special longlines running along the perimeter of the array can be used to wire-AND signals coming from nearby IOBs or from internal longlines. These longlines form the wide edge decoders discussed in "Wide Edge Decoders" on page 27.

### *Three-State Buffer Modes*

The 3-state buffers can be configured in three modes:

- Standard 3-state buffer
- Wired-AND with input on the I pin
- Wired OR-AND

#### Standard 3-State Buffer

All three pins are used. Place the library element BUFT. Connect the input to the I pin and the output to the O pin. The T pin is an active-High 3-state (i.e. an active-Low enable). Tie the T pin to Ground to implement a standard buffer.

#### Wired-AND with Input on the I Pin

The buffer can be used as a Wired-AND. Use the WAND1 library symbol, which is essentially an open-drain buffer. WAND4, WAND8, and WAND16 are also available. See the *XACT Libraries Guide* for further information.

The T pin is internally tied to the I pin. Connect the input to the I pin and the output to the O pin. Connect the outputs of all the WAND1s together and attach a PULLUP symbol.

#### Wired OR-AND

The buffer can be configured as a Wired OR-AND. A High level on either input turns off the output. Use the WOR2AND library symbol, which is essentially an open-drain 2-input OR gate. The two input pins are functionally equivalent. Attach the two inputs to the I0 and I1 pins and tie the output to the O pin. Tie the outputs of all the WOR2ANDs together and attach a PULLUP symbol.

### *Three-State Buffer Examples*

Figure 21 shows how to use the 3-state buffers to implement a wired-AND function. When all the buffer inputs are High, the pull-up resistor(s) provide the High output.

Figure 22 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active-High 3-state (T) is identical to an active-Low output enable, as shown in Table 13.

**Table 13: Three-State Buffer Functionality**

| IN | T | OUT |
|---|---|---|
| X | 1 | Z |
| IN | 0 | IN |

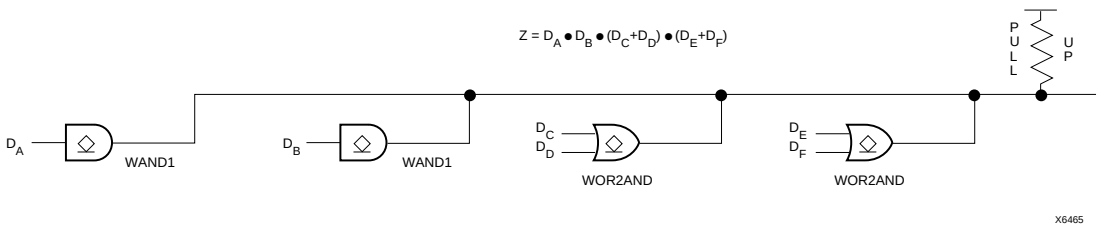



**Figure 21: Open-Drain Buffers Implement a Wired-AND Function**

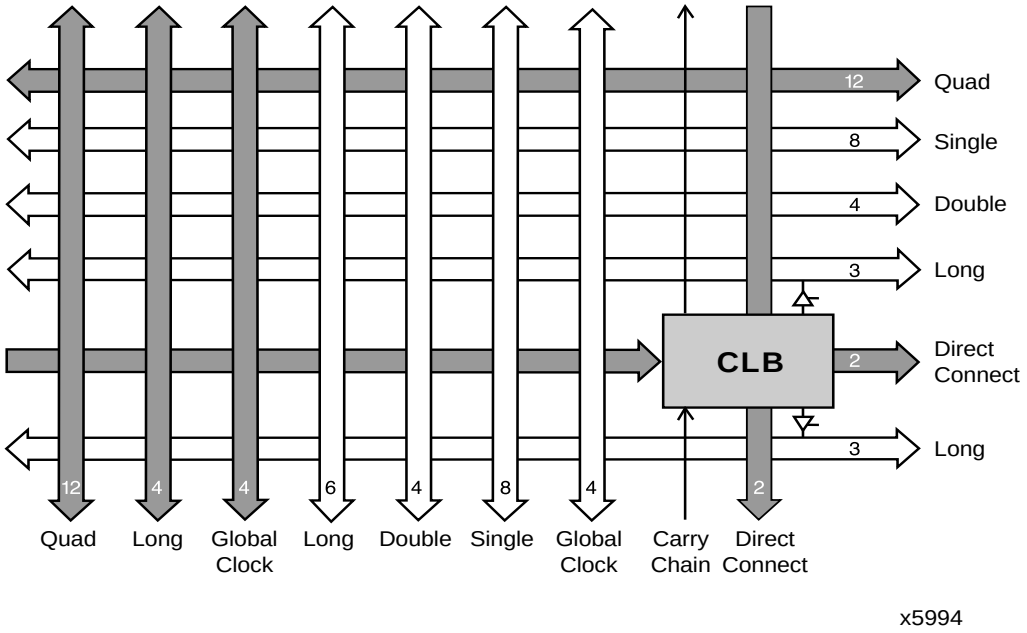



**Figure 25: High-Level Routing Diagram of XC4000 Series CLB (shaded arrows indicate XC4000X only)**



**Table 14: Routing per CLB in XC4000 Series Devices**

| | XC4000E | | XC4000X | |
|---|---|---|---|---|
| | Vertical | Horizontal | Vertical | Horizontal |
| Singles | 8 | 8 | 8 | 8 |
| Doubles | 4 | 4 | 4 | 4 |
| Quads | 0 | 0 | 12 | 12 |
| Longlines | 6 | 6 | 10 | 6 |
| Direct Connects | 0 | 0 | 2 | 2 |
| Globals | 4 | 0 | 8 | 0 |
| Carry Logic | 2 | 0 | 1 | 0 |
| Total | 24 | 18 | 45 | 32 |

### *Programmable Switch Matrices*

The horizontal and vertical single- and double-length lines intersect at a box called a programmable switch matrix (PSM). Each switch matrix consists of programmable pass transistors used to establish connections between the lines (see Figure 26).

For example, a single-length signal entering on the right side of the switch matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Similarly, a double-length signal can be routed to a double-length line on any or all of the other three edges of the programmable switch matrix.

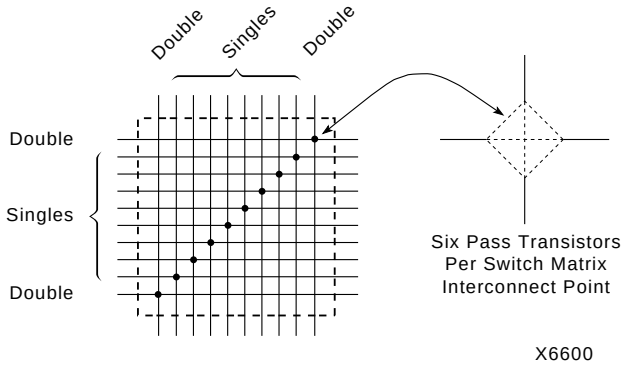



**Figure 26: Programmable Switch Matrix (PSM)**

### *Single-Length Lines*

Single-length lines provide the greatest interconnect flexibility and offer fast routing between adjacent blocks. There are eight vertical and eight horizontal single-length lines associated with each CLB. These lines connect the switching matrices that are located in every row and a column of CLBs.

Single-length lines are connected by way of the programmable switch matrices, as shown in Figure 28. Routing connectivity is shown in Figure 27.

Single-length lines incur a delay whenever they go through a switching matrix. Therefore, they are not suitable for routing signals for long distances. They are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.

circuit prevents undefined floating levels. However, it is overridden by any driver, even a pull-up resistor.

Each XC4000E longline has a programmable splitter switch at its center, as does each XC4000X longline driven by TBUFs. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Each XC4000X longline not driven by TBUFs has a buffered programmable splitter switch at the 1/4, 1/2, and 3/4 points of the array. Due to the buffering, XC4000X longline performance does not deteriorate with the larger array sizes. If the longline is split, the resulting partial longlines are independent.

Routing connectivity of the longlines is shown in Figure 27 on page 30.

### *Direct Interconnect (XC4000X only)*

The XC4000X offers two direct, efficient and fast connections between adjacent CLBs. These nets facilitate a data flow from the left to the right side of the device, or from the top to the bottom, as shown in Figure 30. Signals routed on the direct interconnect exhibit minimum interconnect propagation delay and use no general routing resources.

The direct interconnect is also present between CLBs and adjacent IOBs. Each IOB on the left and top device edges has a direct path to the nearest CLB. Each CLB on the right and bottom edges of the array has a direct path to the nearest two IOBs, since there are two IOBs for each row or column of CLBs.

The place and route software uses direct interconnect whenever possible, to maximize routing resources and minimize interconnect delays.

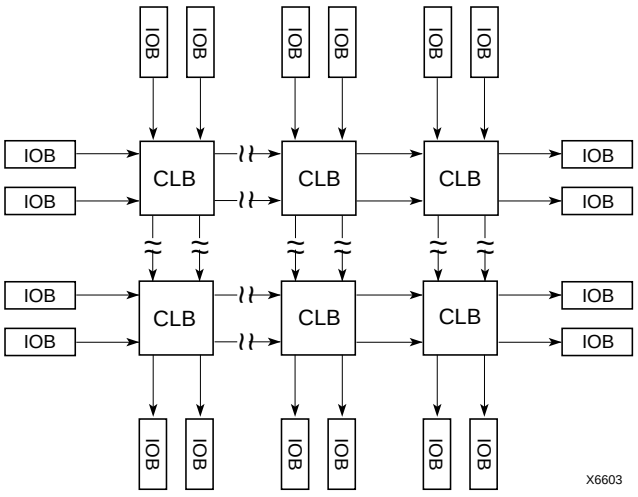



**Figure 30: XC4000X Direct Interconnect**

## I/O Routing

XC4000 Series devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines spanning two CLBs (four IOBs), and four longlines. Global lines and Wide Edge Decoder lines are provided. XC4000X devices also include eight octal lines.

A high-level diagram of the VersaRing is shown in Figure 31. The shaded arrows represent routing present only in XC4000X devices.

Figure 33 on page 34 is a detailed diagram of the XC4000E and XC4000X VersaRing. The area shown includes two IOBs. There are two IOBs per CLB row or column, therefore this diagram corresponds to the CLB routing diagram shown in Figure 27 on page 30. The shaded areas represent routing and routing connections present only in XC4000X devices.

### *Octal I/O Routing (XC4000X only)*

Between the XC4000X CLB array and the pad ring, eight interconnect tracks provide for versatility in pin assignment and fixed pinout flexibility. (See Figure 32 on page 33.)

These routing tracks are called octals, because they can be broken every eight CLBs (sixteen IOBs) by a programmable buffer that also functions as a splitter switch. The buffers are staggered, so each line goes through a buffer at every eighth CLB location around the device edge.

The octal lines bend around the corners of the device. The lines cross at the corners in such a way that the segment most recently buffered before the turn has the farthest distance to travel before the next buffer, as shown in Figure 32.

The top and bottom Global Early buffers are about 1 ns slower clock to out than the left and right Global Early buffers.

The Global Early buffers can be driven by either semi-dedicated pads or internal logic. They share pads with the Global Low-Skew buffers, so a single net can drive both global buffers, as described above.

To use a Global Early buffer, place a BUFGE element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=T attribute or property to direct that a BUFGE be placed in one of the two Global Early buffers on the top edge of the device, or a LOC=TR to indicate the Global Early buffer on the top edge of the device, on the right.

## Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated Vcc and Ground ring surrounding the logic array provides power to the I/O drivers, as shown in Figure 39. An independent matrix of Vcc and Ground lines supplies the interior logic of the device.

This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately de-coupled. Typically, a 0.1 µF capacitor connected between each Vcc pin and the board's Ground plane will provide adequate de-coupling.

Output buffers capable of driving/sinking the specified 12 mA loads under specified worst-case conditions may be capable of driving/sinking up to 10 times as much current under best case conditions.

Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the Ground pads. The I/O Block output buffers have a slew-rate limited mode (default) which should be used where output rise and fall times are not speed-critical.

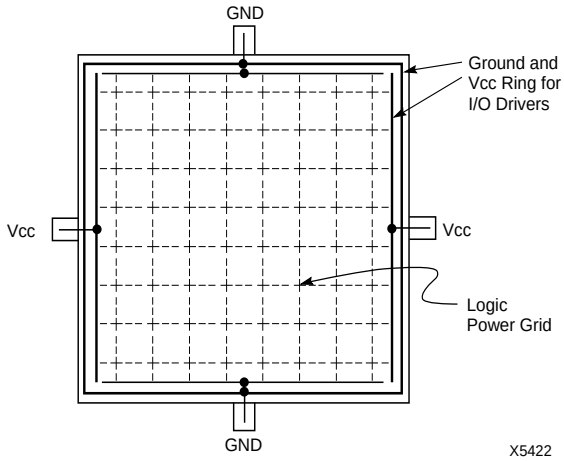



**Figure 39: XC4000 Series Power Distribution**

## Pin Descriptions

There are three types of pins in the XC4000 Series devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with a 50 kΩ - 100 kΩ pull-up resistor.

After configuration, if an IOB is unused it is configured as an input with a 50 kΩ - 100 kΩ pull-up resistor.

XC4000 Series devices have no dedicated Reset input. Any user I/O can be configured to drive the Global Set/Reset net, GSR. See "Global Set/Reset" on page 11 for more information on GSR.

XC4000 Series devices have no Powerdown control input, as the XC3000 and XC2000 families do. The XC3000/XC2000 Powerdown control also 3-stated all of the device
I/O pins. For XC4000 Series devices, use the global 3-state net, GTS, instead. This net 3-states all outputs, but does not place the device in low-power mode. See "IOB Output Signals" on page 23 for more information on GTS.

Device pins for XC4000 Series devices are described in Table 16. Pin functions during configuration for each of the seven configuration modes are summarized in Table 22 on page 58, in the "Configuration Timing" section.

**Table 20: XC4000E Program Data**

| Device | XC4003E | XC4005E | XC4006E | XC4008E | XC4010E | XC4013E | XC4020E | XC4025E |
|---|---|---|---|---|---|---|---|---|
| **Max Logic Gates** | 3,000 | 5,000 | 6,000 | 8,000 | 10,000 | 13,000 | 20,000 | 25,000 |
| **CLBs (Row x Col.)** | 100 (10 x 10) | 196 (14 x 14) | 256 (16 x 16) | 324 (18 x 18) | 400 (20 x 20) | 576 (24 x 24) | 784 (28 x 28) | 1,024 (32 x 32) |
| **IOBs** | 80 | 112 | 128 | 144 | 160 | 192 | 224 | 256 |
| **Flip-Flops** | 360 | 616 | 768 | 936 | 1,120 | 1,536 | 2,016 | 2,560 |
| **Bits per Frame** | 126 | 166 | 186 | 206 | 226 | 266 | 306 | 346 |
| **Frames** | 428 | 572 | 644 | 716 | 788 | 932 | 1,076 | 1,220 |
| **Program Data** | 53,936 | 94,960 | 119,792 | 147,504 | 178,096 | 247,920 | 329,264 | 422,128 |
| **PROM Size (bits)** | 53,984 | 95,008 | 119,840 | 147,552 | 178,144 | 247,968 | 329,312 | 422,176 |

Notes: 1. Bits per Frame = (10 x number of rows) + 7 for the top + 13 for the bottom + 1 + 1 start bit + 4 error check bits
Number of Frames = (36 x number of columns) + 26 for the left edge + 41 for the right edge + 1
Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits
PROM Size = Program Data + 40 (header) + 8
2. The user can add more “one” bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra “one” bits, even for extra leading ones at the beginning of the header.

**Table 21: XC4000EX/XL Program Data**

| Device | XC4002XL | XC4005 | XC4010 | XC4013 | XC4020 | XC4028 | XC4036 | XC4044 | XC4052 | XC4062 | XC4085 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Max Logic Gates** | 2,000 | 5,000 | 10,000 | 13,000 | 20,000 | 28,000 | 36,000 | 44,000 | 52,000 | 62,000 | 85,000 |
| **CLBs (Row x Column)** | 64 (8 x 8) | 196 (14 x 14) | 400 (20 x 20) | 576 (24 x 24) | 784 (28 x 28) | 1,024 (32 x 32) | 1,296 (36 x 36) | 1,600 (40 x 40) | 1,936 (44 x 44) | 2,304 (48 x 48) | 3,136 (56 x 56) |
| **IOBs** | 64 | 112 | 160 | 192 | 224 | 256 | 288 | 320 | 352 | 384 | 448 |
| **Flip-Flops** | 256 | 616 | 1,120 | 1,536 | 2,016 | 2,560 | 3,168 | 3,840 | 4,576 | 5,376 | 7,168 |
| **Bits per Frame** | 133 | 205 | 277 | 325 | 373 | 421 | 469 | 517 | 565 | 613 | 709 |
| **Frames** | 459 | 741 | 1,023 | 1,211 | 1,399 | 1,587 | 1,775 | 1,963 | 2,151 | 2,339 | 2,715 |
| **Program Data** | 61,052 | 151,910 | 283,376 | 393,580 | 521,832 | 668,124 | 832,480 | 1,014,876 | 1,215,320 | 1,433,804 | 1,924,940 |
| **PROM Size (bits)** | 61,104 | 151,960 | 283,424 | 393,632 | 521,880 | 668,172 | 832,528 | 1,014,924 | 1,215,368 | 1,433,852 | 1,924,992 |

Notes: 1. Bits per frame = (13 x number of rows) + 9 for the top + 17 for the bottom + 8 + 1 start bit + 4 error check bits.
Frames = (47 x number of columns) + 27 for the left edge + 52 for the right edge + 4.
Program data = (bits per frame x number of frames) + 5 postamble bits.
PROM size = (program data + 40 header bits + 8 start bits) rounded up to the nearest byte.
2. The user can add more “one” bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value must be adjusted for all such extra “one” bits, even for extra leading “ones” at the beginning of the header.

## Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 19. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the $\overline{\text{INIT}}$ pin Low and goes into a Wait state.

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in Figure 45. The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback data is independent of the current device state. CLB outputs should not be included (Read Capture option not

used), and if RAM is present, the RAM content must be unchanged.

Statistically, one error out of 2048 might go undetected.

## Configuration Sequence

There are four major steps in the XC4000 Series power-up configuration sequence.

- Configuration Memory Clear
- Initialization
- Configuration
- Start-Up

The full process is illustrated in Figure 46.

### *Configuration Memory Clear*

When power is first applied or is reapplied to an FPGA, an internal circuit forces initialization of the configuration logic. When Vcc reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a time delay is started. This time delay is nominally 16 ms, and up to 10% longer in the low-voltage devices. The delay is four times as long when in Master Modes (M0 Low), to allow ample time for all slaves to reach a stable Vcc. When all $\overline{INIT}$ pins are tied together, as recommended, the longest delay takes precedence. Therefore, devices with different time delays can easily be mixed and matched in a daisy chain.

This delay is applied only on power-up. It is not applied when re-configuring an FPGA by pulsing the $\overline{PROGRAM}$ pin

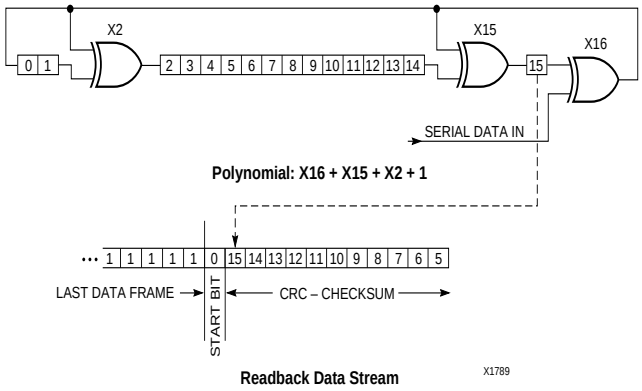



**Figure 45: Circuit for Generating CRC-16**

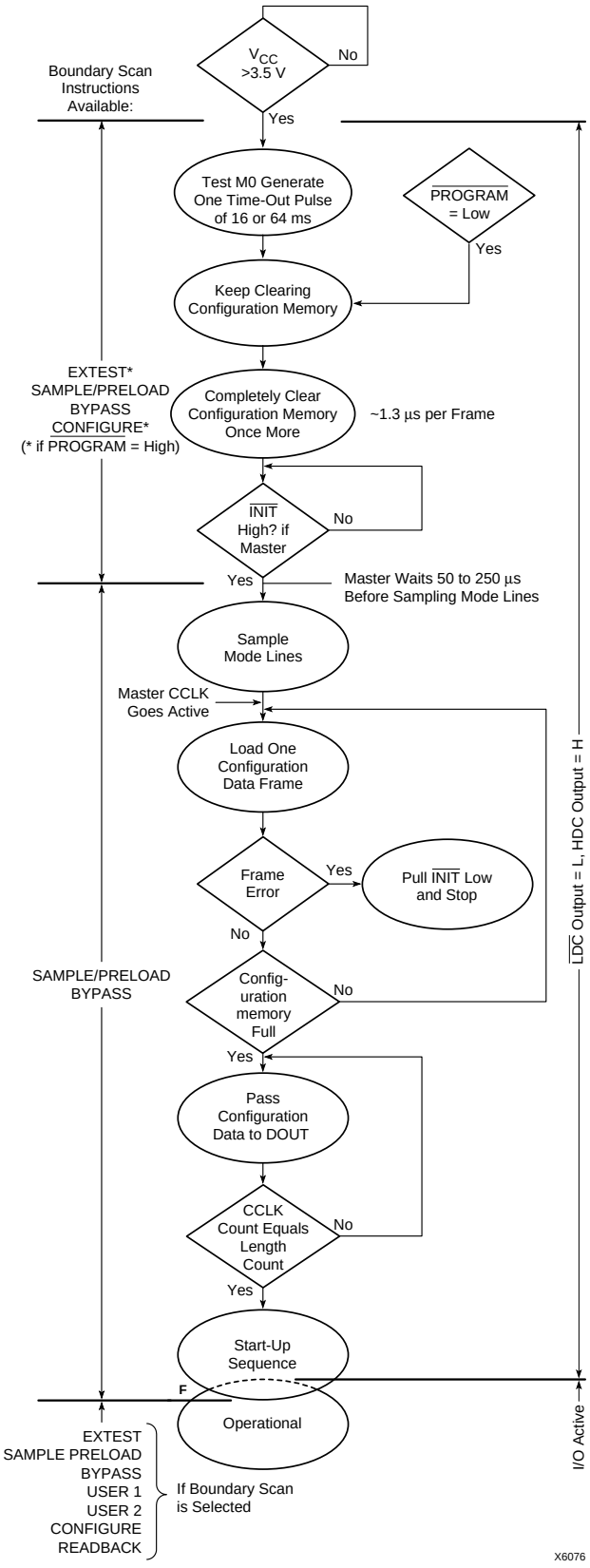



**Figure 46: Power-up Configuration Sequence**

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. Reset/Set is then released another clock period later to make sure that user-operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in Figure 47, but the designer can modify it to meet particular requirements.

Normally, the start-up sequence is controlled by the internal device oscillator output (CCLK), which is asynchronous to the system clock.

XC4000 Series offers another start-up clocking option, UCLK_NOSYNC. The three events described above need not be triggered by CCLK. They can, as a configuration option, be triggered by a user clock. This means that the device can wake up in synchronism with the user system.

When the UCLK_SYNC option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the start-up sequence until DONE is released and has gone High. This option can be used to force synchronization of several FPGAs to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

If either of these two options is selected, and no user clock is specified in the design or attached to the device, the chip could reach a point where the configuration of the device is complete and the Done pin is asserted, but the outputs do not become active. The solution is either to recreate the bitstream specifying the start-up clock as CCLK, or to supply the appropriate user clock.

### Start-up Sequence

The Start-up sequence begins when the configuration memory is full, and the total number of configuration clocks received since $\overline{\text{INIT}}$ went High equals the loaded value of the length count.

The next rising clock edge sets a flip-flop Q0, shown in Figure 48. Q0 is the leading bit of a 5-bit shift register. The outputs of this register can be programmed to control three events.

- The release of the open-drain DONE output
- The change of configuration-related pins to the user function, activating all IOBs.
- The termination of the global Set/Reset initialization of all CLB and IOB storage elements.

The DONE pin can also be wire-ANDed with DONE pins of other FPGAs or with other external signals, and can then be used as input to bit Q3 of the start-up register. This is called “Start-up Timing Synchronous to Done In” and is selected by either CCLK_SYNC or UCLK_SYNC.

When DONE is not used as an input, the operation is called “Start-up Timing Not Synchronous to DONE In,” and is selected by either CCLK_NOSYNC or UCLK_NOSYNC.

As a configuration option, the start-up control register beyond Q0 can be clocked either by subsequent CCLK pulses or from an on-chip user net called STARTUP.CLK. These signals can be accessed by placing the STARTUP library symbol.

### Start-up from CCLK

If CCLK is used to drive the start-up, Q0 through Q3 provide the timing. Heavy lines in Figure 47 show the default timing, which is compatible with XC2000 and XC3000 devices using early DONE and late Reset. The thin lines indicate all other possible timing options.

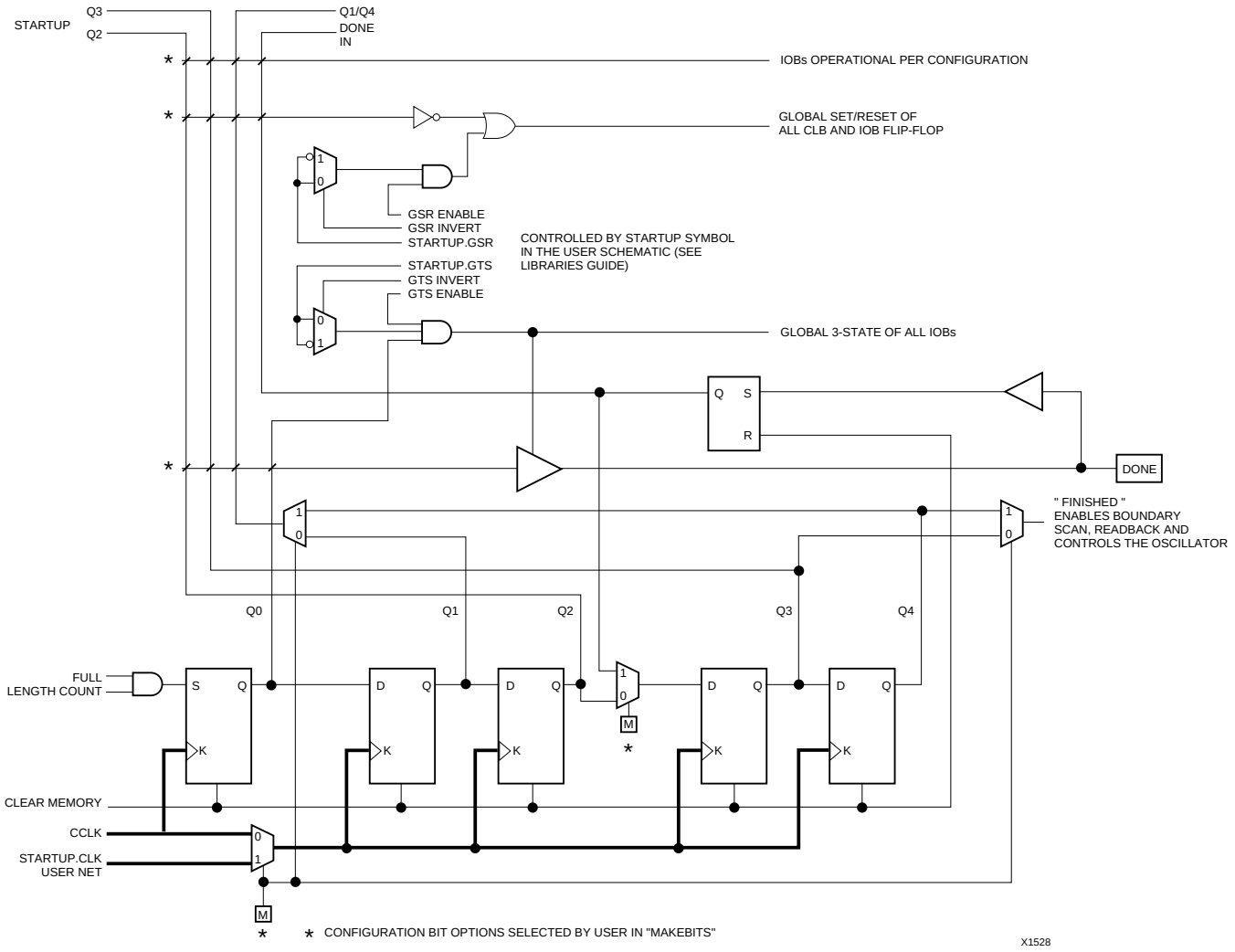



**Figure 48: Start-up Logic**

## Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Note that in XC4000 Series devices, configuration data is *not* inverted with respect to configuration as it is in XC2000 and XC3000 families.

XC4000 Series Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, place the READBACK library symbol and attach the appropriate pad symbols, as shown in Figure 49.

After Readback has been initiated by a High level on RDBK.TRIG after configuration, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

**Table 22: Pin Functions During Configuration**

| CONFIGURATION MODE <M2:M1:M0> | | | | | | |
|---|---|---|---|---|---|---|
| **SLAVE SERIAL <1:1:1>** | **MASTER SERIAL <0:0:0>** | **SYNCH. PERIPHERAL <0:1:1>** | **ASYNCH. PERIPHERAL <1:0:1>** | **MASTER PARALLEL DOWN <1:1:0>** | **MASTER PARALLEL UP <1:0:0>** | **USER OPERATION** |
| M2(HIGH) (I) | M2(LOW) (I) | M2(LOW) (I) | M2(HIGH) (I) | M2(HIGH) (I) | M2(HIGH) (I) | (I) |
| M1(HIGH) (I) | M1(LOW) (I) | M1(HIGH) (I) | M1(LOW) (I) | M1(HIGH) (I) | M1(LOW) (I) | (O) |
| M0(HIGH) (I) | M0(LOW) (I) | M0(HIGH) (I) | M0(HIGH) (I) | M0(LOW) (I) | M0(LOW) (I) | (I) |
| HDC (HIGH) | HDC (HIGH) | HDC (HIGH) | HDC (HIGH) | HDC (HIGH) | HDC (HIGH) | I/O |
| $\overline{\text{LDC}}$ (LOW) | $\overline{\text{LDC}}$ (LOW) | $\overline{\text{LDC}}$ (LOW) | $\overline{\text{LDC}}$ (LOW) | $\overline{\text{LDC}}$ (LOW) | $\overline{\text{LDC}}$ (LOW) | I/O |
| $\overline{\text{INIT}}$ | $\overline{\text{INIT}}$ | $\overline{\text{INIT}}$ | $\overline{\text{INIT}}$ | $\overline{\text{INIT}}$ | $\overline{\text{INIT}}$ | I/O |
| DONE | DONE | DONE | DONE | DONE | DONE | DONE |
| $\overline{\text{PROGRAM}}$ (I) | $\overline{\text{PROGRAM}}$ (I) | $\overline{\text{PROGRAM}}$ (I) | $\overline{\text{PROGRAM}}$ (I) | $\overline{\text{PROGRAM}}$ (I) | $\overline{\text{PROGRAM}}$ (I) | $\overline{\text{PROGRAM}}$ |
| CCLK (I) | CCLK (O) | CCLK (I) | CCLK (O) | CCLK (O) | CCLK (O) | CCLK (I) |
| | | RDY/$\overline{\text{BUSY}}$ (O) | RDY/$\overline{\text{BUSY}}$ (O) | $\overline{\text{RCLK}}$ (O) | $\overline{\text{RCLK}}$ (O) | I/O |
| | | | $\overline{\text{RS}}$ (I) | | | I/O |
| | | | $\overline{\text{CS0}}$ (I) | | | I/O |
| | | DATA 7 (I) | DATA 7 (I) | DATA 7 (I) | DATA 7 (I) | I/O |
| | | DATA 6 (I) | DATA 6 (I) | DATA 6 (I) | DATA 6 (I) | I/O |
| | | DATA 5 (I) | DATA 5 (I) | DATA 5 (I) | DATA 5 (I) | I/O |
| | | DATA 4 (I) | DATA 4 (I) | DATA 4 (I) | DATA 4 (I) | I/O |
| | | DATA 3 (I) | DATA 3 (I) | DATA 3 (I) | DATA 3 (I) | I/O |
| | | DATA 2 (I) | DATA 2 (I) | DATA 2 (I) | DATA 2 (I) | I/O |
| | | DATA 1 (I) | DATA 1 (I) | DATA 1 (I) | DATA 1 (I) | I/O |
| DIN (I) | DIN (I) | DATA 0 (I) | DATA 0 (I) | DATA 0 (I) | DATA 0 (I) | I/O |
| DOUT | DOUT | DOUT | DOUT | DOUT | DOUT | SGCK4-GCK6-I/O |
| TDI | TDI | TDI | TDI | TDI | TDI | TDI-I/O |
| TCK | TCK | TCK | TCK | TCK | TCK | TCK-I/O |
| TMS | TMS | TMS | TMS | TMS | TMS | TMS-I/O |
| TDO | TDO | TDO | TDO | TDO | TDO | TDO-(O) |
| | | | $\overline{\text{WS}}$ (I) | A0 | A0 | I/O |
| | | | | A1 | A1 | PGCK4-GCK7-I/O |
| | | | CS1 | A2 | A2 | I/O |
| | | | | A3 | A3 | I/O |
| | | | | A4 | A4 | I/O |
| | | | | A5 | A5 | I/O |
| | | | | A6 | A6 | I/O |
| | | | | A7 | A7 | I/O |
| | | | | A8 | A8 | I/O |
| | | | | A9 | A9 | I/O |
| | | | | A10 | A10 | I/O |
| | | | | A11 | A11 | I/O |
| | | | | A12 | A12 | I/O |
| | | | | A13 | A13 | I/O |
| | | | | A14 | A14 | I/O |
| | | | | A15 | A15 | SGCK1-GCK8-I/O |
| | | | | A16 | A16 | PGCK1-GCK1-I/O |
| | | | | A17 | A17 | I/O |
| | | | | A18* | A18* | I/O |
| | | | | A19* | A19* | I/O |
| | | | | A20* | A20* | I/O |
| | | | | A21* | A21* | I/O |
| | | | | | | ALL OTHERS |

## Configuration Timing

The seven configuration modes are discussed in detail in this section. Timing specifications are included.

### Slave Serial Mode

In Slave Serial mode, an external signal drives the CCLK input of the FPGA. The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

Figure 51 shows a full master/slave system. An XC4000 Series device in Slave Serial mode should be connected as shown in the third device from the left.

Slave Serial mode is selected by a <111> on the mode pins (M2, M1, M0). Slave Serial is the default mode if the mode pins are left unconnected, as they have weak pull-up resistors during configuration.

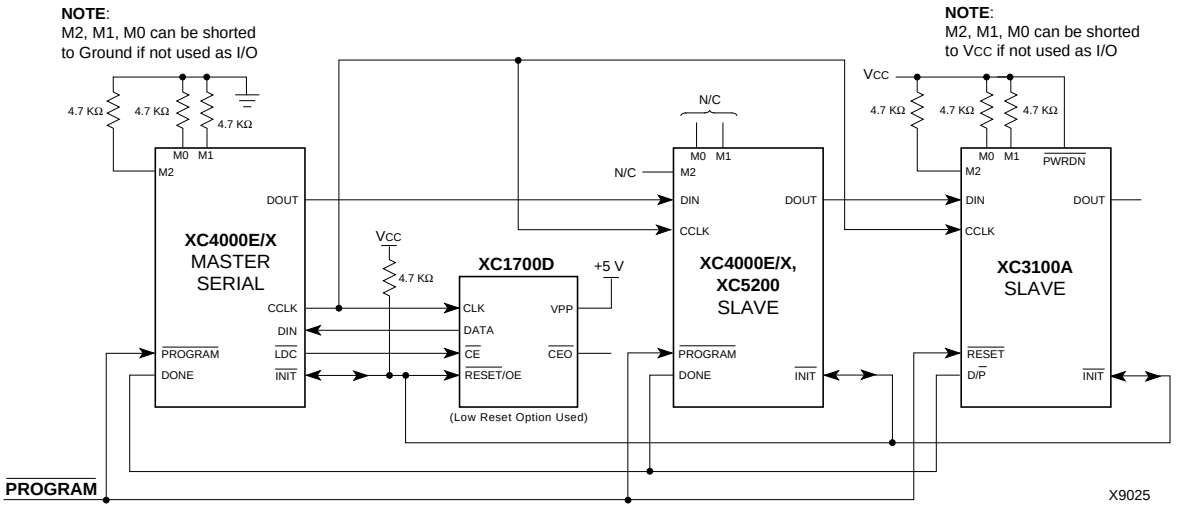
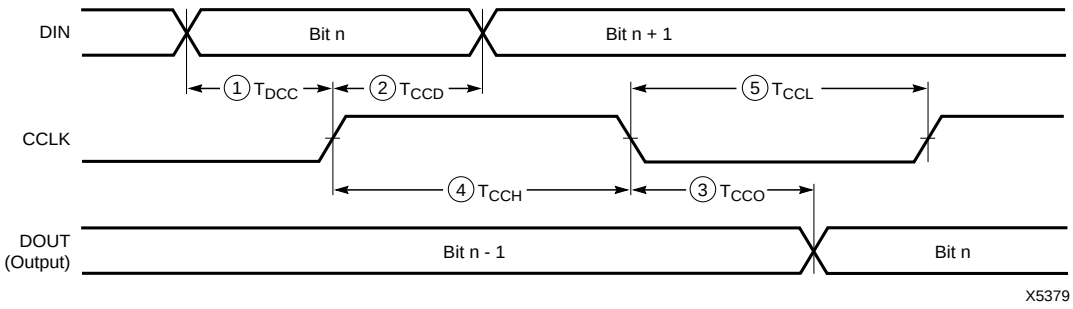



**Figure 51: Master/Slave Serial Mode Circuit Diagram**




| | Description | Symbol | | Min | Max | Units |
|---|---|---|---|---|---|---|
| CCLK | DIN setup | 1 | $T_{DCC}$ | 20 | | ns |
| | DIN hold | 2 | $T_{CCD}$ | 0 | | ns |
| | DIN to DOUT | 3 | $T_{CCO}$ | | 30 | ns |
| | High time | 4 | $T_{CCH}$ | 45 | | ns |
| | Low time | 5 | $T_{CCL}$ | 45 | | ns |
| | Frequency | | $F_{CC}$ | | 10 | MHz |

Note: Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.

**Figure 52: Slave Serial Mode Programming Switching Characteristics**

## Master Serial Mode

In Master Serial mode, the CCLK output of the lead FPGA drives a Xilinx Serial PROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

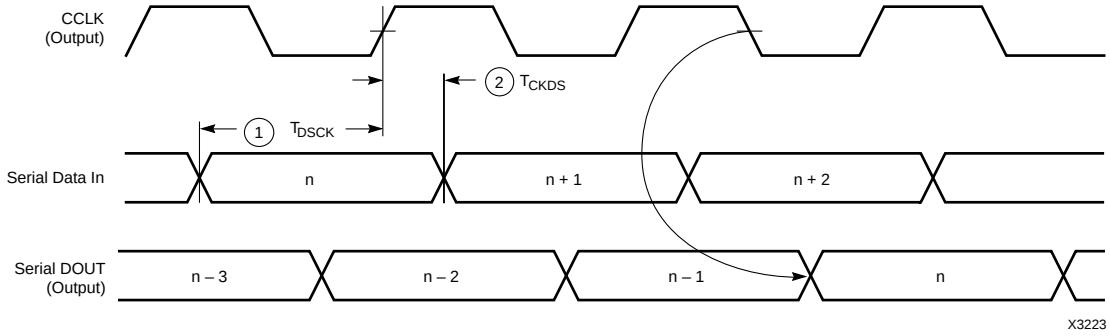
The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In the bitstream generation software, the user can specify Fast ConfigRate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. For actual timing values please refer to "Configuration Switching Characteristics" on page 68. Be sure that the serial PROM and slaves are fast enough to support this data rate. XC2000, XC3000/A, and XC3100A devices do not support the Fast ConfigRate option.

The SPROM CE input can be driven from either $\overline{LDC}$ or DONE. Using $\overline{LDC}$ avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but $\overline{LDC}$ is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the early DONE option is invoked.

Figure 51 on page 60 shows a full master/slave system. The leftmost device is in Master Serial mode.

Master Serial mode is selected by a <000> on the mode pins (M2, M1, M0).

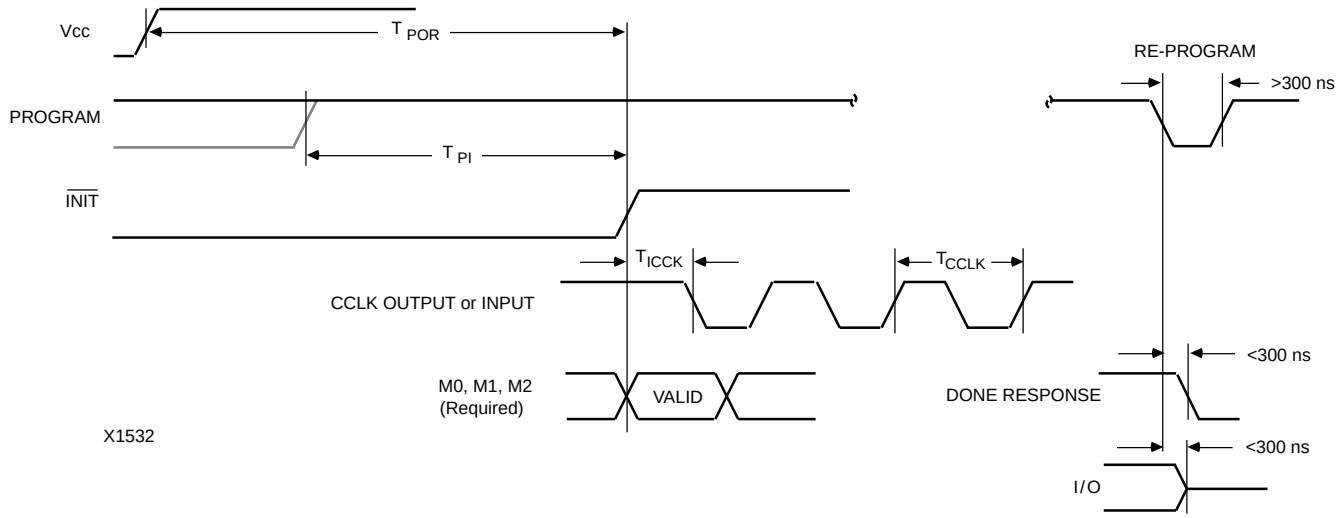



| | Description | Symbol | | Min | Max | Units |
|---|---|---|---|---|---|---|
| CCLK | DIN setup | 1 | $T_{DSCK}$ | 20 | | ns |
| | DIN hold | 2 | $T_{CKDS}$ | 0 | | ns |

Notes: 1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling $\overline{PROGRAM}$ Low until Vcc is valid.
2. Master Serial mode timing is based on testing in slave mode.

**Figure 53: Master Serial Mode Programming Switching Characteristics**

## Configuration Switching Characteristics




### Master Modes (XC4000E/EX)

| Description | | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| Power-On Reset | M0 = High | $T_{POR}$ | 10 | 40 | ms |
| | M0 = Low | $T_{POR}$ | 40 | 130 | ms |
| Program Latency | | $T_{PI}$ | 30 | 200 | µs per CLB column |
| CCLK (output) Delay | | $T_{ICCK}$ | 40 | 250 | µs |
| CCLK (output) Period, slow | | $T_{CCLK}$ | 640 | 2000 | ns |
| CCLK (output) Period, fast | | $T_{CCLK}$ | 80 | 250 | ns |

### Master Modes (XC4000XL)

| Description | | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| Power-On Reset | M0 = High | $T_{POR}$ | 10 | 40 | ms |
| | M0 = Low | $T_{POR}$ | 40 | 130 | ms |
| Program Latency | | $T_{PI}$ | 30 | 200 | µs per CLB column |
| CCLK (output) Delay | | $T_{ICCK}$ | 40 | 250 | µs |
| CCLK (output) Period, slow | | $T_{CCLK}$ | 540 | 1600 | ns |
| CCLK (output) Period, fast | | $T_{CCLK}$ | 67 | 200 | ns |

### Slave and Peripheral Modes (All)

| Description | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Power-On Reset | $T_{POR}$ | 10 | 33 | ms |
| Program Latency | $T_{PI}$ | 30 | 200 | µs per CLB column |
| CCLK (input) Delay (required) | $T_{ICCK}$ | 4 | | µs |
| CCLK (input) Period (required) | $T_{CCLK}$ | 100 | | ns |

**Table 25: Component Availability Chart for XC4000E FPGAs**

| | PINS | 84 | 100 | 100 | 120 | 144 | 156 | 160 | 191 | 208 | 208 | 223 | 225 | 240 | 240 | 299 | 304 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TYPE | Plast. PLCC | Plast. PQFP | Plast. VQFP | Ceram. PGA | Plast. TQFP | Ceram. PGA | Plast. PQFP | Ceram. PGA | High-Perf. QFP | Plast. PQFP | Ceram. PGA | Plast. BGA | High-Perf. QFP | Plast. PQFP | Ceram. PGA | High-Perf. QF |
| | CODE | PC84 | PQ100 | VQ100 | PG120 | TQ144 | PG156 | PQ160 | PG191 | HQ208 | PQ208 | PG223 | BG225 | HQ240 | PQ240 | PG299 | HQ304 |
| XC4003E | -4 | C I | C I | C I | C I | | | | | | | | | | | | |
| | -3 | C I | C I | C I | C I | | | | | | | | | | | | |
| | -2 | C I | C I | C I | C I | | | | | | | | | | | | |
| | -1 | C | C | C | C | | | | | | | | | | | | |
| XC4005E | -4 | C I | C I | | | C I | C I | C I | | | C I | | | | | | |
| | -3 | C I | C I | | | C I | C I | C I | | | C I | | | | | | |
| | -2 | C I | C I | | | C I | C I | C I | | | C I | | | | | | |
| | -1 | C | C | | | C | C | C | | | C | | | | | | |
| XC4006E | -4 | C I | | | | C I | C I | C I | | | C I | | | | | | |
| | -3 | C I | | | | C I | C I | C I | | | C I | | | | | | |
| | -2 | C I | | | | C I | C I | C I | | | C I | | | | | | |
| | -1 | C | | | | C | C | C | | | C | | | | | | |
| XC4008E | -4 | C I | | | | | | C I | C I | | C I | | | | | | |
| | -3 | C I | | | | | | C I | C I | | C I | | | | | | |
| | -2 | C I | | | | | | C I | C I | | C I | | | | | | |
| | -1 | C | | | | | | C | C | | C | | | | | | |
| XC4010E | -4 | C I | | | | | | C I | C I | C I | C I | | C I | | | | |
| | -3 | C I | | | | | | C I | C I | C I | C I | | C I | | | | |
| | -2 | C I | | | | | | C I | C I | C I | C I | | C I | | | | |
| | -1 | C | | | | | | C | C | C | C | | C | | | | |
| XC4013E | -4 | | | | | | | C I | | C I | C I | C I | C I | C I | C I | | |
| | -3 | | | | | | | C I | | C I | C I | C I | C I | C I | C I | | |
| | -2 | | | | | | | C I | | C I | C I | C I | C I | C I | C I | | |
| | -1 | | | | | | | C | | C | C | C | C | C | C | | |
| XC4020E | -4 | | | | | | | | | C I | | C I | | C I | | | |
| | -3 | | | | | | | | | C I | | C I | | C I | | | |
| | -2 | | | | | | | | | C I | | C I | | C I | | | |
| | -1 | | | | | | | | | C | | C | | C | | | |
| XC4025E | -4 | | | | | | | | | | | C I | | C I | | C I | C I |
| | -3 | | | | | | | | | | | C I | | C I | | C I | C I |
| | -2 | | | | | | | | | | | C | | C | | C | C |

1/29/99

C = Commercial $T_J$ = 0° to +85°C

I= Industrial $T_J$ = -40°C to +100°C

**Table 26: Component Availability Chart for XC4000EX FPGAs**

| | PINS | 208 | 240 | 299 | 304 | 352 | 411 | 432 |
|---|---|---|---|---|---|---|---|---|
| | TYPE | High-Perf. QFP | High-Perf. QFP | Ceram. PGA | High-Perf. QFP | Plast. BGA | Ceram. PGA | Plast. BGA |
| | CODE | HQ208 | HQ240 | PG299 | HQ304 | BG352 | PG411 | BG432 |
| XC4028EX | -4 | C I | C I | C I | C I | C I | | |
| | -3 | C I | C I | C I | C I | C I | | |
| | -2 | C | C | C | C | C | | |
| XC4036EX | -4 | | C I | | C I | C I | C I | C I |
| | -3 | | C I | | C I | C I | C I | C I |
| | -2 | | C | | C | C | C | C |

1/29/99

C = Commercial $T_J$ = 0° to +85°C

I= Industrial $T_J$ = -40°C to +100°C