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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1296 |
| Number of Logic Elements/Cells | 3078 |
| Total RAM Bits | 41472 |
| Number of I/O | 256 |
| Number of Gates | 36000 |
| Voltage - Supply | 3V ~ 3.6V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 304-BFQFP Exposed Pad |
| Supplier Device Package | 304-PQFP (40x40) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc4036xl-1hq304c |

Supported CLB memory configurations and timing modes for single- and dual-port modes are shown in [Table 3](#).

XC4000 Series devices are the first programmable logic devices with edge-triggered (synchronous) and dual-port RAM accessible to the user. Edge-triggered RAM simplifies system timing. Dual-port RAM doubles the effective throughput of FIFO applications. These features can be individually programmed in any XC4000 Series CLB.

Advantages of On-Chip and Edge-Triggered RAM

The on-chip RAM is extremely fast. The read access time is the same as the logic delay. The write access time is slightly slower. Both access times are much faster than any off-chip solution, because they avoid I/O delays.

Edge-triggered RAM, also called synchronous RAM, is a feature never before available in a Field Programmable Gate Array. The simplicity of designing with edge-triggered RAM, and the markedly higher achievable performance, add up to a significant improvement over existing devices with on-chip RAM.

Three application notes are available from Xilinx that discuss edge-triggered RAM: “XC4000E Edge-Triggered and Dual-Port RAM Capability,” “Implementing FIFOs in XC4000E RAM,” and “Synchronous and Asynchronous FIFO Designs.” All three application notes apply to both XC4000E and XC4000X RAM.

Table 3: Supported RAM Modes

| | 16 x 1 | 16 x 2 | 32 x 1 | Edge- Triggered Timing | Level- Sensitive Timing |
|-------------|--------------|--------------|--------------|------------------------------|-------------------------------|
| Single-Port | √ | √ | √ | √ | √ |
| Dual-Port | √ | | | √ | |

RAM Configuration Options

The function generators in any CLB can be configured as RAM arrays in the following sizes:

- Two 16x1 RAMs: two data inputs and two data outputs with identical or, if preferred, different addressing for each RAM
- One 32x1 RAM: one data input and one data output.

One F or G function generator can be configured as a 16x1 RAM while the other function generators are used to implement any function of up to 5 inputs.

Additionally, the XC4000 Series RAM may have either of two timing modes:

- Edge-Triggered (Synchronous): data written by the designated edge of the CLB clock. WE acts as a true clock enable.
- Level-Sensitive (Asynchronous): an external WE signal acts as the write strobe.

The selected timing mode applies to both function generators within a CLB when both are configured as RAM.

The number of read ports is also programmable:

- Single Port: each function generator has a common read and write port
- Dual Port: both function generators are configured together as a single 16x1 dual-port RAM with one write port and two read ports. Simultaneous read and write operations to the same or different addresses are supported.

RAM configuration options are selected by placing the appropriate library symbol.

Choosing a RAM Configuration Mode

The appropriate choice of RAM mode for a given design should be based on timing and resource requirements, desired functionality, and the simplicity of the design process. Recommended usage is shown in [Table 4](#).

The difference between level-sensitive, edge-triggered, and dual-port RAM is only in the write operation. Read operation and timing is identical for all modes of operation.

Table 4: RAM Mode Selection

| | Level-Sens itive | Edge-Trigg ered | Dual-Port Edge-Trigg ered |
|-------------------------|---------------------|--------------------|---------------------------------|
| Use for New Designs? | No | Yes | Yes |
| Size (16x1, Registered) | 1/2 CLB | 1/2 CLB | 1 CLB |
| Simultaneous Read/Write | No | No | Yes |
| Relative Performance | X | 2X | 2X (4X effective) |

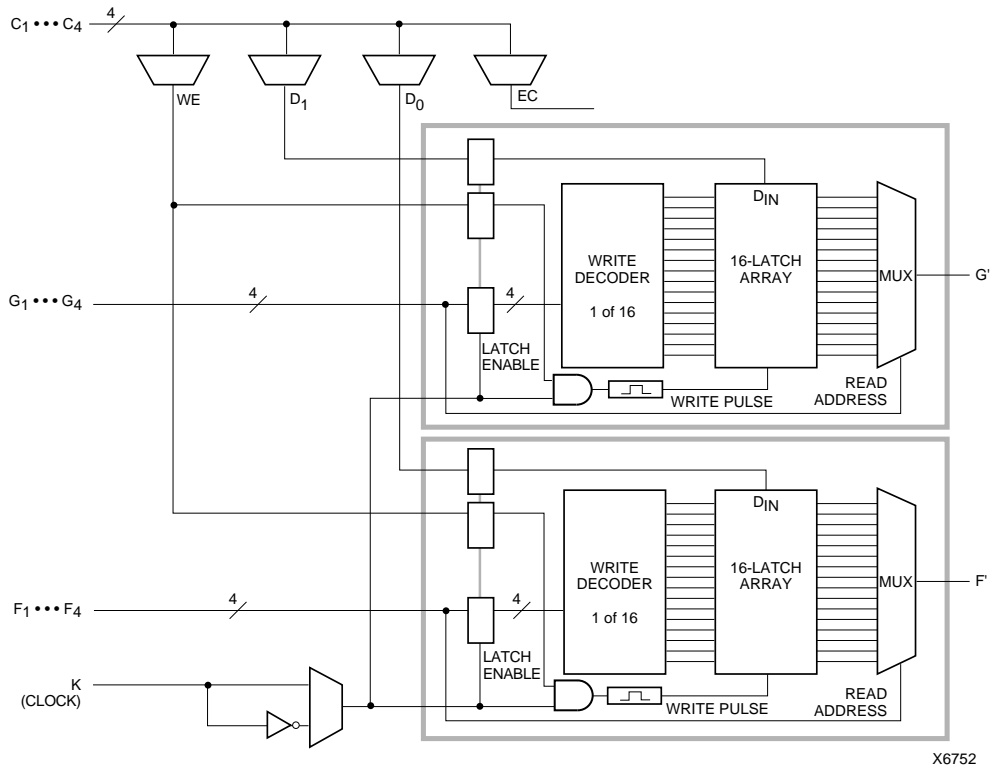
RAM Inputs and Outputs

The F1-F4 and G1-G4 inputs to the function generators act as address lines, selecting a particular memory cell in each look-up table.

The functionality of the CLB control signals changes when the function generators are configured as RAM. The DIN/H2, H1, and SR/H0 lines become the two data inputs (D0, D1) and the Write Enable (WE) input for the 16x2 memory. When the 32x1 configuration is selected, D1 acts as the fifth address bit and D0 is the data input.

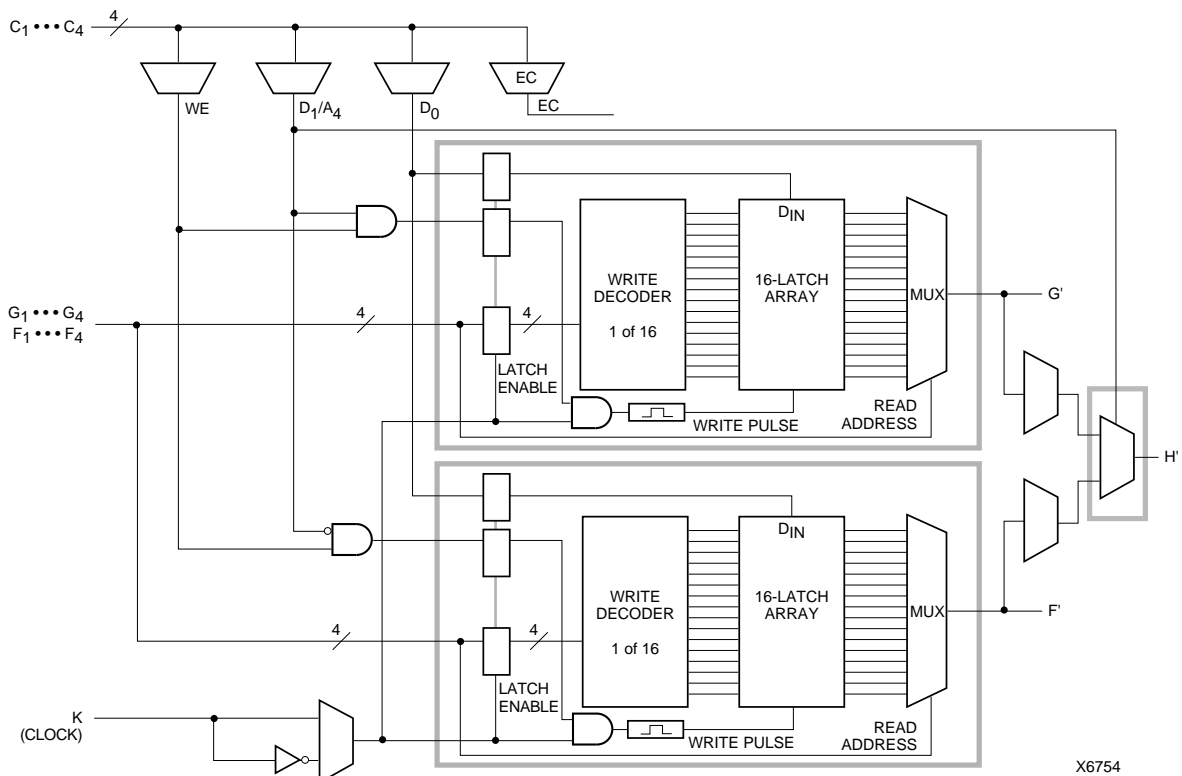
The contents of the memory cell(s) being addressed are available at the F' and G' function-generator outputs. They can exit the CLB through its X and Y outputs, or can be captured in the CLB flip-flop(s).

Configuring the CLB function generators as Read/Write memory does not affect the functionality of the other por-



X6752

Figure 4: 16x2 (or 16x1) Edge-Triggered Single-Port RAM



X6754

Figure 5: 32x1 Edge-Triggered Single-Port RAM (F and G addresses are identical)

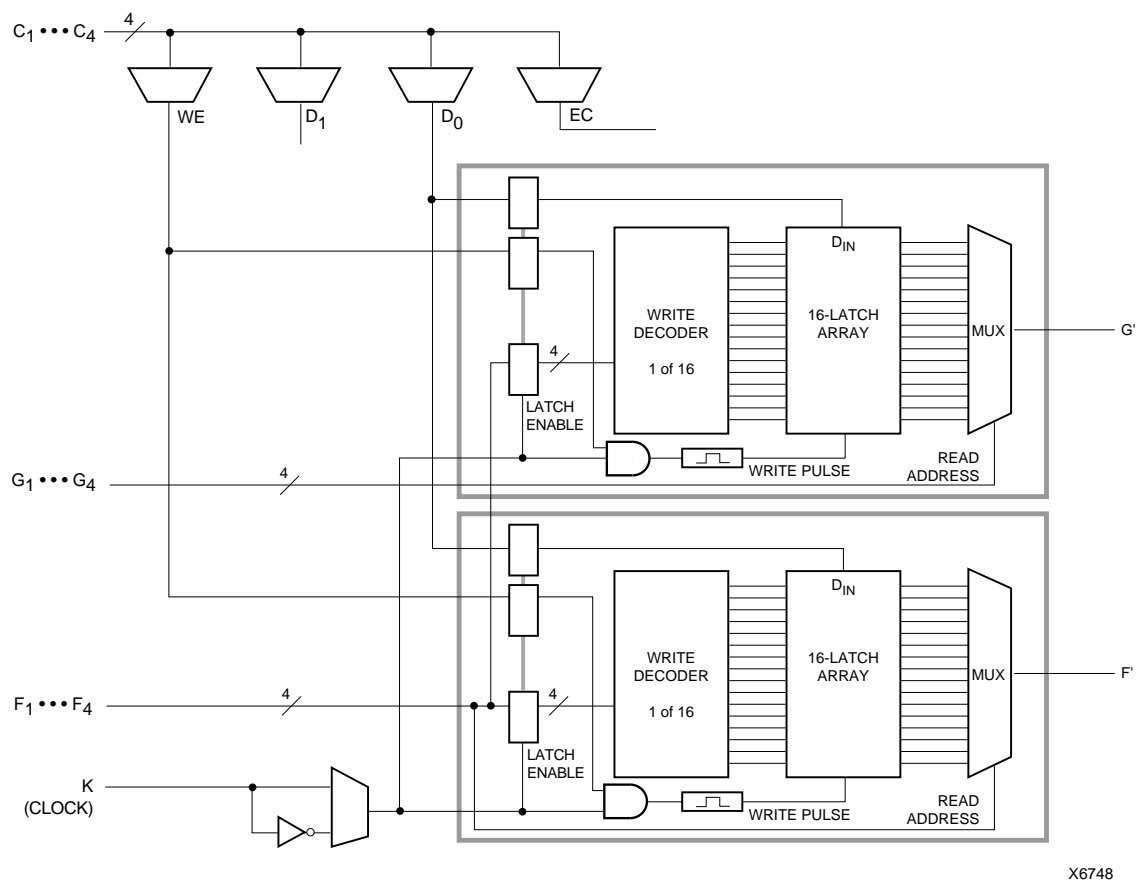


Figure 7: 16x1 Edge-Triggered Dual-Port RAM

Figure 8 shows the write timing for level-sensitive, single-port RAM.

The relationships between CLB pins and RAM inputs and outputs for single-port level-sensitive mode are shown in Table 7.

Figure 9 and Figure 10 show block diagrams of a CLB configured as 16x2 and 32x1 level-sensitive, single-port RAM.

Initializing RAM at Configuration

Both RAM and ROM implementations of the XC4000 Series devices are initialized during configuration. The initial contents are defined via an INIT attribute or property

attached to the RAM or ROM symbol, as described in the schematic library guide. If not defined, all RAM contents are initialized to all zeros, by default.

RAM initialization occurs only during configuration. The RAM content is not affected by Global Set/Reset.

Table 7: Single-Port Level-Sensitive RAM Signals

| RAM Signal | CLB Pin | Function |
|------------|----------------|--------------|
| D | D0 or D1 | Data In |
| A[3:0] | F1-F4 or G1-G4 | Address |
| WE | WE | Write Enable |
| O | F' or G' | Data Out |

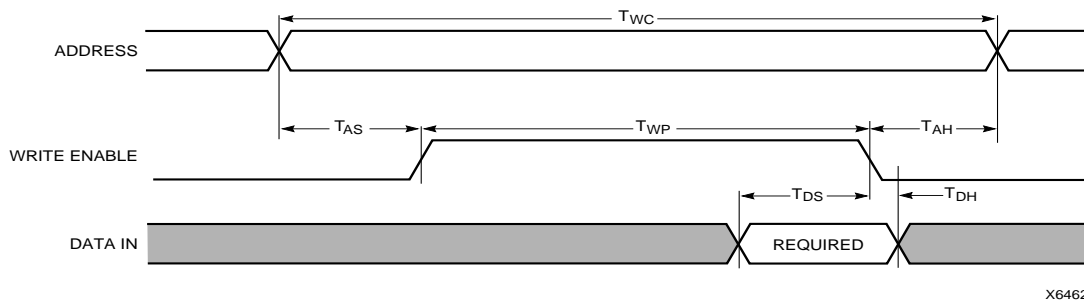


Figure 8: Level-Sensitive RAM Write Timing

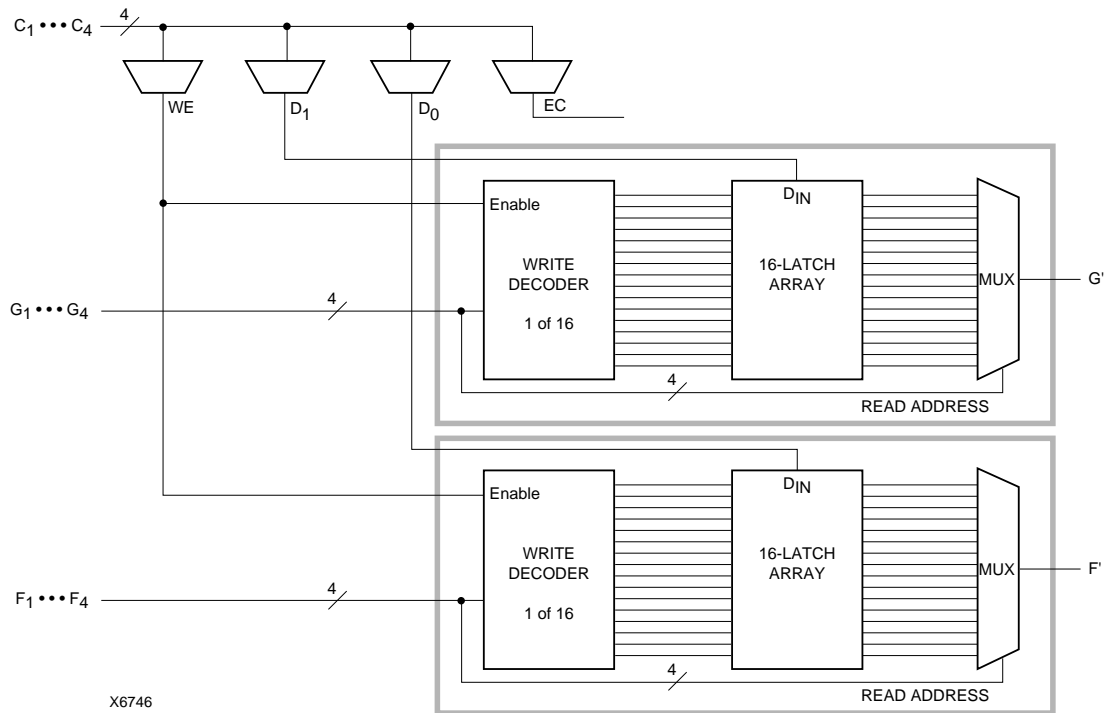


Figure 9: 16x2 (or 16x1) Level-Sensitive Single-Port RAM

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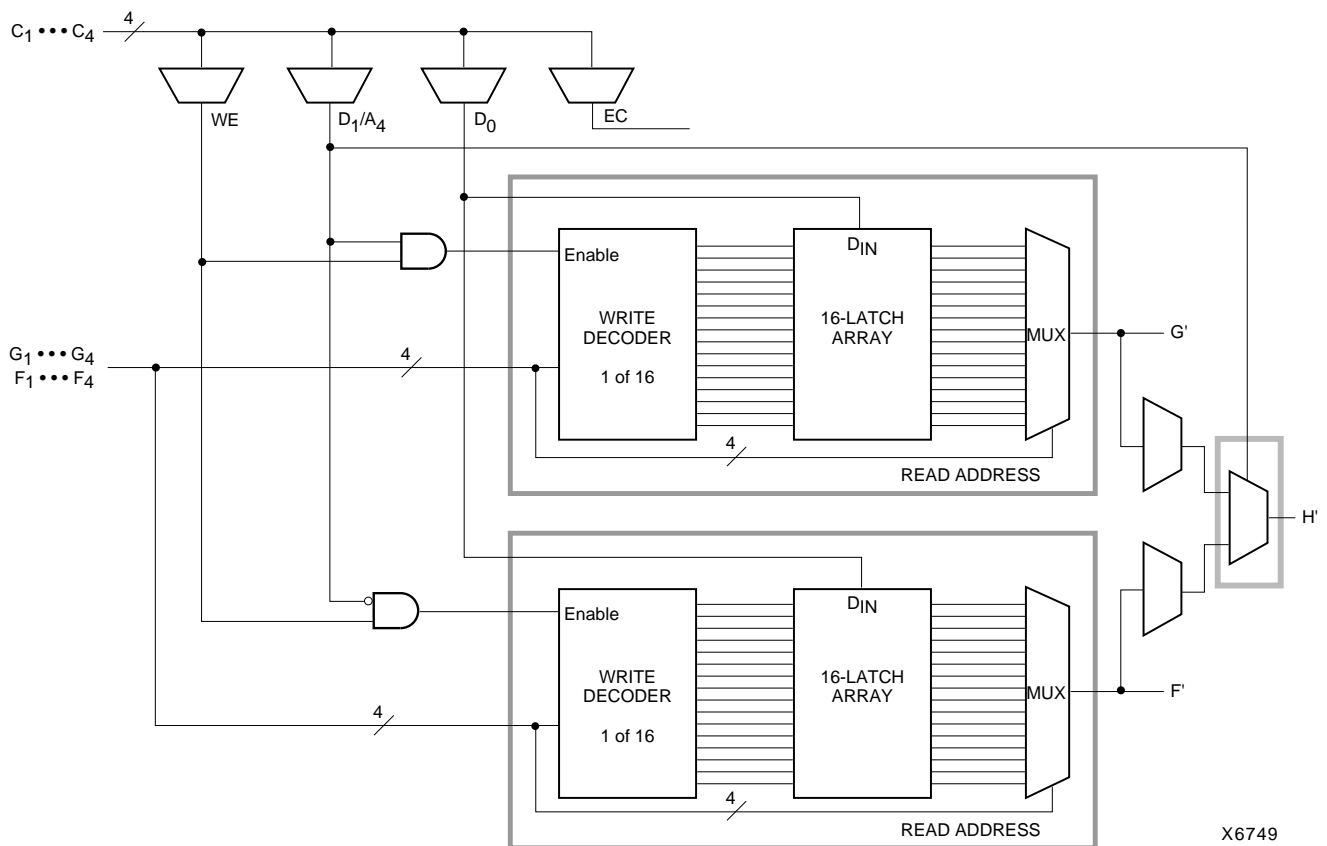


Figure 10: 32x1 Level-Sensitive Single-Port RAM (F and G addresses are identical)

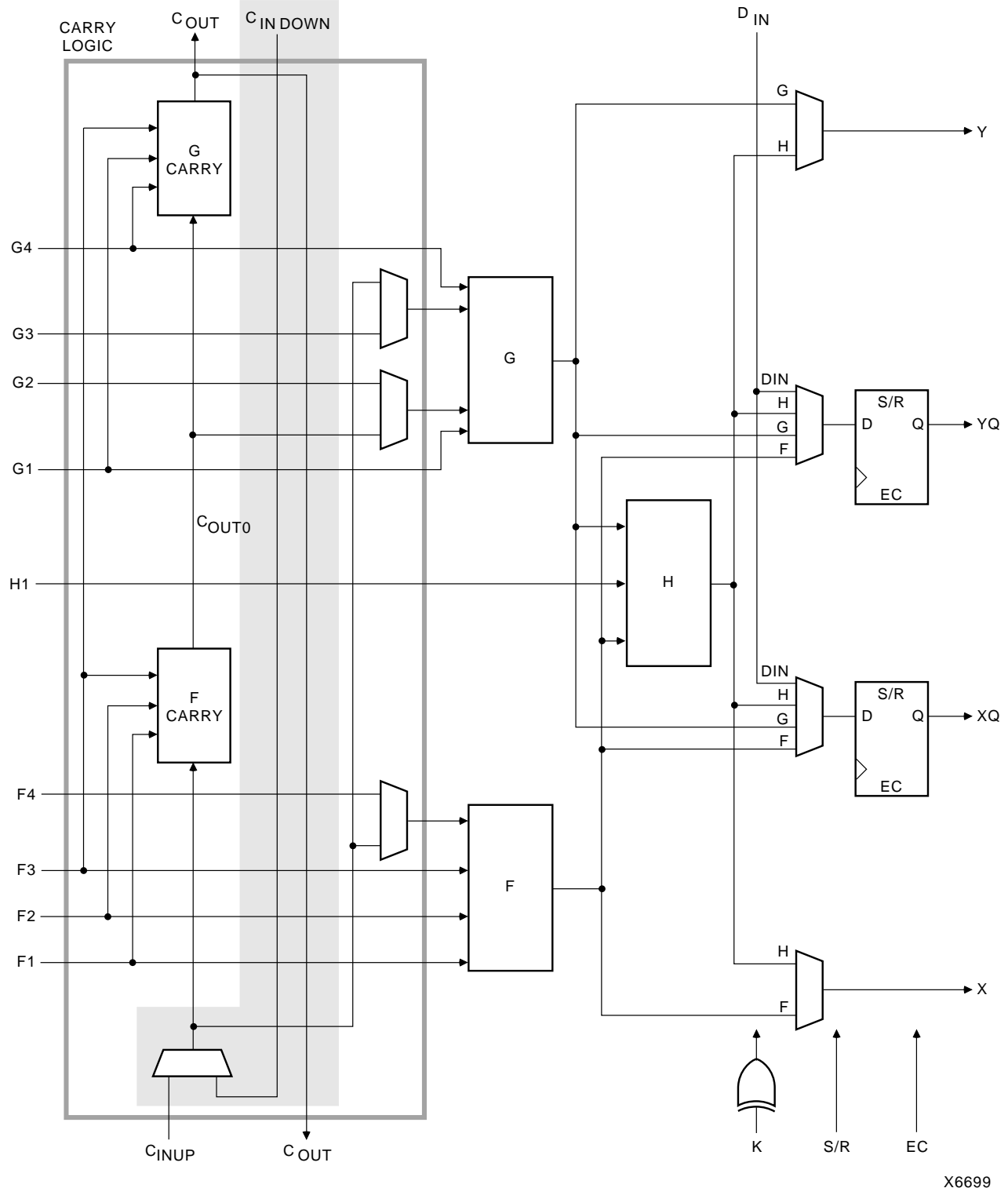


Figure 13: Fast Carry Logic in XC4000E CLB (shaded area not present in XC4000X)

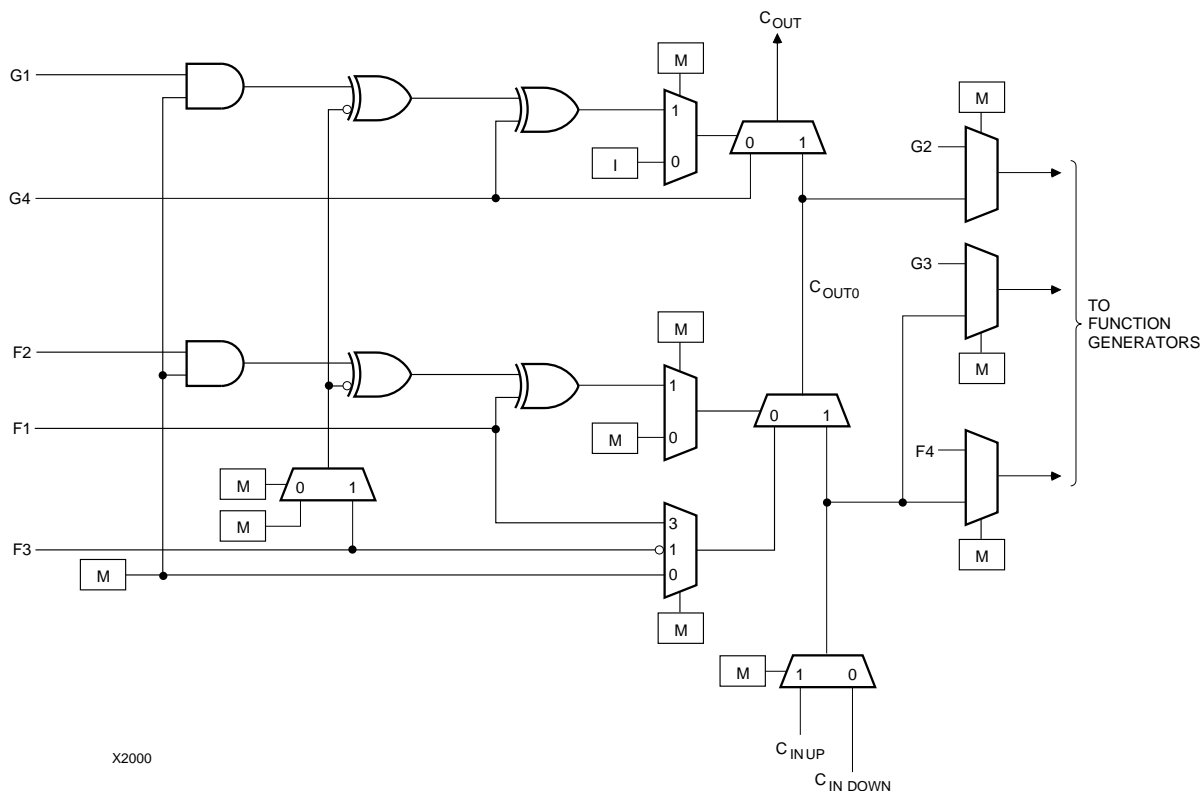


Figure 14: Detail of XC4000E Dedicated Carry Logic

Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals.

Figure 15 shows a simplified block diagram of the XC4000E IOB. A more complete diagram which includes the boundary scan logic of the XC4000E IOB can be found in Figure 40 on page 43, in the “Boundary Scan” section.

The XC4000X IOB contains some special features not included in the XC4000E IOB. These features are highlighted in a simplified block diagram found in **Figure 16**, and discussed throughout this section. When XC4000X special features are discussed, they are clearly identified in the text. Any feature not so identified is present in both XC4000E and XC4000X devices.

I/O Input Signals

Two paths, labeled I1 and I2 in [Figure 15](#) and [Figure 16](#), bring input signals into the array. Inputs also connect to an input register that can be programmed as either an edge-triggered flip-flop or a level-sensitive latch.

The choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are available, and some combinations of latches and flip-flops can be implemented in a single IOB, as described in the *XACT Libraries Guide*.

The XC4000E inputs can be globally configured for either TTL (1.2V) or 5.0 volt CMOS thresholds, using an option in the bitstream generation software. There is a slight input hysteresis of about 300mV. The XC4000E output levels are also configurable; the two global adjustments of input threshold and output level are independent.

Inputs on the XC4000XL are TTL compatible and 3.3V CMOS compatible. Outputs on the XC4000XL are pulled to the 3.3V positive supply.

The inputs of XC4000 Series 5-Volt devices can be driven by the outputs of any 3.3-Volt device, if the 5-Volt inputs are in TTL mode.

Supported sources for XC4000 Series device inputs are shown in [Table 8](#).

Additional Input Latch for Fast Capture (XC4000X only)

The XC4000X IOB has an additional optional latch on the input. This latch, as shown in [Figure 16](#), is clocked by the output clock — the clock used for the output flip-flop — rather than the input clock. Therefore, two different clocks can be used to clock the two input storage elements. This additional latch allows the very fast capture of input data, which is then synchronized to the internal clock by the IOB flip-flop or latch.

To use this Fast Capture technique, drive the output clock pin (the Fast Capture latching signal) from the output of one of the Global Early buffers supplied in the XC4000X. The second storage element should be clocked by a Global Low-Skew buffer, to synchronize the incoming data to the internal logic. (See [Figure 17](#).) These special buffers are described in “Global Nets and Buffers (XC4000X only)” on [page 37](#).

The Fast Capture latch (FCL) is designed primarily for use with a Global Early buffer. For Fast Capture, a single clock signal is routed through both a Global Early buffer and a Global Low-Skew buffer. (The two buffers share an input pad.) The Fast Capture latch is clocked by the Global Early buffer, and the standard IOB flip-flop or latch is clocked by the Global Low-Skew buffer. This mode is the safest way to use the Fast Capture latch, because the clock buffers on both storage elements are driven by the same pad. There is no external skew between clock pads to create potential problems.

To place the Fast Capture latch in a design, use one of the special library symbols, ILFFX or ILFLX. ILFFX is a transparent-Low Fast Capture latch followed by an active-High input flip-flop. ILFLX is a transparent-Low Fast Capture latch followed by a transparent-High input latch. Any of the clock inputs can be inverted before driving the library element, and the inverter is absorbed into the IOB. If a single BUFG output is used to drive both clock inputs, the software automatically runs the clock through both a Global Low-Skew buffer and a Global Early buffer, and clocks the Fast Capture latch appropriately.

[Figure 16 on page 21](#) also shows a two-tap delay on the input. By default, if the Fast Capture latch is used, the Xilinx software assumes a Global Early buffer is driving the clock, and selects MEDDELAY to ensure a zero hold time. Select

the desired delay based on the discussion in the previous subsection.

IOB Output Signals

Output signals can be optionally inverted within the IOB, and can pass directly to the pad or be stored in an edge-triggered flip-flop. The functionality of this flip-flop is shown in [Table 11](#).

An active-High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (OUT) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB.

The 4-mA maximum output current specification of many FPGAs often forces the user to add external buffers, which are especially cumbersome on bidirectional I/O lines. The XC4000E and XC4000EX/XL devices solve many of these problems by providing a guaranteed output sink current of 12 mA. Two adjacent outputs can be interconnected externally to sink up to 24 mA. The XC4000E and XC4000EX/XL FPGAs can thus directly drive buses on a printed circuit board.

By default, the output pull-up structure is configured as a TTL-like totem-pole. The High driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below Vcc. Alternatively, the outputs can be globally configured as CMOS drivers, with p-channel pull-up transistors pulling to Vcc. This option, applied using the bitstream generation software, applies to all outputs on the device. It is not individually programmable. In the XC4000XL, all outputs are pulled to the positive supply rail.

Table 11: Output Flip-Flop Functionality (active rising edge is shown)

| Mode | Clock | Clock Enable | T | D | Q |
|-----------------|-------|--------------|----|---|----|
| Power-Up or GSR | X | X | 0* | X | SR |
| Flip-Flop | X | 0 | 0* | X | Q |
| | | 1* | 0* | D | D |
| | X | X | 1 | X | Z |
| | 0 | X | 0* | X | Q |

Legend:

X

Don't care

Rising edge

SR

Set or Reset value. Reset is default.

0*

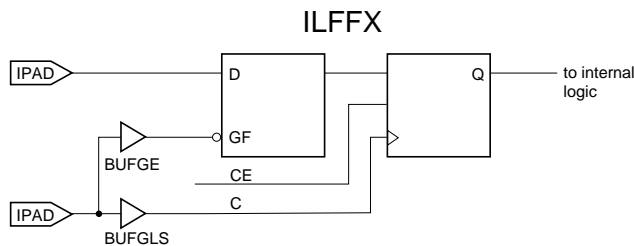
Input is Low or unconnected (default value)

1*

Input is High or unconnected (default value)

Z

3-state



X9013

Figure 17: Examples Using XC4000X FCL

Output Multiplexer/2-Input Function Generator (XC4000X only)

As shown in [Figure 16 on page 21](#), the output path in the XC4000X IOB contains an additional multiplexer not available in the XC4000E IOB. The multiplexer can also be configured as a 2-input function generator, implementing a pass-gate, AND-gate, OR-gate, or XOR-gate, with 0, 1, or 2 inverted inputs. The logic used to implement these functions is shown in the upper gray area of [Figure 16](#).

When configured as a multiplexer, this feature allows two output signals to time-share the same output pad; effectively doubling the number of device outputs without requiring a larger, more expensive package.

When the MUX is configured as a 2-input function generator, logic can be implemented within the IOB itself. Combined with a Global Early buffer, this arrangement allows very high-speed gating of a single signal. For example, a wide decoder can be implemented in CLBs, and its output gated with a Read or Write Strobe Driven by a BUFGE buffer, as shown in [Figure 19](#). The critical-path pin-to-pin delay of this circuit is less than 6 nanoseconds.

As shown in [Figure 16](#), the IOB input pins Out, Output Clock, and Clock Enable have different delays and different flexibilities regarding polarity. Additionally, Output Clock sources are more limited than the other inputs. Therefore, the Xilinx software does not move logic into the IOB function generators unless explicitly directed to do so.

The user can specify that the IOB function generator be used, by placing special library symbols beginning with the letter "O." For example, a 2-input AND-gate in the IOB function generator is called OAND2. Use the symbol input pin labelled "F" for the signal on the critical path. This signal is placed on the OK pin — the IOB input with the shortest delay to the function generator. Two examples are shown in [Figure 20](#).

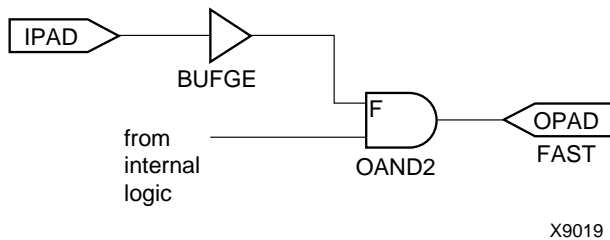


Figure 19: Fast Pin-to-Pin Path in XC4000X



Figure 20: AND & MUX Symbols in XC4000X IOB

Other IOB Options

There are a number of other programmable options in the XC4000 Series IOB.

Pull-up and Pull-down Resistors

Programmable pull-up and pull-down resistors are useful for tying unused pins to Vcc or Ground to minimize power consumption and reduce noise sensitivity. The configurable pull-up resistor is a p-channel transistor that pulls to Vcc. The configurable pull-down resistor is an n-channel transistor that pulls to Ground.

The value of these resistors is 50 kΩ – 100 kΩ. This high value makes them unsuitable as wired-AND pull-up resistors.

The pull-up resistors for most user-programmable IOBs are active during the configuration process. See [Table 22 on page 58](#) for a list of pins with pull-ups active before and during configuration.

After configuration, voltage levels of unused pads, bonded or un-bonded, must be valid logic levels, to reduce noise sensitivity and avoid excess current. Therefore, by default, unused pads are configured with the internal pull-up resistor active. Alternatively, they can be individually configured with the pull-down resistor, or as a driven output, or to be driven by an external source. To activate the internal pull-up, attach the PULLUP library component to the net attached to the pad. To activate the internal pull-down, attach the PULLDOWN library component to the net attached to the pad.

Independent Clocks

Separate clock signals are provided for the input and output flip-flops. The clock can be independently inverted for each flip-flop within the IOB, generating either falling-edge or rising-edge triggered flip-flops. The clock inputs for each IOB are independent, except that in the XC4000X, the Fast Capture latch shares an IOB input with the output clock pin.

Early Clock for IOBs (XC4000X only)

Special early clocks are available for IOBs. These clocks are sourced by the same sources as the Global Low-Skew buffers, but are separately buffered. They have fewer loads and therefore less delay. The early clock can drive either the IOB output clock or the IOB input clock, or both. The early clock allows fast capture of input data, and fast clock-to-output on output data. The Global Early buffers that drive these clocks are described in ["Global Nets and Buffers \(XC4000X only\)" on page 37](#).

Global Set/Reset

As with the CLB registers, the Global Set/Reset signal (GSR) can be used to set or clear the input and output registers, depending on the value of the INIT attribute or property. The two flip-flops can be individually configured to set

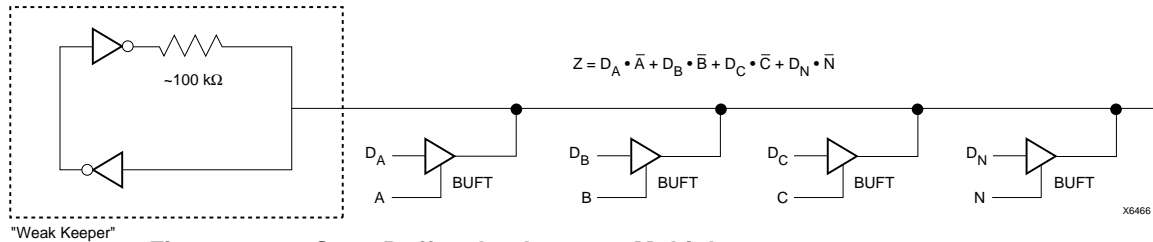


Figure 22: 3-State Buffers Implement a Multiplexer

Wide Edge Decoders

Dedicated decoder circuitry boosts the performance of wide decoding functions. When the address or data field is wider than the function generator inputs, FPGAs need multi-level decoding and are thus slower than PALs. XC4000 Series CLBs have nine inputs. Any decoder of up to nine inputs is, therefore, compact and fast. However, there is also a need for much wider decoders, especially for address decoding in large microprocessor systems.

An XC4000 Series FPGA has four programmable decoders located on each edge of the device. The inputs to each decoder are any of the IOB I1 signals on that edge plus one local interconnect per CLB row or column. Each row or column of CLBs provides up to three variables or their complements., as shown in Figure 23. Each decoder generates a High output (resistor pull-up) when the AND condition of the selected inputs, or their complements, is true. This is analogous to a product term in typical PAL devices.

Each of these wired-AND gates is capable of accepting up to 42 inputs on the XC4005E and 72 on the XC4013E. There are up to 96 inputs for each decoder on the XC4028X and 132 on the XC4052X. The decoders may also be split in two when a larger number of narrower decoders are required, for a maximum of 32 decoders per device.

The decoder outputs can drive CLB inputs, so they can be combined with other logic to form a PAL-like AND/OR structure. The decoder outputs can also be routed directly to the chip outputs. For fastest speed, the output should be on the same chip edge as the decoder. Very large PALs can be emulated by ORing the decoder outputs in a CLB. This decoding feature covers what has long been considered a weakness of older FPGAs. Users often resorted to external PALs for simple but fast decoding functions. Now, the dedicated decoders in the XC4000 Series device can implement these functions fast and efficiently.

To use the wide edge decoders, place one or more of the WAND library symbols (WAND1, WAND4, WAND8, WAND16). Attach a DECODE attribute or property to each WAND symbol. Tie the outputs together and attach a PUL-

LUP symbol. Location attributes or properties such as L (left edge) or TR (right half of top edge) should also be used to ensure the correct placement of the decoder inputs.

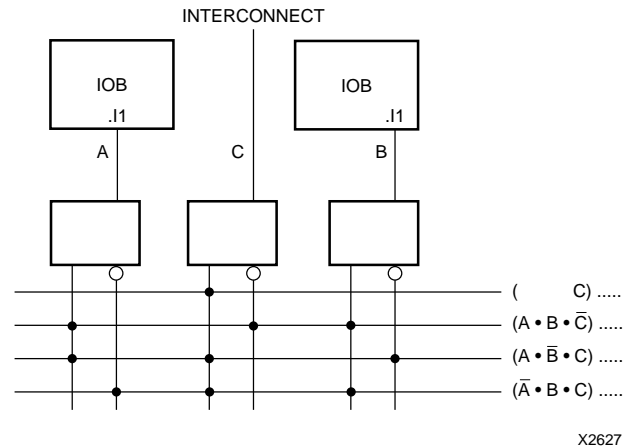


Figure 23: XC4000 Series Edge Decoding Example

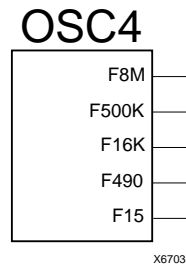


Figure 24: XC4000 Series Oscillator Symbol

On-Chip Oscillator

XC4000 Series devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration modes. The oscillator runs at a nominal 8 MHz frequency that varies with process, Vcc, and temperature. The output frequency falls between 4 and 10 MHz.

The top and bottom Global Early buffers are about 1 ns slower clock to out than the left and right Global Early buffers.

The Global Early buffers can be driven by either semi-dedicated pads or internal logic. They share pads with the Global Low-Skew buffers, so a single net can drive both global buffers, as described above.

To use a Global Early buffer, place a BUFGE element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=T attribute or property to direct that a BUFGE be placed in one of the two Global Early buffers on the top edge of the device, or a LOC=TR to indicate the Global Early buffer on the top edge of the device, on the right.

Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated Vcc and Ground ring surrounding the logic array provides power to the I/O drivers, as shown in [Figure 39](#). An independent matrix of Vcc and Ground lines supplies the interior logic of the device.

This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately de-coupled. Typically, a 0.1 μ F capacitor connected between each Vcc pin and the board's Ground plane will provide adequate de-coupling.

Output buffers capable of driving/sinking the specified 12 mA loads under specified worst-case conditions may be capable of driving/sinking up to 10 times as much current under best case conditions.

Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the Ground pads. The I/O Block output buffers have a slew-rate limited mode (default) which should be used where output rise and fall times are not speed-critical.

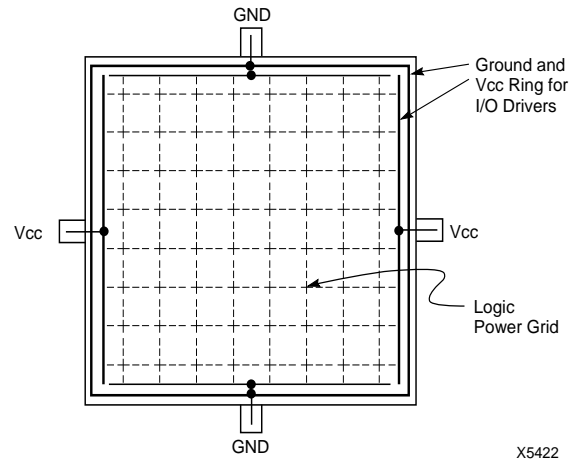


Figure 39: XC4000 Series Power Distribution

Pin Descriptions

There are three types of pins in the XC4000 Series devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with a 50 k Ω - 100 k Ω pull-up resistor.

After configuration, if an IOB is unused it is configured as an input with a 50 k Ω - 100 k Ω pull-up resistor.

XC4000 Series devices have no dedicated Reset input. Any user I/O can be configured to drive the Global Set/Reset net, GSR. See ["Global Set/Reset" on page 11](#) for more information on GSR.

XC4000 Series devices have no Powerdown control input, as the XC3000 and XC2000 families do. The XC3000/XC2000 Powerdown control also 3-stated all of the device

I/O pins. For XC4000 Series devices, use the global 3-state net, GTS, instead. This net 3-states all outputs, but does not place the device in low-power mode. See ["IOB Output Signals" on page 23](#) for more information on GTS.

Device pins for XC4000 Series devices are described in [Table 16](#). Pin functions during configuration for each of the seven configuration modes are summarized in [Table 22 on page 58](#), in the "Configuration Timing" section.

Table 16: Pin Descriptions (Continued)

| Pin Name | I/O During Config. | I/O After Config. | Pin Description |
|---------------------------------------------|--------------------|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TDI, TCK, TMS | I | I/O or I (JTAG) | If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. The pins can be used automatically or user-constrained. To use them, use "LOC=" or place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used. |
| HDC | O | I/O | High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin. |
| $\overline{\text{LDC}}$ | O | I/O | Low During Configuration ($\overline{\text{LDC}}$) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, $\overline{\text{LDC}}$ is a user-programmable I/O pin. |
| $\overline{\text{INIT}}$ | I/O | I/O | Before and during configuration, $\overline{\text{INIT}}$ is a bidirectional signal. A 1 k Ω - 10 k Ω external pull-up resistor is recommended. As an active-Low open-drain output, $\overline{\text{INIT}}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active-Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 μs after $\overline{\text{INIT}}$ has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, $\overline{\text{INIT}}$ is a user-programmable I/O pin. |
| PGCK1 - PGCK4 (XC4000E only) | Weak Pull-up | I or I/O | Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O. The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFGP symbol is automatically placed on one of these pins. |
| SGCK1 - SGCK4 (XC4000E only) | Weak Pull-up | I or I/O | Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGE symbol is automatically placed on one of these pins. |
| GCK1 - GCK8 (XC4000X only) | Weak Pull-up | I or I/O | Eight inputs can each drive a Global Low-Skew buffer. In addition, each can drive a Global Early buffer. Each pair of global buffers can also be driven from internal logic, but must share an input signal. If not used to drive a global buffer, any of these pins is a user-programmable I/O. Any input pad symbol connected directly to the input of a BUFGS or BUFG symbol is automatically placed on one of these pins. |
| FCLK1 - FCLK4 (XC4000XLA and XC4000XV only) | Weak Pull-up | I or I/O | Four inputs can each drive a Fast Clock (FCLK) buffer which can deliver a clock signal to any IOB clock input in the octant of the die served by the Fast Clock buffer. Two Fast Clock buffers serve the two IOB octants on the left side of the die and the other two Fast Clock buffers serve the two IOB octants on the right side of the die. On each side of the die, one Fast Clock buffer serves the upper octant and the other serves the lower octant. If not used to drive a Fast Clock buffer, any of these pins is a user-programmable I/O. |

Setting CCLK Frequency

For Master modes, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz for XC4000E and XC4000EX devices and from 0.6 MHz to 1.8 MHz for XC4000XL devices. In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz for XC4000E/EX devices and from 5 MHz to 15 MHz for XC4000XL devices. The frequency is selected by an option when running the bitstream generation software. If an XC4000 Series Master is driving an XC3000- or XC2000-family slave, slow CCLK mode must be used. In addition, an XC4000XL device driving a XC4000E or XC4000EX should use slow mode. Slow mode is the default.

Table 19: XC4000 Series Data Stream Formats

| Data Type | All Other Modes (D0...) |
|-----------------------------|-------------------------|
| Fill Byte | 11111111b |
| Preamble Code | 0010b |
| Length Count | COUNT(23:0) |
| Fill Bits | 1111b |
| Start Field | 0b |
| Data Frame | DATA(n-1:0) |
| CRC or Constant Field Check | xxxx (CRC) or 0110b |
| Extend Write Cycle | — |
| Postamble | 01111111b |
| Start-Up Bytes | xxh |
| Legend: | |
| Not shaded | Once per bitstream |
| Light | Once per data frame |
| Dark | Once per device |

Data Stream Format

The data stream (“bitstream”) format is identical for all configuration modes.

The data stream formats are shown in [Table 19](#). Bit-serial data is read from left to right, and byte-parallel data is effectively assembled from this serial bitstream, with the first bit in each byte assigned to D0.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones. This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see [Table 20](#) and [Table 21](#)). Each frame begins with a start field and ends with an error check. A postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All startup bytes are don't-cares; these bytes are not included in bitstreams created by the Xilinx software.

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading and the pulling down of the $\overline{\text{INIT}}$ pin. In Master modes, CCLK and address signals continue to operate externally. The user must detect $\overline{\text{INIT}}$ and initialize a new configuration by pulsing the $\overline{\text{PROGRAM}}$ pin Low or cycling Vcc.

Start-up from a User Clock (STARTUP.CLK)

When, instead of CCLK, a user-supplied start-up clock is selected, Q1 is used to bridge the unknown phase relationship between CCLK and the user clock. This arbitration causes an unavoidable one-cycle uncertainty in the timing of the rest of the start-up sequence.

DONE Goes High to Signal End of Configuration

XC4000 Series devices read the expected length count from the bitstream and store it in an internal register. The length count varies according to the number of devices and the composition of the daisy chain. Each device also counts the number of CCLKs during configuration.

Two conditions have to be met in order for the DONE pin to go high:

- the chip's internal memory must be full, and
- the configuration length count must be met, *exactly*.

This is important because the counter that determines when the length count is met begins with the very first CCLK, not the first one after the preamble.

Therefore, if a stray bit is inserted before the preamble, or the data source is not ready at the time of the first CCLK, the internal counter that holds the number of CCLKs will be one ahead of the actual number of data bits read. At the end of configuration, the configuration memory will be full, but the number of bits in the internal counter will not match the expected length count.

As a consequence, a Master mode device will continue to send out CCLKs until the internal counter turns over to zero, and then reaches the correct length count a second time. This will take several seconds [$2^{24} * \text{CCLK period}$] — which is sometimes interpreted as the device not configuring at all.

If it is not possible to have the data ready at the time of the first CCLK, the problem can be avoided by increasing the number in the length count by the appropriate value. The *XACT User Guide* includes detailed information about manually altering the length count.

Note that DONE is an open-drain output and does not go High unless an internal pull-up is activated or an external pull-up is attached. The internal pull-up is activated as the default by the bitstream generation software.

Release of User I/O After DONE Goes High

By default, the user I/O are released one CCLK cycle after the DONE pin goes High. If CCLK is not clocked after DONE goes High, the outputs remain in their initial state — 3-stated, with a 50 k Ω - 100 k Ω pull-up. The delay from DONE High to active user I/O is controlled by an option to the bitstream generation software.

Release of Global Set/Reset After DONE Goes High

By default, Global Set/Reset (GSR) is released two CCLK cycles after the DONE pin goes High. If CCLK is not clocked twice after DONE goes High, all flip-flops are held in their initial set or reset state. The delay from DONE High to GSR inactive is controlled by an option to the bitstream generation software.

Configuration Complete After DONE Goes High

Three full CCLK cycles are required after the DONE pin goes High, as shown in [Figure 47 on page 53](#). If CCLK is not clocked three times after DONE goes High, readback cannot be initiated and most boundary scan instructions cannot be used.

Configuration Through the Boundary Scan Pins

XC4000 Series devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with $\overline{\text{INIT}}$ held Low (or drive the $\overline{\text{PROGRAM}}$ pin Low for more than 300 ns followed by a High while holding $\overline{\text{INIT}}$ Low). Holding $\overline{\text{INIT}}$ Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold $\overline{\text{INIT}}$ Low.
- Issue the CONFIG command to the TMS input
- Wait for $\overline{\text{INIT}}$ to go High
- Sequence the boundary scan Test Access Port to the SHIFT-DR state
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after INIT goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note XAPP017, “*Boundary Scan in XC4000 Devices*.” This application note also applies to XC4000E and XC4000X devices.

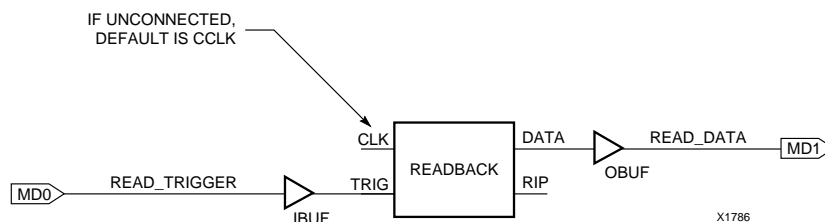


Figure 49: Readback Schematic Example

Readback Options

Readback options are: Read Capture, Read Abort, and Clock Select. They are set with the bitstream generation software.

Read Capture

When the Read Capture option is selected, the readback data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals *are* inverted.

When the Read Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations.

If the RAM capability of the CLBs is used, RAM data are available in readback, since they directly overwrite the F and G function-table configuration of the CLB.

RDBK.TRIG is located in the lower-left corner of the device, as shown in [Figure 50](#).

Read Abort

When the Read Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the readback operation and prepares the logic to accept another trigger.

After an aborted readback, additional clocks (up to one readback clock per configuration frame) may be required to re-initialize the control logic. The status of readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If readback must be inhibited for security reasons, the readback control nets are simply not connected.

RDBK.CLK is located in the lower right chip corner, as shown in [Figure 50](#).

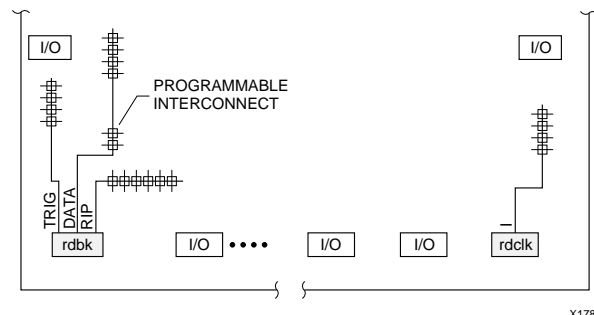


Figure 50: READBACK Symbol in Graphical Editor

Violating the Maximum High and Low Time Specification for the Readback Clock

The readback clock has a maximum High and Low time specification. In some cases, this specification cannot be met. For example, if a processor is controlling readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in [Table 19](#), [Table 20](#) and [Table 21](#).

Readback with the XChecker Cable

The XChecker Universal Download/Readback Cable and Logic Probe uses the readback feature for bitstream verification. It can also display selected internal signals on the PC or workstation screen, functioning as a low-cost in-circuit emulator.

Master Serial Mode

In Master Serial mode, the CCLK output of the lead FPGA drives a Xilinx Serial PROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

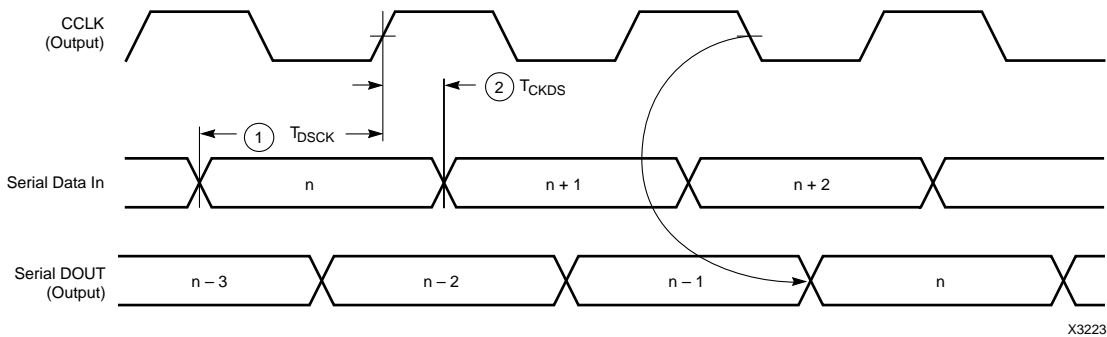
In the bitstream generation software, the user can specify Fast ConfigRate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight.

For actual timing values please refer to “**Configuration Switching Characteristics**” on page 68. Be sure that the serial PROM and slaves are fast enough to support this data rate. XC2000, XC3000/A, and XC3100A devices do not support the Fast ConfigRate option.

The SPROM CE input can be driven from either $\overline{\text{LDC}}$ or DONE. Using $\overline{\text{LDC}}$ avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but $\overline{\text{LDC}}$ is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the early DONE option is invoked.

Figure 51 on page 60 shows a full master/slave system. The leftmost device is in Master Serial mode.

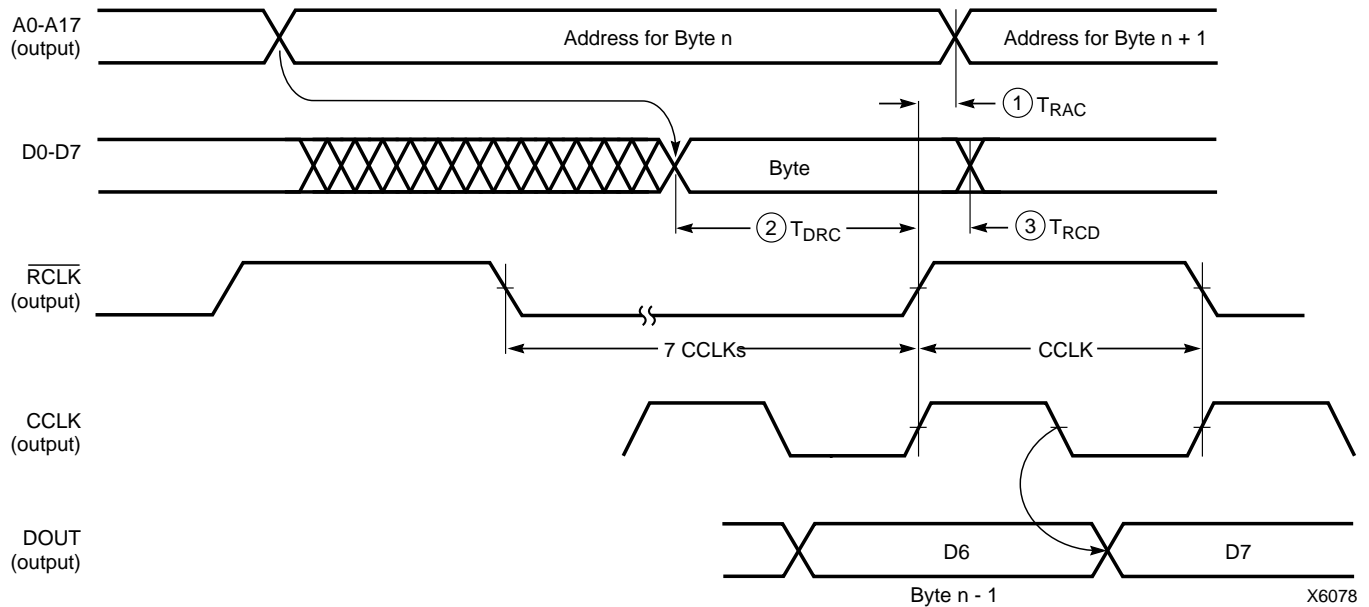
Master Serial mode is selected by a <000> on the mode pins (M2, M1, M0).



| | Description | Symbol | Min | Max | Units |
|------|-------------|--------------|-----|-----|-------|
| CCLK | DIN setup | 1 T_{DSCK} | 20 | | ns |
| | DIN hold | 2 T_{CKDS} | 0 | | ns |

Notes: 1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling PROGRAM Low until Vcc is valid.
2. Master Serial mode timing is based on testing in slave mode.

Figure 53: Master Serial Mode Programming Switching Characteristics



| | Description | Symbol | Min | Max | Units |
|------|------------------------|-------------|-----|-----|-------|
| RCLK | Delay to Address valid | 1 T_{RAC} | 0 | 200 | ns |
| | Data setup time | 2 T_{DRC} | 60 | | ns |
| | Data hold time | 3 T_{RCD} | 0 | | ns |

Notes: 1. At power-up, V_{cc} must rise from 2.0 V to V_{cc} min in less than 25 ms, otherwise delay configuration by pulling PROGRAM Low until V_{cc} is valid.
2. The first Data byte is loaded and CCLK starts at the end of the first \overline{RCLK} active cycle (rising edge).
This timing diagram shows that the EPROM requirements are extremely relaxed. EPROM access time can be longer than 500 ns. EPROM data output has no hold-time requirements.

Figure 55: Master Parallel Mode Programming Switching Characteristics

Synchronous Peripheral Mode

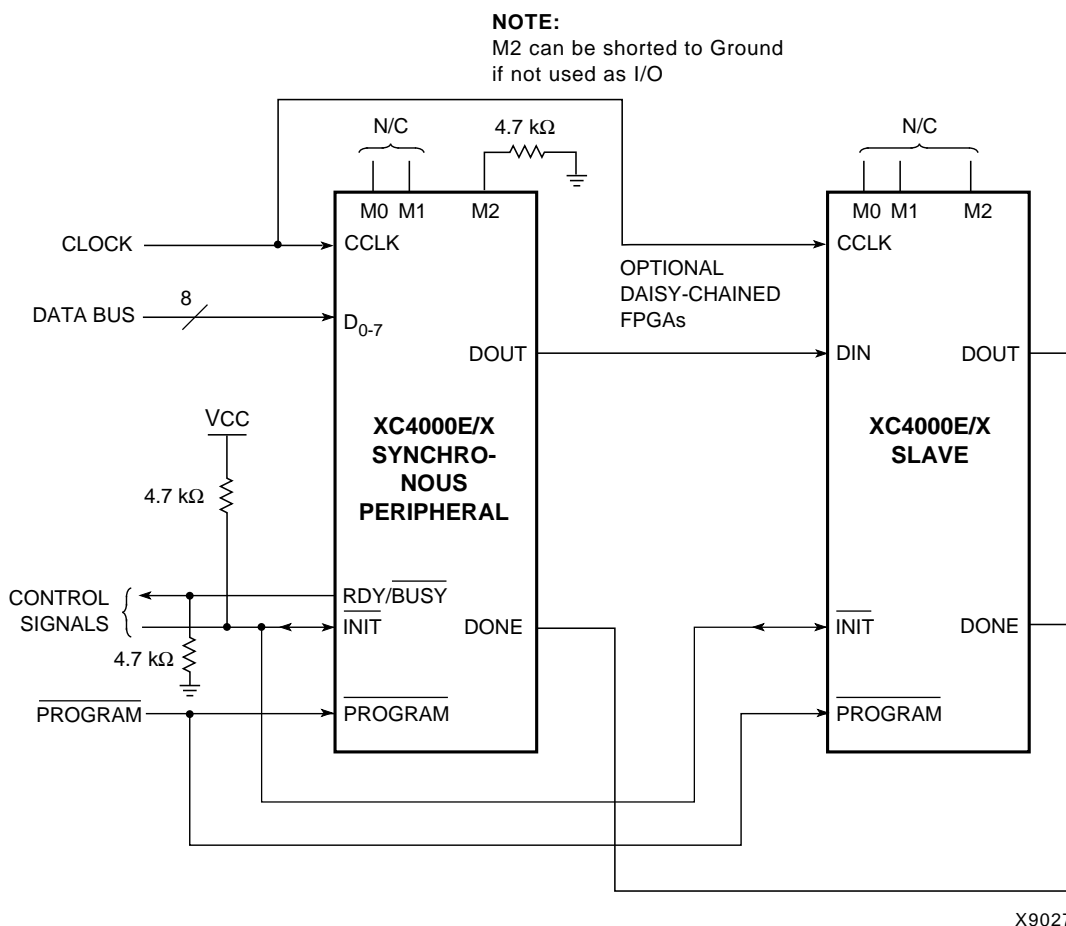
Synchronous Peripheral mode can also be considered Slave Parallel mode. An external signal drives the CCLK input(s) of the FPGA(s). The first byte of parallel configuration data must be available at the Data inputs of the lead FPGA a short setup time before the rising CCLK edge. Subsequent data bytes are clocked in on every eighth consecutive rising CCLK edge.

The same CCLK edge that accepts data, also causes the RDY/ $\overline{\text{BUSY}}$ output to go High for one CCLK period. The pin name is a misnomer. In Synchronous Peripheral mode it is really an ACKNOWLEDGE signal. Synchronous operation does not require this response, but it is a meaningful signal for test purposes. Note that RDY/ $\overline{\text{BUSY}}$ is pulled High with a high-impedance pullup prior to $\overline{\text{INIT}}$ going High.

The lead FPGA serializes the data and presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

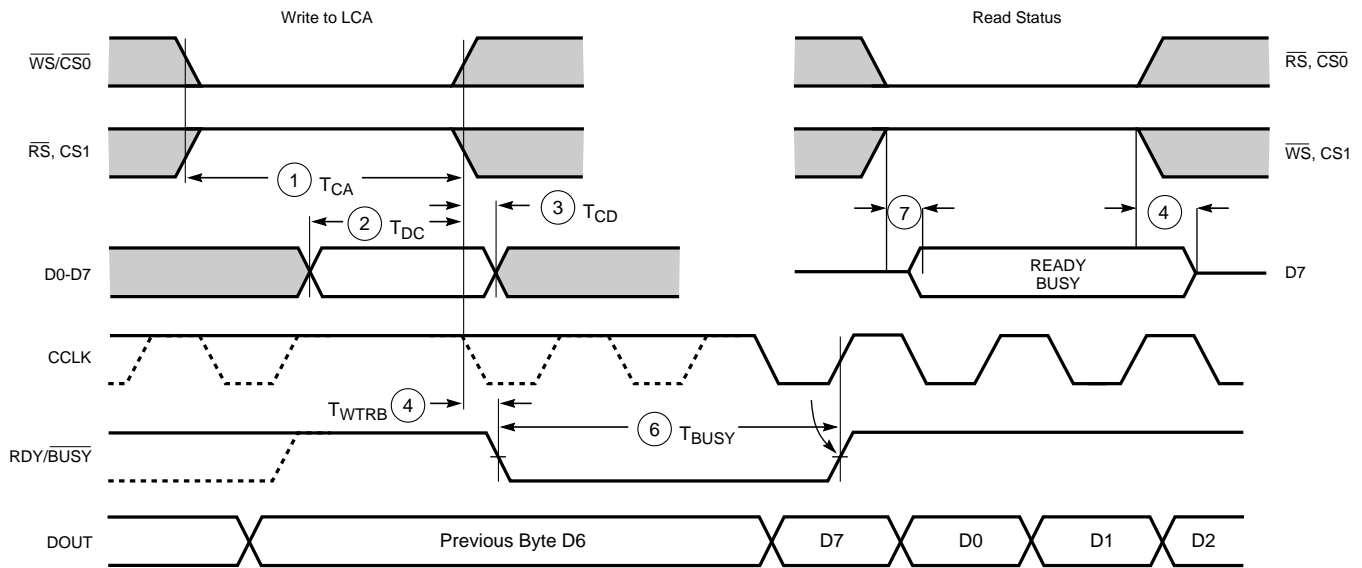
In order to complete the serial shift operation, 10 additional CCLK rising edges are required after the last data byte has been loaded, plus one more CCLK cycle for each daisy-chained device.

Synchronous Peripheral mode is selected by a <011> on the mode pins (M2, M1, M0).



X9027

Figure 56: Synchronous Peripheral Mode Circuit Diagram



X6097

| | Description | Symbol | Min | Max | Units |
|-------|--------------------------------------------------|--------------|-----|-----|--------------|
| Write | Effective Write time (CS0, WS=Low; RS, CS1=High) | 1 T_{CA} | 100 | | ns |
| | DIN setup time | 2 T_{DC} | 60 | | ns |
| | DIN hold time | 3 T_{CD} | 0 | | ns |
| RDY | RDY/BUSY delay after end of Write or Read | 4 T_{WTRB} | | 60 | ns |
| | RDY/BUSY active after beginning of Read | 7 | | 60 | ns |
| | RDY/BUSY Low output (Note 4) | 6 T_{BUSY} | 2 | 9 | CCLK periods |

- Notes:
1. Configuration must be delayed until the \overline{INIT} pins of all daisy-chained FPGAs are High.
 2. The time from the end of \overline{WS} to CCLK cycle for the new byte of data depends on the completion of previous byte processing and the phase of the internal timing generator for CCLK.
 3. CCLK and DOUT timing is tested in slave mode.
 4. T_{BUSY} indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest T_{BUSY} occurs when a byte is loaded into an empty parallel-to-serial converter. The longest T_{BUSY} occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

This timing diagram shows very relaxed requirements. Data need not be held beyond the rising edge of \overline{WS} . RDY/BUSY will go active within 60 ns after the end of \overline{WS} . A new write may be asserted immediately after RDY/BUSY goes Low, but write may not be terminated until RDY/BUSY has been High for one CCLK period.

Figure 59: Asynchronous Peripheral Mode Programming Switching Characteristics

Table 25: Component Availability Chart for XC4000E FPGAs

| | PINS | TYPE | CODE | 84 | 100 | 100 | 120 | 144 | 156 | 160 | 191 | 208 | 208 | 223 | 225 | 240 | 240 | 299 | 304 |
|---------|------|------|------|-------------|-------------|-------------|------------|-------------|------------|-------------|------------|----------------|-------------|------------|------------|----------------|-------------|------------|---------------|
| | | | | Plast. PLCC | Plast. PQFP | Plast. VQFP | Ceram. PGA | Plast. TQFP | Ceram. PGA | Plast. PQFP | Ceram. PGA | High-Perf. QFP | Plast. PQFP | Ceram. PGA | Plast. BGA | High-Perf. QFP | Plast. PQFP | Ceram. PGA | High-Perf. QF |
| | | | | PC84 | PQ100 | VQ100 | PG120 | TQ144 | PG156 | PQ160 | PG191 | HQ208 | PQ208 | PG223 | BG225 | HQ240 | PQ240 | PG299 | HQ304 |
| XC4003E | -4 | C I | C I | C I | C I | | | | | | | | | | | | | | |
| | -3 | C I | C I | C I | C I | | | | | | | | | | | | | | |
| | -2 | C I | C I | C I | C I | | | | | | | | | | | | | | |
| | -1 | C | C | C | C | | | | | | | | | | | | | | |
| XC4005E | -4 | C I | C I | | | | | C I | C I | C I | | | C I | | | | | | |
| | -3 | C I | C I | | | | | C I | C I | C I | | | C I | | | | | | |
| | -2 | C I | C I | | | | | C I | C I | C I | | | C I | | | | | | |
| | -1 | C | C | | | | | C | C | C | | | C | | | | | | |
| XC4006E | -4 | C I | | | | | | C I | C I | C I | | | C I | | | | | | |
| | -3 | C I | | | | | | C I | C I | C I | | | C I | | | | | | |
| | -2 | C I | | | | | | C I | C I | C I | | | C I | | | | | | |
| | -1 | C | | | | | | C | C | C | | | C | | | | | | |
| XC4008E | -4 | C I | | | | | | | | C I | C I | | C I | | | | | | |
| | -3 | C I | | | | | | | | C I | C I | | C I | | | | | | |
| | -2 | C I | | | | | | | | C I | C I | | C I | | | | | | |
| | -1 | C | | | | | | | | C | C | | C | | | | | | |
| XC4010E | -4 | C I | | | | | | | | C I | C I | C I | C I | | | C I | | | |
| | -3 | C I | | | | | | | | C I | C I | C I | C I | | | C I | | | |
| | -2 | C I | | | | | | | | C I | C I | C I | C I | | | C I | | | |
| | -1 | C | | | | | | | | C | C | C | C | | | C | | | |
| XC4013E | -4 | | | | | | | | | C I | | C I | C I | C I | C I | C I | C I | | |
| | -3 | | | | | | | | | C I | | C I | C I | C I | C I | C I | C I | | |
| | -2 | | | | | | | | | C I | | C I | C I | C I | C I | C I | C I | | |
| | -1 | | | | | | | | | C | | C | C | C | C | C | C | | |
| XC4020E | -4 | | | | | | | | | | | C I | | C I | | C I | | | |
| | -3 | | | | | | | | | | | C I | | C I | | C I | | | |
| | -2 | | | | | | | | | | | C I | | C I | | C I | | | |
| | -1 | | | | | | | | | | | C | | C | | C | | | |
| XC4025E | -4 | | | | | | | | | | | | | C I | | C I | | C I | C I |
| | -3 | | | | | | | | | | | | | C I | | C I | | C I | C I |
| | -2 | | | | | | | | | | | | | C | | C | | C | C |

1/29/99

C = Commercial $T_J = 0^\circ$ to $+85^\circ\text{C}$

I = Industrial $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$

Table 26: Component Availability Chart for XC4000EX FPGAs

| | PINS | TYPE | CODE | 208 | 240 | 299 | 304 | 352 | 411 | 432 |
|----------|------|------|------|----------------|----------------|------------|----------------|------------|------------|------------|
| | | | | High-Perf. QFP | High-Perf. QFP | Ceram. PGA | High-Perf. QFP | Plast. BGA | Ceram. PGA | Plast. BGA |
| | | | | HQ208 | HQ240 | PG299 | HQ304 | BG352 | PG411 | BG432 |
| XC4028EX | -4 | C I | C I | C I | C I | C I | C I | C I | | |
| | -3 | C I | C I | C I | C I | C I | C I | C I | | |
| | -2 | C | C | C | C | C | C | C | | |
| XC4036EX | -4 | | | C I | C I | | C I | C I | C I | C I |
| | -3 | | | C I | C I | | C I | C I | C I | C I |
| | -2 | | | C | C | | C | C | C | C |

1/29/99

C = Commercial $T_J = 0^\circ$ to $+85^\circ\text{C}$

I = Industrial $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$

User I/O Per Package

Table 27, Table 28, and Table 29 show the number of user I/Os available in each package for XC4000-Series devices. Call your local sales office for the latest availability information, or see the Xilinx website at <http://www.xilinx.com> for the latest revision of the specifications.

Table 27: User I/O Chart for XC4000XL FPGAs

| Device | Max I/O | Maximum User Accessible I/O by Package Type | | | | | | | | | | | | | | | | | | | | | |
|----------|---------|---------------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| | | PC84 | PQ100 | VQ100 | TQ144 | HT144 | HQ160 | PQ160 | TQ176 | HT176 | HQ208 | PQ208 | HQ240 | PQ240 | BG256 | PG299 | HQ304 | BG352 | PG411 | BG432 | PG475 | PG559 | BG560 |
| XC4002XL | 64 | 61 | 64 | 64 | | | | | | | | | | | | | | | | | | | |
| XC4005XL | 112 | 61 | 77 | 77 | 112 | | | 112 | | | 112 | | | | | | | | | | | | |
| XC4010XL | 160 | 61 | 77 | | 113 | | | 129 | 145 | | 160 | | | 160 | | | | | | | | | |
| XC4013XL | 192 | | | | | 113 | | 129 | | 145 | | 160 | | 192 | 192 | | | | | | | | |
| XC4020XL | 224 | | | | | 113 | | 129 | | 145 | | 160 | | 192 | 205 | | | | | | | | |
| XC4028XL | 256 | | | | | | 129 | | | | 160 | | 193 | | 205 | 256 | 256 | 256 | | | | | |
| XC4036XL | 288 | | | | | | 129 | | | | 160 | | 193 | | | | 256 | 288 | 288 | 288 | | | |
| XC4044XL | 320 | | | | | | 129 | | | | 160 | | 193 | | | | 256 | 289 | 320 | 320 | | | |
| XC4052XL | 352 | | | | | | | | | | | 193 | | | | | 256 | | 352 | 352 | | | 352 |
| XC4062XL | 384 | | | | | | | | | | | 193 | | | | | 256 | | | 352 | 384 | | 384 |
| XC4085XL | 448 | | | | | | | | | | | | | | | | | | | 352 | | 448 | 448 |

1/29/99

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Table 28: User I/O Chart for XC4000E FPGAs

| Device | Max I/O | Maximum User Accessible I/O by Package Type | | | | | | | | | | | | | | | |
|---------|---------|---------------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| | | PC84 | PQ100 | VQ100 | PG120 | TQ144 | PG156 | PQ160 | PG191 | HQ208 | PQ208 | PG223 | BG225 | HQ240 | PQ240 | PG299 | HQ304 |
| XC4003E | 80 | 61 | 77 | 77 | 80 | | | | | | | | | | | | |
| XC4005E | 112 | 61 | 77 | | | 112 | 112 | 112 | | | 112 | | | | | | |
| XC4006E | 128 | 61 | | | | 113 | 125 | 128 | | | 128 | | | | | | |
| XC4008E | 144 | 61 | | | | | | 129 | 144 | | 144 | | | | | | |
| XC4010E | 160 | 61 | | | | | | 129 | 160 | 160 | 160 | | 160 | | | | |
| XC4013E | 192 | | | | | | | 129 | | 160 | 160 | 192 | 192 | 192 | 192 | | |
| XC4020E | 224 | | | | | | | | | 160 | | 192 | | 193 | | | |
| XC4025E | 256 | | | | | | | | | | | 192 | | 193 | | 256 | 256 |

1/29/99

Table 29: User I/O Chart for XC4000EX FPGAs

| Device | Max I/O | Maximum User Accessible I/O by Package Type | | | | | | |
|----------|---------|---------------------------------------------|-------|-------|-------|-------|-------|-------|
| | | HQ208 | HQ240 | PG299 | HQ304 | BG352 | PG411 | BG432 |
| XC4028EX | 256 | 160 | 193 | 256 | 256 | 256 | | |
| XC4036EX | 288 | | 193 | | 256 | 288 | 288 | 288 |

1/29/99