E·XFL

XMOS - XU232-1024-FB374-C40 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	YCoro
Core Size	32-Bit 32-Core
Speed	4000MIPS
Connectivity	USB
Peripherals	-
Number of I/O	176
Program Memory Size	-
Program Memory Type	ROMIess
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	0.95V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	324-FBGA
Supplier Device Package	324-FBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xu232-1024-fb374-c40

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table of Contents

1	xCORE Multicore Microcontrollers	2
2	XU232-1024-FB374 Features	5
3	Pin Configuration	6
4	Signal Description	7
5	Example Application Diagram	3
6	Product Overview	4
7	PLL	7
8	Boot Procedure	8
9	Memory	1
10	USB PHY	3
11	JTAG	4
12	Board Integration	5
13	DC and Switching Characteristics	9
14	Package Information	3
15	Ordering Information	4
App	endices	5
A	Configuration of the XU232-1024-FB374	5
В	Processor Status Configuration	8
С	Tile Configuration	9
D	Node Configuration	7
E	USB Node Configuration	5
F	USB PHY Configuration	7
G	JTAG, xSCOPE and Debugging	4
н	Schematics Design Check List	6
1	PCB Layout Design Check List	8
J	Associated Design Documentation	9
K	Related Documentation	9
L	Revision History	0

TO OUR VALUED CUSTOMERS

It is our intention to provide you with accurate and comprehensive documentation for the hardware and software components used in this product. To subscribe to receive updates, visit http://www.xmos.com/.

XMOS Ltd. is the owner or licensee of the information in this document and is providing it to you "AS IS" with no warranty of any kind, express or implied and shall have no liability in relation to its use. XMOS Ltd. makes no representation that the information, or any particular implementation thereof, is or will be free from any claims of infringement and again, shall have no liability in relation to any such claims.

XMOS and the XMOS logo are registered trademarks of XMOS Ltd in the United Kingdom and other countries, and may not be used without written permission. Company and product names mentioned in this document are the trademarks or registered trademarks of their respective owners.

2 XU232-1024-FB374 Features

► Multicore Microcontroller with Advanced Multi-Core RISC Architecture

- 32 real-time logical cores on 4 xCORE tiles
- Cores share up to 2000 MIPS
 - Up to 4000 MIPS in dual issue mode
- Each logical core has:
 - Guaranteed throughput of between 1/5 and 1/8 of tile MIPS
 - 16x32bit dedicated registers
- 167 high-density 16/32-bit instructions
 - All have single clock-cycle execution (except for divide)
 - 32x32 ${\rightarrow}64$ bit MAC instructions for DSP, arithmetic and user-definable cryptographic functions

▶ Dual USB PHY, fully compliant with USB 2.0 specification

Programmable I/O

- 176 general-purpose I/O pins, configurable as input or output
 - Up to 56 x 1bit port, 22 x 4bit port, 13 x 8bit port, 6 x 16bit port, 4 x 32bit port
 8 xCONNECT links
- Port sampling rates of up to 60 MHz with respect to an external clock
- 128 channel ends (32 per tile) for communication with other cores, on or off-chip

Memory

- 1024KB internal single-cycle SRAM (max 256KB per tile) for code and data storage
- 32KB internal OTP (max 8KB per tile) for application boot code

Hardware resources

- 24 clock blocks (6 per tile)
- 40 timers (10 per tile)
- 16 locks (4 per tile)
- JTAG Module for On-Chip Debug

Security Features

• Programming lock disables debug and prevents read-back of memory contents

-XM()S

• AES bootloader ensures secrecy of IP held on external flash memory

Ambient Temperature Range

- Commercial qualification: 0°C to 70°C
- Industrial qualification: -40 °C to 85 °C
- Speed Grade
 - 40: 2000 MIPS
- Power Consumption
 - 1140 mA (typical)
- ▶ 374-pin FBGA package 0.8 mm pitch

4 Signal Description

This section lists the signals and I/O pins available on the XU232-1024-FB374. The device provides a combination of 1 bit, 4bit, 8bit and 16bit ports, as well as wider ports that are fully or partially (gray) bonded out. All pins of a port provide either output or input, but signals in different directions cannot be mapped onto the same port.

Pins may have one or more of the following properties:

- PD/PU: The IO pin has a weak pull-down or pull-up resistor. On GPIO pins this resistor can be enabled. This resistor is designed to ensure defined logic input state for unconnected pins. It should not be used to pull external circuitry. Note that the resistors are highly non-linear and only a maximum pull current is specified in Section 13.2.
- ST: The IO pin has a Schmitt Trigger on its input.
- ▶ IOT: The IO pin is powered from VDDIOT (X1) or VDDIOT_2 (X3), not VDDIO

	IO:	the	pin	is	powered	from	VDDIO
--	-----	-----	-----	----	---------	------	-------

	Power pins (12)					
Signal	Function	Туре	Properties			
GND	Digital ground	GND				
OTP_VCC	OTP power supply	PWR				
PLL_AGND	Analog ground for PLL	PWR				
PLL_AVDD	Analog PLL power	PWR				
USB_2_VDD	Digital tile power	PWR				
USB_2_VDD33	USB Analog power	PWR				
USB_VDD	Digital tile power	PWR				
USB_VDD33	USB Analog power	PWR				
VDD	Digital tile power	PWR				
VDDIO	Digital I/O power	PWR				
VDDIOT	Digital I/O power (top)	PWR				
VDDIOT_2	Digital I/O power (top, X3)	PWR				

	JTAG pins (6)				
Signal	Function	Туре	Properties		
RST_N	Global reset input	Input	IO, PU, ST		
ТСК	Test clock	Input	IO, PD, ST		
TDI	Test data input	Input	IO, PU		
TDO	Test data output	Output	IO, PD		
TMS	Test mode select	Input	IO, PU		
TRST_N	Test reset input	Input	IO, PU, ST		

XU232-1024-FB374 Datasheet

Signal	Function	Туре	Properties
X3D32	4E ² 8C ⁶ 16B ⁶	I/O	IOT, PD
X3D33	4E ³ 8C ⁷ 16B ⁷	I/O	IOT, PD
X3D40	8D ⁴ 16B ¹²	I/O	IOT, PD
X3D41	8D ⁵ 16B ¹³	I/O	IOT, PD
X3D42	8D ⁶ 16B ¹⁴	I/O	IOT, PD
X3D43	8D ⁷ 16B ¹⁵	I/O	IOT, PD

System pins (4)					
Signal	Function	Туре	Properties		
CLK	PLL reference clock	Input	IO, PD, ST		
DEBUG_N	Multi-chip debug	I/O	IO, PU		
MODE0	Boot mode select	Input	PU		
MODE1	Boot mode select	Input	PU		

	usb pins (10)					
Signal	Function	Туре	Properties			
USB_2_DM	USB Serial Data Inverted, node 2	I/O				
USB_2_DP	USB Serial Data, node 2	I/O				
USB_2_ID	USB Device ID (OTG) - Reserved, node 2	I/O				
USB_2_RTUNE	USB resistor, node 2	I/O				
USB_2_VBUS	USB Power Detect Pin, node 2	I/O				
USB_DM	USB Serial Data Inverted	I/O				
USB_DP	USB Serial Data	I/O				
USB_ID	USB Device ID (OTG) - Reserved	I/O				
USB_RTUNE	USB resistor	I/O				
USB_VBUS	USB Power Detect Pin	I/O				

-XMOS[®]-



ports are available. All pins of a port provide either output or input. Signals in different directions cannot be mapped onto the same port.

The port logic can drive its pins high or low, or it can sample the value on its pins, optionally waiting for a particular condition. Ports are accessed using dedicated instructions that are executed in a single processor cycle. xCORE-200 IO pins can be used as *open collector* outputs, where signals are driven low if a zero is output, but left high impedance if a one is output. This option is set on a per-port basis.

Data is transferred between the pins and core using a FIFO that comprises a SERDES and transfer register, providing options for serialization and buffered data.

Each port has a 16-bit counter that can be used to control the time at which data is transferred between the port value and transfer register. The counter values can be obtained at any time to find out when data was obtained, or used to delay I/O until some time in the future. The port counter value is automatically saved as a timestamp, that can be used to provide precise control of response times.

The ports and xCONNECT links are multiplexed onto the physical pins. If an xConnect Link is enabled, the pins of the underlying ports are disabled. If a port is enabled, it overrules ports with higher widths that share the same pins. The pins on the wider port that are not shared remain available for use when the narrower port is enabled. Ports always operate at their specified width, even if they share pins with another port.

6.4 Clock blocks

xCORE devices include a set of programmable clocks called clock blocks that can be used to govern the rate at which ports execute. Each xCORE tile has six clock blocks: the first clock block provides the tile reference clock and runs at a default frequency of 100MHz; the remaining clock blocks can be set to run at different frequencies.

-XM()S

XS2-U32A-1024-FB374



A clock block can use a 1-bit port as its clock source allowing external application clocks to be used to drive the input and output interfaces. xCORE-200 clock blocks optionally divide the clock input from a 1-bit port.

In many cases I/O signals are accompanied by strobing signals. The xCORE ports can input and interpret strobe (known as readyIn and readyOut) signals generated by external sources, and ports can generate strobe signals to accompany output data.

On reset, each port is connected to clock block 0, which runs from the xCORE Tile reference clock.

6.5 Channels and Channel Ends

Logical cores communicate using point-to-point connections, formed between two channel ends. A channel-end is a resource on an xCORE tile, that is allocated by the program. Each channel-end has a unique system-wide identifier that comprises a unique number and their tile identifier. Data is transmitted to a channel-end by an output-instruction; and the other side executes an input-instruction. Data can be passed synchronously or asynchronously between the channel ends.

6.6 xCONNECT Switch and Links

XMOS devices provide a scalable architecture, where multiple xCORE devices can be connected together to form one system. Each xCORE device has an xCONNECT interconnect that provides a communication infrastructure for all tasks that run on the various xCORE tiles on the system.

The interconnect relies on a collection of switches and XMOS links. Each xCORE device has an on-chip switch that can set up circuits or route data. The switches are connected by xConnect Links. An XMOS link provides a physical connection between two switches. The switch has a routing algorithm that supports many different topologies, including lines, meshes, trees, and hypercubes.

The links operate in either 2 wires per direction or 5 wires per direction mode, depending on the amount of bandwidth required. Circuit switched, streaming



8.1 Boot from QSPI master

If set to boot from QSPI master, the processor enables the six pins specified in Figure 10, and drives the SPI clock at 50 MHz (assuming a 400 MHz core clock). A READ command is issued with a 24-bit address 0x000000. The clock polarity and phase are 0 / 0.

	Pin	Signal	Description
	X0D01	SS	Slave Select
Figure 10:	X0D04X0D07	SPIO	Data
QSPI pins	X0D10	SCLK	Clock

-XMOS[®]

The xCORE Tile expects each byte to be transferred with the *least-significant nibble* first. Programmers who write bytes into an QSPI interface using the most significant nibble first may have to reverse the nibbles in each byte of the image stored in the OSPI device.

possible. A bulk decoupling capacitor of at least 10 uF should be placed on each of these supplies.

RST_N is an active-low asynchronous-assertion global reset signal. Following a reset, the PLL re-establishes lock after which the device boots up according to the boot mode (*see* §8). RST_N and must be asserted low during and after power up for 100 ns.

12.1 USB connections

USB_VBUS should be connected to the VBUS pin of the USB connector. A 2.2 μ F capacitor to ground is required on the VBUS pin. A ferrite bead may be used to reduce HF noise.

For self-powered systems, a bleeder resistor may be required to stop VBUS from floating when no USB cable is attached.

USB_DP and USB_DN should be connected to the USB connector. USB_ID does not need to be connected.

12.2 USB signal routing and placement

The USB_DP and USB_DN lines are the positive and negative data polarities of a high speed USB signal respectively. Their high-speed differential nature implies that they must be coupled and properly isolated. The board design must ensure that the board traces for USB_DP and USB_DN are tightly matched. In addition, according to the USB 2.0 specification, the USB_DP and USB_DN differential impedance must be 90 Ω .



12.2.1 General routing and placement guidelines

The following guidelines will help to avoid signal quality and EMI problems on high speed USB designs. They relate to a four-layer (Signal, GND, Power, Signal) PCB.

For best results, most of the routing should be done on the top layer (assuming the USB connector and XS2-U32A-1024-FB374 are on the top layer) closest to GND. Reference planes should be below the transmission lines in order to maintain control of the trace impedance.

I/O AC

	Symbol	Parameter	MIN	ТҮР	MAX	UNITS	Notes
	T(XOVALID)	Input data valid window	8			ns	
Figure 27: O AC char- acteristics	T(XOINVALID)	0) Output data invalid window				ns	
	T(XIFMAX)	Rate at which data can be sampled with respect to an external clock			60	MHz	

13.7 xCORE Tile I/O AC Cha	racteristics
----------------------------	--------------

The input valid window parameter relates to the capability of the device to capture data input to the chip with respect to an external clock source. It is calculated as the sum of the input setup time and input hold time with respect to the external clock as measured at the pins. The output invalid window specifies the time for which an output is invalid with respect to the external clock. Note that these parameters are specified as a window rather than absolute numbers since the device provides functionality to delay the incoming clock with respect to the incoming data.

Information on interfacing to high-speed synchronous interfaces can be found in the XS1 Port I/O Timing document, X5821.

13.8 xConnect Link Performance

	Symbol	Parameter	MIN	ТҮР	MAX	UNITS	Notes
	B(2blinkP)	2b link bandwidth (packetized)			87	MBit/s	A, B
Figure 28:	B(5blinkP)	5b link bandwidth (packetized)			217	MBit/s	A, B
Link	B(2blinkS)	2b link bandwidth (streaming)			100	MBit/s	В
performance	B(5blinkS)	5b link bandwidth (streaming)			250	MBit/s	В

A Assumes 32-byte packet in 3-byte header mode. Actual performance depends on size of the header and payload.

B 7.5 ns symbol time.

The asynchronous nature of links means that the relative phasing of CLK clocks is not important in a multi-clock system, providing each meets the required stability criteria.

1	30	ITAC	Timina
	3.9	JIAU	rinning

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
f(TCK_D)	TCK frequency (debug)			18	MHz	
f(TCK_B)	TCK frequency (boundary scan)			10	MHz	
T(SETUP)	TDO to TCK setup time	5			ns	А
T(HOLD)	TDO to TCK hold time	5			ns	А
T(DELAY)	TCK to output delay			15	ns	В

Figure 29 JTAG timing

A Timing applies to TMS and TDI inputs.

B Timing applies to TDO output from negative edge of TCK.

All JTAG operations are synchronous to TCK apart from the global asynchronous reset TRST_N.

-XM()S

B Processor Status Configuration

The processor status control registers can be accessed directly by the processor using processor status reads and writes (use getps(reg) and setps(reg,value) for reads and writes).

Number	Perm	Description	
0x00	RW	RAM base address	
0x01	RW	Vector base address	
0x02	RW	xCORE Tile control	
0x03	RO	xCORE Tile boot status	
0x05	RW	Security configuration	
0x06	RW	Ring Oscillator Control	
0x07	RO	Ring Oscillator Value	
0x08	RO	Ring Oscillator Value	
0x09	RO	Ring Oscillator Value	
0x0A	RO	Ring Oscillator Value	
0x0C	RO	RAM size	
0x10	DRW	Debug SSR	
0x11	DRW	Debug SPC	
0x12	DRW	Debug SSP	
0x13	DRW	DGETREG operand 1	
0x14	DRW	DGETREG operand 2	
0x15	DRW	Debug interrupt type	
0x16	DRW	Debug interrupt data	
0x18	DRW	Debug core control	
0x20 0x27	DRW	Debug scratch	
0x30 0x33	DRW	Instruction breakpoint address	
0x40 0x43	DRW	Instruction breakpoint control	
0x50 0x53	DRW	Data watchpoint address 1	
0x60 0x63	DRW	Data watchpoint address 2	
0x70 0x73	DRW	Data breakpoint control register	
0x80 0x83	DRW	Resources breakpoint mask	
0x90 0x93	DRW	Resources breakpoint value	
0x9C 0x9F	DRW	Resources breakpoint control register	

-XMOS

Figure 33:

Summary

XS2-U32A-1024-FB374

B.5 Security configuration: 0x05

Bits	Perm	Init	Description
31	RW		Disables write permission on this register
30:15	RO	-	Reserved
14	RW		Disable access to XCore's global debug
13	RO	-	Reserved
12	RW		lock all OTP sectors
11:8	RW		lock bit for each OTP sector
7	RW		Enable OTP reduanacy
6	RO	-	Reserved
5	RW		Override boot mode and read boot image from OTP
4	RW		Disable JTAG access to the PLL/BOOT configuration registers
3:1	RO	-	Reserved
0	RW		Disable access to XCore's JTAG debug TAP

Copy of the security register as read from OTP.

0x05: Security configuration

B.6 Ring Oscillator Control: 0x06

There are four free-running oscillators that clock four counters. The oscillators can be started and stopped using this register. The counters should only be read when the ring oscillator has been stopped for at least 10 core clock cycles (this can be achieved by inserting two nop instructions between the SETPS and GETPS). The counter values can be read using four subsequent registers. The ring oscillators are asynchronous to the xCORE tile clock and can be used as a source of random bits.

0x06: Ring Oscillator Control

Bits	Perm	Init	Description
31:2	RO	-	Reserved
1	RW	0	Core ring oscillator enable.
0	RW	0	Peripheral ring oscillator enable.

B.7 Ring Oscillator Value: 0x07

This register contains the current count of the xCORE Tile Cell ring oscillator. This value is not reset on a system reset.

-XMOS-

0	x0C
RAM	size

	Bits	Perm	Init	Description
x0C:	31:2	RO		Most significant 16 bits of all addresses.
size	1:0	RO	-	Reserved

B.12 Debug SSR: 0x10

This register contains the value of the SSR register when the debugger was called.

Bits	Perm	Init	Description
31:11	RO	-	Reserved
10	DRW		Address space indentifier
9	DRW		Determines the issue mode (DI bit) upon Kernel Entry after Exception or Interrupt.
8	RO		Determines the issue mode (DI bit).
7	DRW		When 1 the thread is in fast mode and will continually issue.
6	DRW		When 1 the thread is paused waiting for events, a lock or another resource.
5	RO	-	Reserved
4	DRW		1 when in kernel mode.
3	DRW		1 when in an interrupt handler.
2	DRW		1 when in an event enabling sequence.
1	DRW		When 1 interrupts are enabled for the thread.
0	DRW		When 1 events are enabled for the thread.

0x10: Debug SSR

B.13 Debug SPC: 0x11

This register contains the value of the SPC register when the debugger was called.

0x11:	Bits	Perm	Init	Description
Debug SPC	31:0	DRW		Value.

-XMOS"-

B.14 Debug SSP: 0x12

This register contains the value of the SSP register when the debugger was called.

43

B.18 Debug interrupt data: 0x16

On a data watchpoint, this register contains the effective address of the memory operation that triggered the debugger. On a resource watchpoint, it countains the resource identifier.

0x16: Debug interrupt data

16: oug	Bits	Perm	Init	Description
ata	31:0	DRW		Value.

B.19 Debug core control: 0x18

This register enables the debugger to temporarily disable logical cores. When returning from the debug interrupts, the cores set in this register will not execute. This enables single stepping to be implemented.

0x18: Debug core control

Bits	Perm	Init	Description
31:8	RO	-	Reserved
7:0	DRW		1-hot vector defining which threads are stopped when not in debug mode. Every bit which is set prevents the respective thread from running.

B.20 Debug scratch: 0x20 .. 0x27

A set of registers used by the debug ROM to communicate with an external debugger, for example over JTAG. This is the same set of registers as the Debug Scratch registers in the xCORE tile configuration.

0x20 .. 0x27: Debug scratch

ebug	Bits	Perm	Init	Description
atch	31:0	DRW		Value.

B.21 Instruction breakpoint address: 0x30 .. 0x33

-XM()S

This register contains the address of the instruction breakpoint. If the PC matches this address, then a debug interrupt will be taken. There are four instruction breakpoints that are controlled individually.



0x30 .. 0x33: Instruction breakpoint address

oint	Bits	Perm	Init	Description
ress	31:0	DRW		Value.

B.22 Instruction breakpoint control: 0x40 .. 0x43

This register controls which logical cores may take an instruction breakpoint, and under which condition.

	Bits	Perm	Init	Description
	31:24	RO	-	Reserved
	23:16	DRW	0	A bit for each thread in the machine allowing the breakpoint to be enabled individually for each thread.
<u>.</u>	15:2	RO	-	Reserved
7. 1 t	1	DRW	0	When 0 break when PC == IBREAK_ADDR. When 1 = break when PC != IBREAK_ADDR.
	0	DRW	0	When 1 the instruction breakpoint is enabled.

0x40 .. 0x43 Instruction breakpoint control

B.23 Data watchpoint address 1: 0x50 ... 0x53

This set of registers contains the first address for the four data watchpoints.

0x50 0x53:				
watchpoint	Bits	Perm	Init	Description
address 1	31:0	DRW		Value.

B.24 Data watchpoint address 2: 0x60 .. 0x63

This set of registers contains the second address for the four data watchpoints.

0x60 0x63:				
watchpoint	Bits	Perm	Init	Description
address 2	31:0	DRW		Value.

-

B.25 Data breakpoint control register: 0x70 ... 0x73

This set of registers controls each of the four data watchpoints.

Bits	Perm	Init	Description
31:24	RO	-	Reserved
23:16	DRW	0	A bit for each thread in the machine allowing the breakpoint to be enabled individually for each thread.
15:3	RO	-	Reserved
2	DRW	0	When 1 the breakpoints will be be triggered on loads.
1	DRW	0	Determines the break condition: $0 = A AND B$, $1 = A OR B$.
0	DRW	0	When 1 the instruction breakpoint is enabled.

0x70 .. 0x73: Data breakpoint control register

B.26 Resources breakpoint mask: 0x80 .. 0x83

This set of registers contains the mask for the four resource watchpoints.

0x80 .. 0x83: Resources breakpoint mask

urces point	Bits	Perm	Init	Description
mask	31:0	DRW		Value.

B.27 Resources breakpoint value: 0x90 .. 0x93

This set of registers contains the value for the four resource watchpoints.

0x90 .. 0x93: Resources breakpoint value

ces oint	Bits	Perm	Init	Description
ເlue	31:0	DRW		Value.

B.28 Resources breakpoint control register: 0x9C .. 0x9F

This set of registers controls each of the four resource watchpoints.

-XMOS

XS2-U32A-1024-FB374

0x04: Control PSwitch permissions to debug registers

Bits	Perm	Init	Description
31	CRW	0	When 1 the PSwitch is restricted to RO access to all CRW registers from SSwitch, XCore(PS_DBG_Scratch) and JTAG
30:1	RO	-	Reserved
0	CRW	0	When 1 the PSwitch is restricted to RO access to all CRW registers from SSwitch

C.5 Cause debug interrupts: 0x05

This register can be used to raise a debug interrupt in this xCORE tile.

0x05: Cause debug interrupts

Bits	Perm	Init	Description
31:2	RO	-	Reserved
1	CRW	0	1 when the processor is in debug mode.
0	CRW	0	Request a debug interrupt on the processor.

C.6 xCORE Tile clock divider: 0x06

This register contains the value used to divide the PLL clock to create the xCORE tile clock. The divider is enabled under control of the tile control register

0x06: xCORE Tile clock divider

Bits	Perm	Init	Description
31	CRW	0	Clock disable. Writing '1' will remove the clock to the tile.
30:16	RO	-	Reserved
15:0	CRW	0	Clock divider.

C.7 Security configuration: 0x07

Copy of the security register as read from OTP.

-XMOS

51

	Bits	Perm	Init	Description
	31	CRO		Disables write permission on this register
	30:15	RO	-	Reserved
	14	CRO		Disable access to XCore's global debug
	13	RO	-	Reserved
	12	CRO		lock all OTP sectors
	11:8	CRO		lock bit for each OTP sector
	7	CRO		Enable OTP reduanacy
	6	RO	-	Reserved
	5	CRO		Override boot mode and read boot image from OTP
	4	CRO		Disable JTAG access to the PLL/BOOT configuration registers
,	3:1	RO	-	Reserved
1	0	CRO		Disable access to XCore's JTAG debug TAP

0x07 Security configuration

C.8 Debug scratch: 0x20 .. 0x27

A set of registers used by the debug ROM to communicate with an external debugger, for example over the switch. This is the same set of registers as the Debug Scratch registers in the processor status.

0x20 .. 0x27 Debug scratch

ebug	Bits	Perm	Init	Description
atch	31:0	CRW		Value.

C.9 PC of logical core 0: 0x40

Value of the PC of logical core 0.

0x40 PC of logical core 0

ical	Bits	Perm	Init	Description
re 0	31:0	CRO		Value.

-XMOS

C.10 PC of logical core 1: 0x41

Value of the PC of logical core 1.



	Bits	Perm	Init	Description	
	31:28	RW	0	The direction for packets whose dimension is F.	
	27:24	RW	0	The direction for packets whose dimension is E.	
	23:20	RW	0	The direction for packets whose dimension is D.	
19:16 RW 0 The direction for packets wh		The direction for packets whose dimension is C.			
	15:12	RW	0	The direction for packets whose dimension is B.	
	11:8	RW	0	The direction for packets whose dimension is A.	
Directions	7:4	RW	0	The direction for packets whose dimension is 9.	
8-15	3:0	RW	0	The direction for packets whose dimension is 8.	

D.12 DEBUG_N configuration, tile 0: 0x10

Configures the behavior of the DEBUG_N pin.

0x1 DEBUG_N co figuratio tile

_	Bits	Perm	Init	Description
0: p	31:2	RO	-	Reserved
n,	1	RW	0	Set 1 to enable GlobalDebug to generate debug request to XCore.
0	0	RW	0	Set 1 to enable inDebug bit to drive GlobalDebug.

D.13 DEBUG_N configuration, tile 1: 0x11

Configures the behavior of the DEBUG_N pin.

0x1 DEBUG_N co figuratio tile

-	Bits	Perm	Init	Description
1:	31:2	RO	-	Reserved
n,	1	RW	0	Set 1 to enable GlobalDebug to generate debug request to XCore.
1	0	RW	0	Set 1 to enable inDebug bit to drive GlobalDebug.

D.14 Debug source: 0x1F

Contains the source of the most recent debug event.

 $\cdot X MOS$

D.18 Static link configuration: 0xA0 .. 0xA7

These registers are used for static (ie, non-routed) links. When a link is made static, all traffic is forwarded to the designated channel end and no routing is attempted. The registers control links C, D, A, B, G, H, E, and F in that order.

Bits	Perm	Init	Description
31	RW	0	Enable static forwarding.
30:9	RO	-	Reserved
8	RW	0	The destination processor on this node that packets received in static mode are forwarded to.
7:5	RO	-	Reserved
4:0	RW	0	The destination channel end on this node that packets received in static mode are forwarded to.

0xA0 .. 0xA7: Static link configuration



J Associated Design Documentation

Document Title	Information	Document Number
Estimating Power Consumption For XS1-U Devices	Power consumption	
Programming XC on XMOS Devices	Timers, ports, clocks, cores and channels	X9577
xTIMEcomposer User Guide	Compilers, assembler and linker/mapper	X3766
	Timing analyzer, xScope, debugger	
	Flash and OTP programming utilities	

K Related Documentation

Document Title	Information	Document Number
The XMOS XS1 Architecture	ISA manual	X7879
XS1 Port I/O Timing	Port timings	X5821
xCONNECT Architecture	Link, switch and system information	X4249
XS1-U Link Performance and Design Guidelines	Link timings	
XS1-U Clock Frequency Control	Advanced clock control	