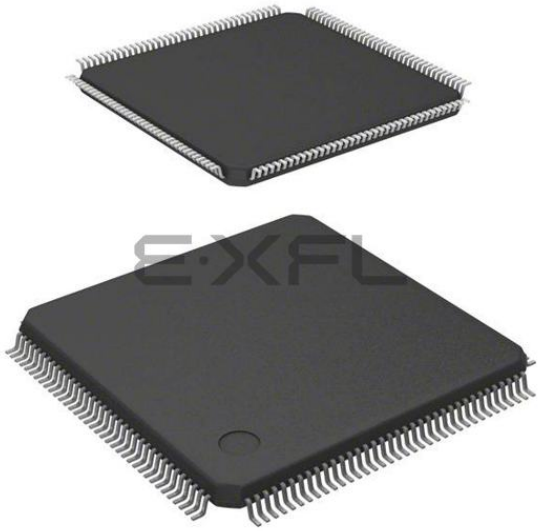

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	64MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	68K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	144-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f276z5q3

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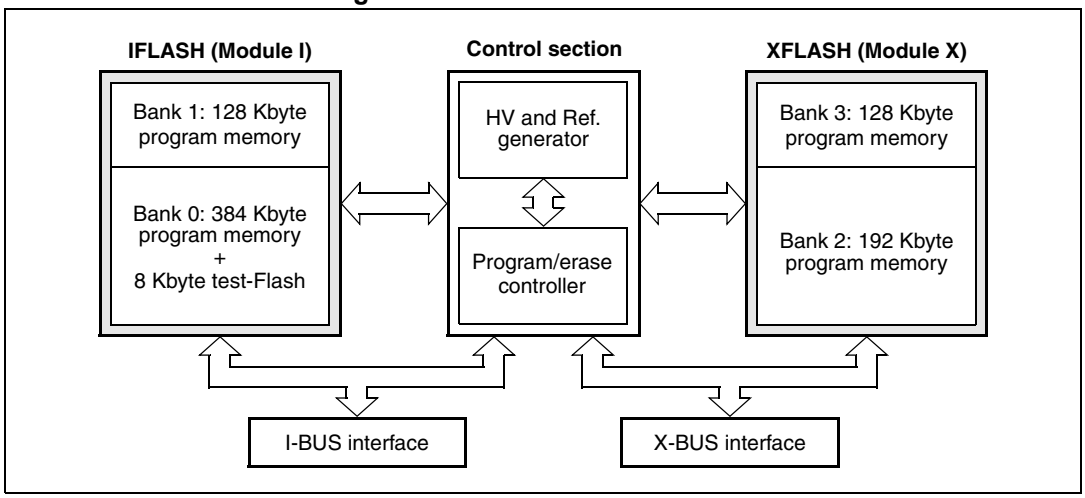
4 Internal Flash memory

4.1 Overview

The on-chip Flash is composed by two matrix modules each one containing one array divided in two banks that can be read and modified independently one of the other: one bank can be read while another bank is under modification.

Figure 4. Flash modules structure



The write operations of the 4 banks are managed by an embedded Flash program/erase controller (FPEC). The high voltages needed for program/erase operations are internally generated.

The data bus is 32-bit wide. Due to ST10 core architecture limitation, only the first 512 Kbytes are accessed at 32-bit (internal Flash bus, see I-BUS), while the remaining 320 Kbytes are accessed at 16-bit (see X-BUS).

4.2 Functional description

4.2.1 Structure

The following table shows the address space reserved to the Flash module.

Table 3. Flash modules absolute mapping

Description	Addresses	Size
IFLASH sectors	0x00 0000 to 0x08 FFFF	512 Kbyte
XFLASH sectors	0x09 0000 to 0x0D FFFF	320 Kbyte
Registers and Flash internal reserved area	0x0E 0000 to 0x0E FFFF	64 Kbyte

write operation is active: the write operation commands must be executed from another Bank, or from the other module or again from another memory (internal RAM or external memory).

Note: During a Write operation, when bit LOCK of FCR0 is set, it is forbidden to write into the Flash Control Registers.

4.3.1 Power supply drop

If during a write operation the internal low voltage supply drops below a certain internal voltage threshold, any write operation running is suddenly interrupted and the modules are reset to Read mode. At following Power-on, an interrupted Flash write operation must be repeated.

4.4 Registers description

4.4.1 Flash control register 0 low

The Flash control register 0 low (FCR0L) together with the Flash control register 0 high (FCR0H) is used to enable and to monitor all the write operations for both the Flash modules. The user has no access in write mode to the test-Flash (B0TF). Besides, test-Flash block is seen by the user in Bootstrap mode only.

FCR0L (0x0E 0000) FCR Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved									BSY1	BSY0	LOCK	res.	BSY3	BSY2	res.
									R	R	R		R	R	

Table 7. Flash control register 0 low

Bit	Function
BSY(3:2)	Bank 3:2 Busy (XFLASH) These bits indicate that a write operation is running on the corresponding Bank of XFLASH. They are automatically set when bit WMS is set. Setting Protection operation sets bit BSY2 (since protection registers are in the Block B2). When these bits are set every read access to the corresponding Bank will output invalid data (software trap 009Bh), while every write access to the Bank will be ignored. At the end of the write operation or during a Program or Erase Suspend these bits are automatically reset and the Bank returns to read mode. After a Program or Erase Resume these bits are automatically set again.

4.4.3 Flash control register 1 low

The Flash control register 1 low (FCR1L), together with Flash control register 1 high (FCR1H), is used to select the sectors to erase, or during any write operation to monitor the status of each sector of the module selected by SMOD bit of FCR0H. First diagram shows FCR1L meaning when SMOD=0; the second one when SMOD=1.

FCR1L (0x0E 0004) SMOD=0 FCR Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													B2F2	B2F1	B2F0
													RS	RS	RS

FCR1L (0x0E 0004) SMOD=1 FCR Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						B0F9	B0F8	B0F7	B0F6	B0F5	B0F4	B0F3	B0F2	B0F1	B0F0
						RS	RS	RS	RS	RS	RS	RS	RS	RS	RS

Table 9. Flash control register 1 low

Bit	Function
SMOD=0 (XFLASH selected)	
B2F(2:0)	Bank 2 XFLASH sector 2:0 status These bits must be set during a Sector Erase operation to select the sectors to erase in bank 2. Besides, during any erase operation, these bits are automatically set and give the status of the 3 sectors of bank 2 (B2F2-B2F0). The meaning of B2Fy bit for sector y of bank 2 is given by the next Table 11. These bits are automatically reset at the end of a write operation if no errors are detected.
SMOD=1 (IFLASH selected)	
B0F(9:0)	Bank 0 IFLASH sector 9:0 status These bits must be set during a Sector Erase operation to select the sectors to erase in bank 0. Besides, during any erase operation, these bits are automatically set and give the status of the 10 sectors of bank 0 (B0F9-B0F0). The meaning of B0Fy bit for sector y of bank 0 is given by the next *Table 11*. These bits are automatically reset at the end of a Write operation if no errors are detected.

Table 11. Banks (BxS) and sectors (BxFy) status bits meaning

ERR	SUSP	BxS = 1 meaning	BxFy = 1 meaning
1	-	Erase error in bank x	Erase error in sector y of bank x
0	1	Erase suspended in bank x	Erase suspended in sector y of bank x
0	0	Don't care	Don't care

4.4.5 Flash data register 0 low

The Flash address registers (FARH/L) and the Flash data registers (FDR1H/L-FDR0H/L) are used during the program operations to store Flash Address in which to program and data to program.

FDR0L (0x0E 0008) FCR Reset value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN15	DIN14	DIN13	DIN12	DIN11	DIN10	DIN9	DIN8	DIN7	DIN6	DIN5	DIN4	DIN3	DIN2	DIN1	DIN0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 12. Flash data register 0 low

Bit	Function
DIN(15:0)	Data input 15:0 These bits must be written with the data to program the Flash with the following operations: word program (32-bit), double word program (64-bit) and set protection.

4.4.6 Flash data register 0 high

FDR0H (0x0E 000A) FCR Reset value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN31	DIN30	DIN29	DIN28	DIN27	DIN26	DIN25	DIN24	DIN23	DIN22	DIN21	DIN20	DIN19	DIN18	DIN17	DIN16
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 13. Flash data register 0 high

Bit	Function
DIN(31:16)	Data input 31:16 These bits must be written with the data to program the Flash with the following operations: word program (32-bit), double word program (64-bit) and set protection.

4.5.8 Flash non volatile access protection register 1 high

FNVAPR1H (0x0E DFBE) NVR Delivery value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEN15	PEN14	PEN13	PEN12	PEN11	PEN10	PEN9	PEN8	PEN7	PEN6	PEN5	PEN4	PEN3	PEN2	PEN1	PEN0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 26. Flash non volatile access protection register 1 high

Bit	Function
PEN15-0	Protections Enable 15-0 If bit PENx is programmed at 0 and bit PDSx+1 is erased at 1, the action of bit ACCP is enabled again. Bit PENx can be programmed at 0 only if bit PDSx has already been programmed at 0.

4.5.9 Access protection

The Flash modules have one level of access protection (access to data both in Reading and Writing): if bit ACCP of FNVAPR0 is programmed at 0, the IFlash module become access protected: data in the IFlash module can be read/written only if the current execution is from the IFlash module itself.

Protection can be permanently disabled by programming bit PDS0 of FNVAPR1H, in order to analyze rejects. Allowing PDS0 bit programming only when ACCP bit is programmed, guarantees that only an execution from the Flash itself can disable the protections.

Protection can be permanently enabled again by programming bit PEN0 of FNVAPR1L. The action to disable and enable again Access Protections in a permanent way can be executed a maximum of 16 times.

Trying to write into the access protected Flash from internal RAM will be unsuccessful. Trying to read into the access protected Flash from internal RAM will output a dummy data.

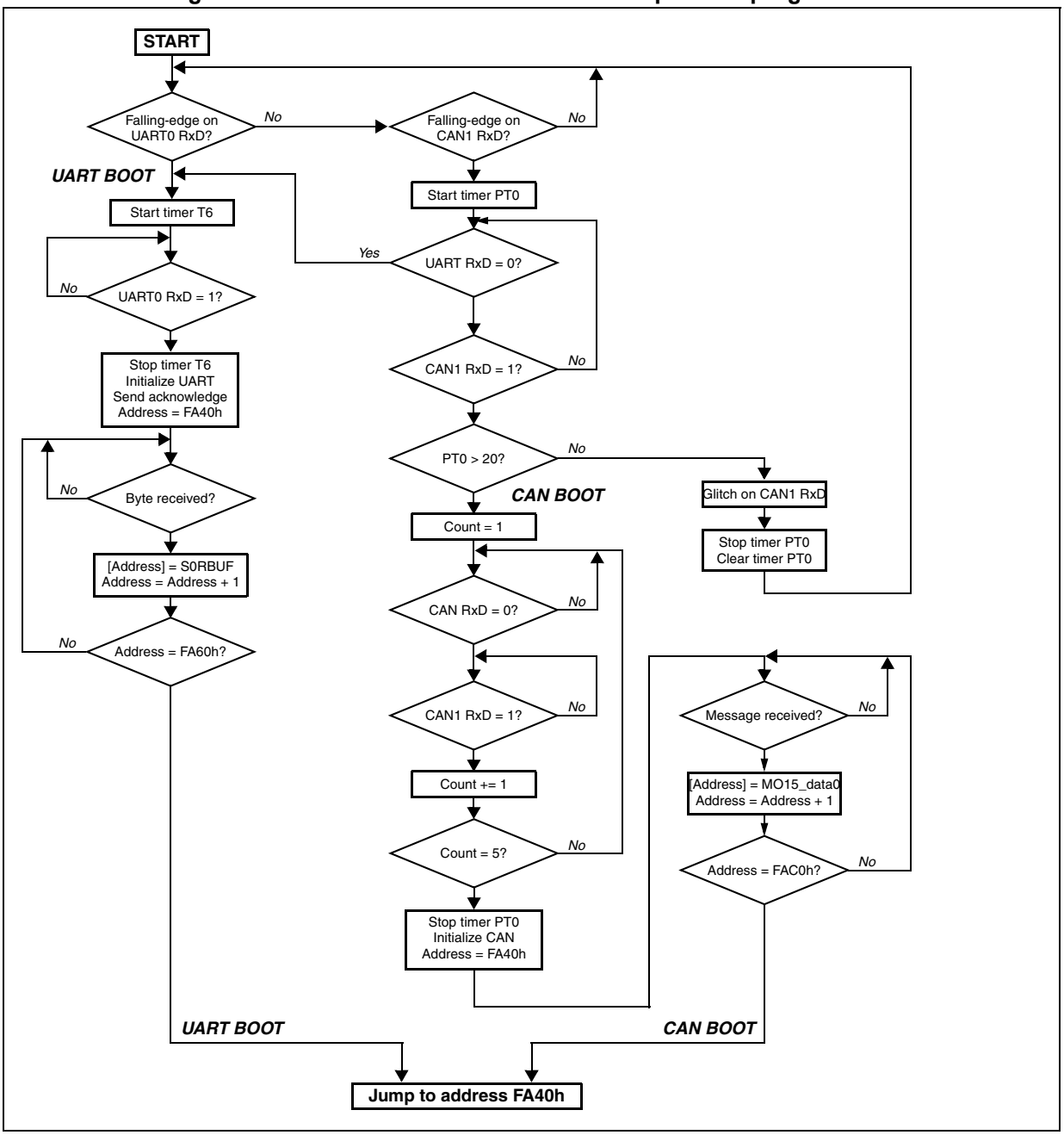
When the Flash module is protected in access, also the data access through PEC of a peripheral is forbidden. To read/write data in PEC mode from/to a protected Bank, first it is necessary to temporary unprotect the Flash module.

Due to ST10 architecture, the XFLASH is seen as external memory: this makes impossible to access protect it from real external memory or internal RAM. In the following table a summary of all levels of possible Access protection is reported: in particular, supposing to enable all possible access protections, when fetching from a memory as listed in the first column, what is possible and what is not possible to do (see column headers) is shown in the table.

Table 27. Summary of access protection level

Access type	Read IFLASH / Jump to IFLASH	Read XFLASH /Jump to XFLASH	Read FLASH Registers	Write FLASH Registers
Fetching from IFLASH	Yes / Yes	Yes / Yes	Yes	Yes
Fetching from XFLASH	No / Yes	Yes / Yes	Yes	No

Figure 5. ST10F276Z5 new standard bootstrap loader program flow



Other than after a normal reset the watchdog timer is disabled, so the bootstrap loading sequence is not time limited. Depending on the selected serial link (UART0 or CAN1), pin TxD0 or CAN1_TxD is configured as output, so the ST10F276Z5 can return the acknowledge byte. Even if the internal IFLASH is enabled, a code cannot be executed from it.

5.7 Selective boot mode

The selective boot is a subcase of the Alternate Boot mode. When none of the signatures are correct, instead of executing the standard bootstrap loader (triggered by P0L.4 low at reset), an additional check is made.

Address 00’1FFCh is read again with the following behavior:

- If value is 0000h or FFFFh, a jump is performed to the standard bootstrap loader.
- Otherwise:
  - High byte is disregarded.
  - Low byte bits select which communication channel is enabled.

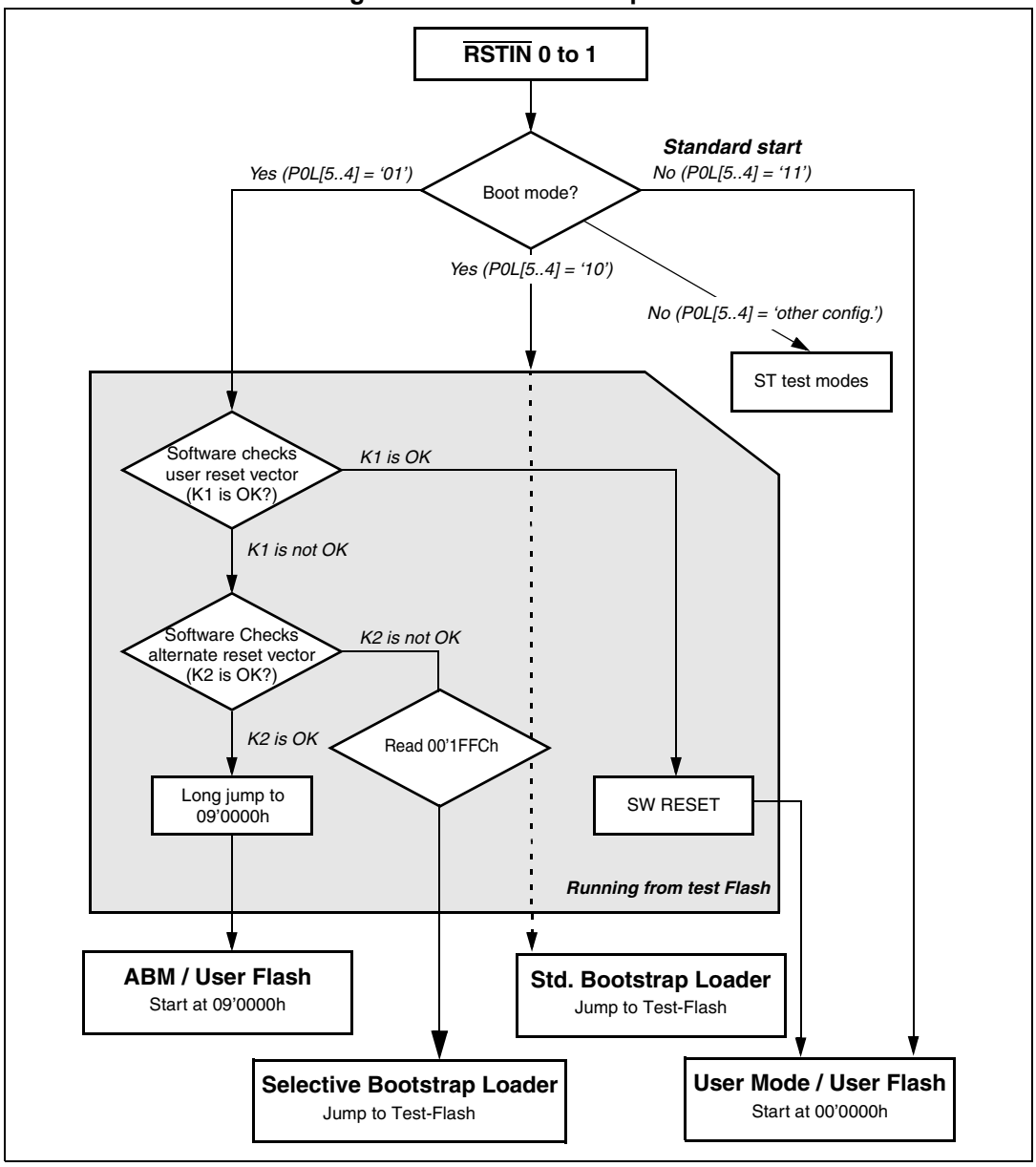
Table 38. Selective boot

Bit	Function
0	UART selection ‘0’: UART is not watched for a Start condition. ‘1’: UART is watched for a Start condition.
1	CAN1 selection ‘0’: CAN1 is not watched for a Start condition. ‘1’: CAN1 is watched for a Start condition.
2..7	Reserved For upward compatibility, must be programmed to ‘0’

Therefore a value:

- 0xXX03 configures the Selective Bootstrap Loader to poll for RxD0 and CAN1_RxD.
- 0xXX01 configures the Selective Bootstrap Loader to poll only RxD0 (no boot via CAN).
- 0xXX02 configures the Selective Bootstrap Loader to poll only CAN1_RxD (no boot via UART).
- Other values allow the ST10F276Z5 to execute an endless loop into the Test-Flash.

Figure 13. Reset boot sequence



7 External bus controller

All of the external memory accesses are performed by the on-chip external bus controller.

The EBC can be programmed to single chip mode when no external memory is required, or to one of four different external memory access modes:

- 16- / 18- / 20- / 24-bit addresses and 16-bit data, demultiplexed
- 16- / 18- / 20- / 24-bit addresses and 16-bit data, multiplexed
- 16- / 18- / 20- / 24-bit addresses and 8-bit data, multiplexed
- 16- / 18- / 20- / 24-bit addresses and 8-bit data, demultiplexed

In demultiplexed bus modes addresses are output on PORT1 and data is input / output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input / output.

Timing characteristics of the external bus interface (memory cycle time, memory tri-state time, length of ALE and read / write delay) are programmable giving the choice of a wide range of memories and external peripherals.

Up to four independent address windows may be defined (using register pairs ADDRSELx / BUSCONx) to access different resources and bus characteristics.

These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1.

All accesses to locations not covered by these four address windows are controlled by BUSCON0. Up to five external $\overline{CS}$ signals (four windows plus default) can be generated in order to save external glue logic. Access to very slow memories is supported by a ‘Ready’ function.

A $\overline{HOLD}$ / $\overline{HLDA}$ protocol is available for bus arbitration which shares external resources with other bus masters.

The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7...P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In master mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to’1’ the slave mode is selected where pin $\overline{HLDA}$ is switched to input. This directly connects the slave controller to another master controller without glue logic.

For applications which require less external memory space, the address space can be restricted to 1 Mbyte, 256 Kbytes or to 64 Kbytes. Port 4 outputs all eight address lines if an address space of 16M Bytes is used, otherwise four, two or no address lines.

Chip select timing can be made programmable. By default (after reset), the $\overline{CSx}$ lines change half a CPU clock cycle after the rising edge of ALE. With the CSCFG bit set in the SYSCON register the $\overline{CSx}$ lines change with the rising edge of ALE.

The active level of the READY pin can be set by bit RDYPOL in the BUSCONx registers. When the READY function is enabled for a specific address window, each bus cycle within the window must be terminated with the active level defined by bit RDYPOL in the associated BUSCON register.

8 Interrupt system

The interrupt response time for internal program execution is from 78 to 187.5 ns at 64 MHz CPU clock.

The ST10F276Z5 architecture supports several mechanisms for fast and flexible response to service requests that can be generated from various sources (internal or external) to the microcontroller. Any of these interrupt requests can be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single Byte or Word data transfer between any two memory locations with an additional increment of either the PEC source or destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited to perform the transmission or the reception of blocks of data. The ST10F276Z5 has 8 PEC channels, each of them offers such fast interrupt-driven data transfer capabilities.

An interrupt control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bit-field is dedicated to each existing interrupt source. Thanks to its related register, each source can be programmed to one of sixteen interrupt priority levels. Once starting to be processed by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

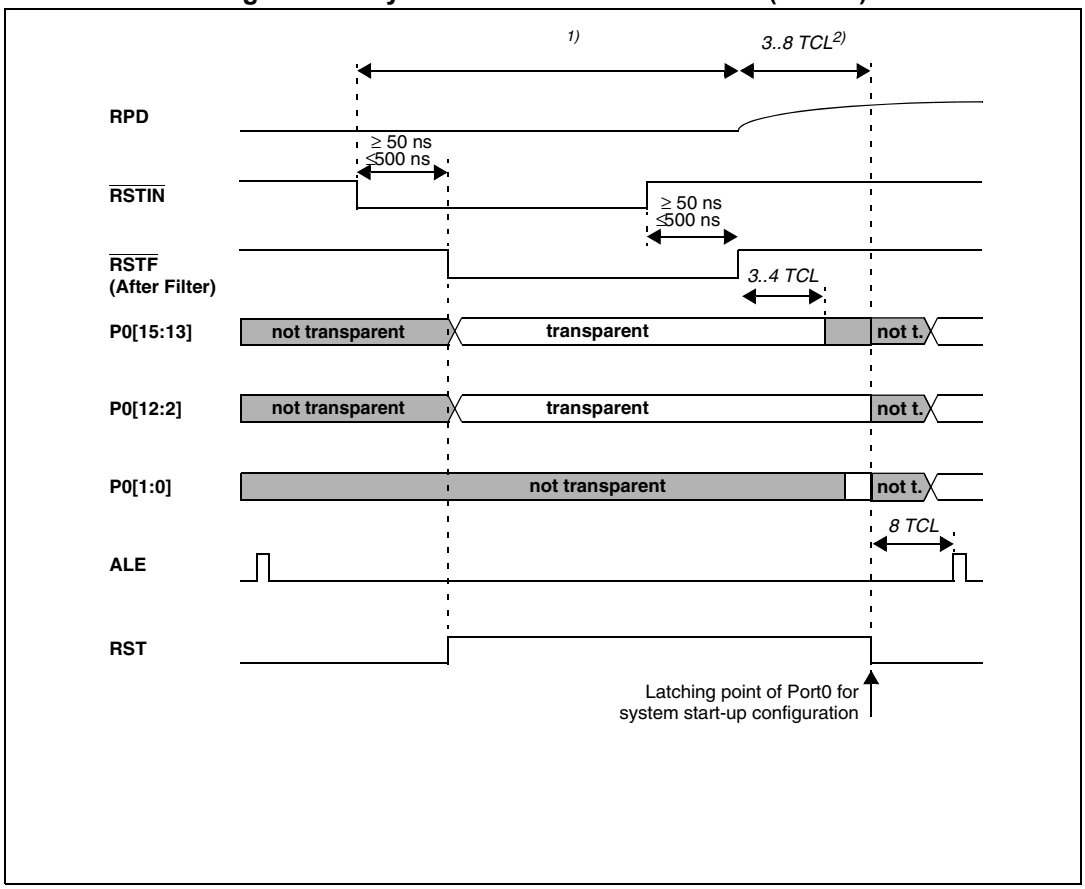
Fast external interrupts may also have interrupt sources selected from other peripherals; for example the CANx controller receive signals (CANx_RxD) and I^2C serial clock signal can be used to interrupt the system.

Table 41 shows all the available ST10F276Z5 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers:

Table 41. Interrupt sources

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	00’0040h	10h
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	00’0044h	11h
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	00’0048h	12h
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	00’004Ch	13h
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	00’0050h	14h
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	00’0054h	15h

Figure 27. Asynchronous hardware RESET ($\overline{EA}$ = 0)



1. This timing can be longer than Port0 settling time + PLL synchronization (if needed, that is P0(15:13) changed).
   It can longer than 500ns to take into account of Input Filter on $\overline{RSTIN}$ pin.
2. 2. 3 to 8 TCL depending on clock source selection.

Exit from asynchronous reset state

When the $\overline{RSTIN}$ pin is pulled high, the device restarts: as already mentioned, if internal FLASH is used, the restarting occurs after the embedded FLASH initialization routine is completed. The system configuration is latched from Port0: ALE, $\overline{RD}$ and $\overline{WR}$/$\overline{WRL}$ pins are driven to their inactive level. The device starts program execution from memory location 00'0000h in code segment 0. This starting location will typically point to the general initialization routine. Timing of asynchronous Hardware Reset sequence are summarized in *Figure 26* and *Figure 27*.

19.4 Software reset

A software reset sequence can be triggered at any time by the protected SRST (software reset) instruction. This instruction can be deliberately executed within a program, e.g. to leave bootstrap loader mode, or on a hardware trap that reveals system failure.

On execution of the SRST instruction, the internal reset sequence is started. The microcontroller behavior is the same as for a synchronous short reset, except that only bits P0.12...P0.8 are latched at the end of the reset sequence, while previously latched, bits P0.7...P0.2 are cleared (that is written at '1').

A Software reset is always taken as synchronous: there is no influence on Software Reset behavior with RPD status. In case Bidirectional Reset is selected, a Software Reset event pulls $\overline{\text{RSTIN}}$ pin low: this occurs only if RPD is high; if RPD is low, $\overline{\text{RSTIN}}$ pin is not pulled low even though Bidirectional Reset is selected.

Refer to *Figure 32* and *Figure 33* for unidirectional SW reset timing, and to *Figure 34*, *Figure 35* and *Figure 36* for bidirectional.

19.5 Watchdog timer reset

When the watchdog timer is not disabled during the initialization, or serviced regularly during program execution, it will overflow and trigger the reset sequence.

Unlike hardware and software resets, the watchdog reset completes a running external bus cycle if this bus cycle either does not use $\overline{\text{READY}}$, or if $\overline{\text{READY}}$ is sampled active (low) after the programmed wait states.

When $\overline{\text{READY}}$ is sampled inactive (high) after the programmed wait states the running external bus cycle is aborted. Then the internal reset sequence is started.

Bit P0.12...P0.8 are latched at the end of the reset sequence and bit P0.7...P0.2 are cleared (that is written at '1').

A Watchdog reset is always taken as synchronous: there is no influence on Watchdog Reset behavior with RPD status. In case Bidirectional Reset is selected, a Watchdog Reset event pulls $\overline{\text{RSTIN}}$ pin low: this occurs only if RPD is high; if RPD is low, $\overline{\text{RSTIN}}$ pin is not pulled low even though Bidirectional Reset is selected.

Refer to *Figure 32* and *Figure 33* for unidirectional SW reset timing, and to *Figure 34*, *Figure 35* and *Figure 36* for bidirectional.

20.3.4 Power reduction modes summary

In the following *Table 64: Power reduction modes summary*, a summary of the different Power reduction modes is reported.

Table 64. Power reduction modes summary

Mode	V_{DD}	V_{STBY}	CPU	Peripherals	RTC	Main OSC	32 kHz OSC	STBY XRAM	XRAM
Idle	on	on	off	on	off	run	off	biased	biased
	on	on	off	on	on	run	on	biased	biased
Power-down	on	on	off	off	off	off	off	biased	biased
	on	on	off	off	on	on	off	biased	biased
	on	on	off	off	on	off	on	biased	biased
Standby	off	on	off	off	off	off	off	biased	off
	off	on	off	off	on	off	on	biased	off

Nonlinearity error

Nonlinearity error is the deviation between actual and the best-fitting A/D conversion characteristics (see *Figure 46*):

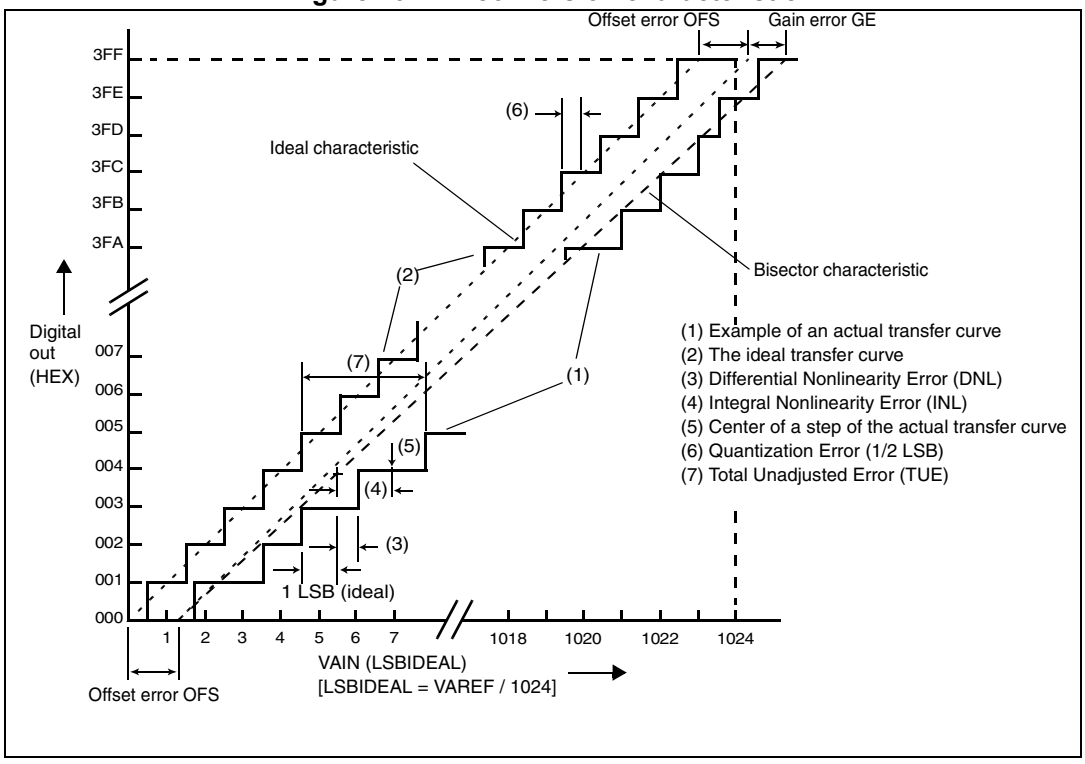
- Differential nonlinearity error is the actual step dimension versus the ideal one (1 LSB_{IDEAL}).
- Integral nonlinearity error is the distance between the center of the actual step and the center of the bisector line, in the actual characteristics. Note that for integral nonlinearity error, the effect of offset, gain and quantization errors is not included.

Note: Bisector characteristic is obtained drawing a line from 1/2 LSB before the first step of the real characteristic, and 1/2 LSB after the last step again of the real characteristic.

23.7.3 Total unadjusted error

The total unadjusted error (TUE) specifies the maximum deviation from the ideal characteristic: The number provided in the datasheet represents the maximum error with respect to the entire characteristic. It is a combination of the offset, gain and integral linearity errors. The different errors may compensate each other depending on the relative sign of the offset and gain errors. Refer to *Figure 46*, see TUE.

Figure 46. A/D conversion characteristic



23.8.2 Definition of internal timing

The internal operation of the ST10F276Z5 is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (for example pipeline) or external (for example bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called “TCL”.

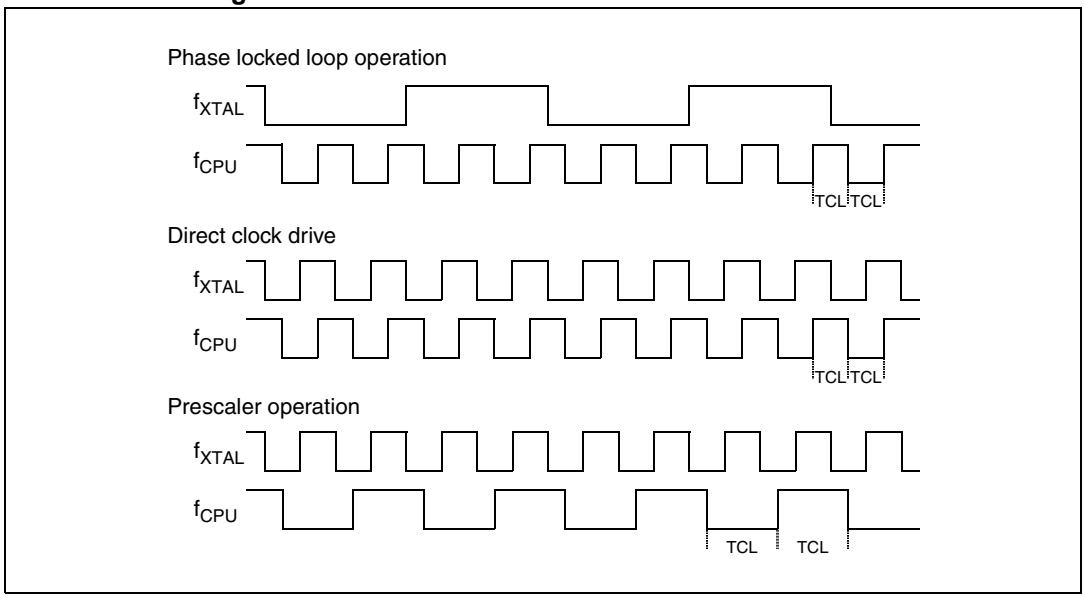
The CPU clock signal can be generated by different mechanisms. The duration of TCL and its variation (and also the derived external timing) depends on the mechanism used to generate f_{CPU}.

This influence must be regarded when calculating the timings for the ST10F276Z5.

The example for PLL operation shown in *Figure 52* refers to a PLL factor of 4.

The mechanism used to generate the CPU clock is selected during reset by the logic levels on pins P0.15-13 (P0H.7-5).

Figure 52. Generation mechanisms for the CPU clock



23.8.12 PLL lock/unlock

During normal operation, if the PLL is unlocked for any reason, an interrupt request to the CPU is generated and the reference clock (oscillator) is automatically disconnected from the PLL input: In this way, the PLL goes into free-running mode, providing the system with a backup clock signal (free running frequency F_{free}). This feature allows to recover from a crystal failure occurrence without risking to go into an undefined configuration: The system is provided with a clock allowing the execution of the PLL unlock interrupt routine in a safe mode.

The path between the reference clock and PLL input can be restored only by a hardware reset, or by a bidirectional software or watchdog reset event that forces the RSTIN pin low.

Note: The external RC circuit on RSTIN pin must be the right size in order to extend the duration of the low pulse to grant the PLL to be locked before the level at RSTIN pin is recognized high: Bidirectional reset internally drives RSTIN pin low for just 1024 TCL (definitely not sufficient to get the PLL locked starting from free-running mode).

Conditions: V_{DD} = 5 V ±10%, T_A = –40 / +125 °C

Table 99. PLL lock/unlock timing

Symbol	Parameter	Conditions	Value		Unit
			Min.	Max.	
T_{PSUP}	PLL Start-up time (1)	Stable V_{DD} and reference clock	–	300	µs
T_{LOCK}	PLL Lock-in time	Stable V_{DD} and reference clock, starting from free-running mode	–	250	
T_{JIT}	Single Period Jitter (1) (cycle to cycle = 2 TCL)	6 sigma time period variation (peak to peak)	–500	+500	ps
F_{free}	PLL free running frequency	Multiplication factors: 3, 4 Multiplication factors: 5, 8, 10, 16	250 500	2000 4000	kHz

1. Not 100% tested, guaranteed by design characterization.

23.8.13 Main oscillator specifications

Conditions: V_{DD} = 5 V ±10%, T_A = –40 / +125 °C

Table 100. Main oscillator specifications

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
g_m	Oscillator transconductance		8	17	35	mA/V
V_{OSC}	Oscillation amplitude (1)	Peak to peak	–	V_{DD} – 0.4	–	V
V_{AV}	Oscillation voltage level (1)	Sine wave middle	–	V_{DD} / 2 –0.25	–	
t_{STUP}	Oscillator start-up time (1)	Stable V_{DD} - crystal	–	3	4	ms
		Stable V_{DD}, resonator	–	2	3	

1. Not 100% tested, guaranteed by design characterization

23.8.18 Multiplexed bus

V_{DD} = 5 V ±10%, V_{SS} = 0 V, T_A = –40 to +125 °C, C_L = 50 pF,
ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (75 ns at 40 MHz CPU clock without wait states).

Table 106. Multiplexed bus

Symbol		Parameter	F_{CPU} = 40 MHz TCL = 12.5 ns		Variable CPU clock 1/2 TCL = 1 to 64 MHz		Unit
			Min.	Max.	Min.	Max.	
t_5	CC	ALE high time	4 + t_A	–	TCL – 8.5 + t_A	–	ns
t_6	CC	Address setup to ALE	1.5 + t_A		TCL – 11 + t_A		
t_7	CC	Address hold after ALE	4 + t_A		TCL – 8.5 + t_A		
t_8	CC	ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	4 + t_A		TCL – 8.5 + t_A		
t_9	CC	ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	– 8.5 + t_A		– 8.5 + t_A		
t_{10}	CC	Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)(1)	–	6	–	6	
t_{11}	CC	Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)1		18.5		TCL + 6	
t_{12}	CC	$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	15.5 + t_C	–	2TCL – 9.5 + t_C	–	
t_{13}	CC	$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	28 + t_C		3TCL – 9.5 + t_C		
t_{14}	SR	$\overline{RD}$ to valid data in (with RW-delay)	–	6 + t_C	–	2TCL – 19 + t_C	
t_{15}	SR	$\overline{RD}$ to valid data in (no RW-delay)		18.5 + t_C		3TCL – 19 + t_C	
t_{16}	SR	ALE low to valid data in		17.5 + + t_A + t_C		3TCL – 20 + + t_A + t_C	
t_{17}	SR	Address/Unlatched $\overline{CS}$ to valid data in		20 + $2t_A$ + + t_C		4TCL – 30 + + $2t_A$ + t_C	
t_{18}	SR	Data hold after $\overline{RD}$ rising edge	0	–	0	–	
t_{19}	SR	Data float after $\overline{RD}$1	–	16.5 + t_F	–	2TCL – 8.5 + t_F	
t_{22}	CC	Data valid to $\overline{WR}$	10 + t_C	–	2TCL – 15 + t_C	–	
t_{23}	CC	Data hold after $\overline{WR}$	4 + t_F		2TCL – 8.5 + t_F		
t_{25}	CC	ALE rising edge after $\overline{RD}$, $\overline{WR}$	15 + t_F		2TCL – 10 + t_F		
t_{27}	CC	Address/Unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	10 + t_F		2TCL – 15 + t_F		

Table 107. Demultiplexed bus (continued)

Symbol		Parameter	F_{CPU} = 40 MHz TCL = 12.5 ns		Variable CPU clock 1/2 TCL = 1 to 64 MHz		Unit
			Min.	Max.	Min.	Max.	
t_{28h}	CC	Address/Unlatched $\overline{CS}$ hold after $\overline{WRH}$	– 5 + t_F	–	– 5 + t_F	–	ns
t_{38}	CC	ALE falling edge to Latched $\overline{CS}$	– 4 – t_A	6 – t_A	– 4 – t_A	6 – t_A	ns
t_{39}	SR	$\overline{Latched\ CS}$ low to Valid Data In	–	16.5 + t_C + 2t_A	–	3TCL – 21+ t_C + 2t_A	ns
t_{41}	CC	$\overline{Latched\ CS}$ hold after $\overline{RD}$, $\overline{WR}$	2 + t_F	–	TCL – 10.5 + t_F	–	ns
t_{82}	CC	Address setup to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	14 + 2t_A	–	2TCL – 11 + 2t_A	–	ns
t_{83}	CC	Address setup to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	2 + 2t_A	–	TCL –10.5 + 2t_A	–	ns
t_{46}	SR	$\overline{RdCS}$ to Valid Data In (with RW-delay)	–	4 + t_C	–	2TCL – 21 + t_C	ns
t_{47}	SR	$\overline{RdCS}$ to Valid Data In (no RW-delay)	–	16.5 + t_C	–	3TCL – 21 + t_C	ns
t_{48}	CC	$\overline{RdCS}$, $\overline{WrCS}$ low time (with RW-delay)	15.5 + t_C	–	2TCL – 9.5 + t_C	–	ns
t_{49}	CC	$\overline{RdCS}$, $\overline{WrCS}$ low time (no RW-delay)	28 + t_C	–	3TCL – 9.5 + t_C	–	ns
t_{50}	CC	Data valid to $\overline{WrCS}$	10 + t_C	–	2TCL – 15 + t_C	–	ns
t_{51}	SR	Data hold after $\overline{RdCS}$	0	–	0	–	ns
t_{53}	SR	Data float after $\overline{RdCS}$ (with RW-delay)	–	16.5 + t_F	–	2TCL – 8.5 + t_F	ns
t_{68}	SR	Data float after $\overline{RdCS}$ (no RW-delay)	–	4 + t_F	–	TCL – 8.5 + t_F	ns
t_{55}	CC	Address hold after $\overline{RdCS}$, $\overline{WrCS}$	– 8.5 + t_F	–	– 8.5 + t_F	–	ns
t_{57}	CC	Data hold after $\overline{WrCS}$	2 + t_F	–	TCL – 10.5 + t_F	–	ns

1. RW-delay and t_A refer to the next following bus cycle.
2. Read data is latched with the same clock edge that triggers the address change and the rising $\overline{RD}$ edge. Therefore address changes which occur before the end of RD have no impact on read cycles.

The following figures (*Figure 57* to *Figure 64*) present the different configurations of external memory cycle.

24 Known limitations

This section describes the functional and electrical limitations identified on the CEG silicon revision of the ST10F276Z5.

The major revision of the device is contained in the device identification register, IDCHIP, located at address F07Ch. For Cxx versions, IDCHIP is set to 1143h.

24.1 Functional limitations

The function limitations identified on the ST10F276Z5 are the following:

- Injected conversion stalling the A/D converter (see *Section 24.1.1: Injected conversion stalling the A/D converter*)
- Concurrent transmission requests in DAR mode (C-CAN module) (see *Section 24.1.2: Concurrent transmission requests in DAR-mode (C-CAN module)*)
- Disabling transmission requests (see *Section 24.1.3: Disabling the transmission requests (C-CAN module)*)
- Spurious $\overline{\text{BREQ}}$ pulse in slave mode during external bus arbitration phase (see *Section 24.1.4: Spurious BREQ pulse in slave mode during external bus arbitration phase*)
- Executing PWRDN instructions (see *Section 24.1.5: Executing PWRDN instructions*)
- Behavior of capture/compare (CAPCOM) outputs in COMPARE mode 3 (see *Section 24.1.6: Behavior of CAPCOM outputs in COMPARE mode 3*)

24.1.1 Injected conversion stalling the A/D converter

Description

The A/D converter is stalled and no further conversions are performed when a new injection request is issued before the CPU reads the ADDAT2 register (that is when the CPU has not read the result of the previous injection request).

Workarounds and recovery actions

The following actions allow to unlock the A/D converter:

1. Read the ADDAT2 register twice at the end of every injected conversion. This action also prevents the ADC from being stalled.
2. Disable and then enable again the wait for read mode.

Application conditions

This problem occurs if all the following conditions are fulfilled:

- Injection requests are hardware triggered (via CapCom CC31).
- The results of injected conversions are read by performing a PEC transfer. This prevents from reading twice the ADDAT2 register by software.
- A high level task is disabling the PEC transfer for a long time (time needed for 2 analog conversions plus time between 2 injection requests).