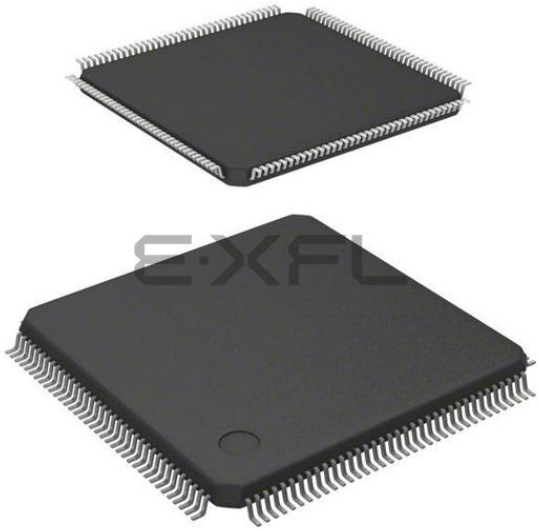

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	40MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	68K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f276z5t3

restrictions and functional differences due to the XBUS peculiarities are present between the classic PWM, and the new XPWM.

- An I^2C interface on the XBUS is added (see X-I^2C or simply I^2C interface).
- CLKOUT function can output either the CPU clock (like in ST10F269) or a software programmable prescaled value of the CPU clock.
- Embedded memory size has been significantly increased (both Flash and RAM).
- PLL multiplication factors have been adapted to new frequency range.
- A/D Converter is not fully compatible versus ST10F269 (timing and programming model). Formula for the conversion time is still valid, while the sampling phase programming model is different.
  Besides, additional 8 channels are available on P1L pins as alternate function: the accuracy reachable with these extra channels is reduced with respect to the standard Port5 channels.
- External Memory bus potential limitations on maximum speed and maximum capacitance load could be introduced (under evaluation): ST10F276Z5 will probably not be able to address an external memory at 64 MHz with 0 wait states (under evaluation).
- XPERCON register bit mapping modified according to new peripherals implementation (not fully compatible with ST10F269).
- Bond-out chip for emulation (ST10R201) cannot achieve more than 50 MHz at room temperature (so no real-time emulation possible at maximum speed).
- Input section characteristics are different. The threshold programmability is extended to all port pins (additional XPICON register); it is possible to select standard TTL (with up to 500 mV of hysteresis) and standard CMOS (with up to 800 mV of hysteresis).
- Output transition is not programmable.
- CAN module is enhanced: the ST10F276Z5 implements two C-CAN modules, so the programming model is slightly different. Besides, the possibility to map in parallel the two CAN modules is added (on P4.5/P4.6).
- On-chip main oscillator input frequency range has been reshaped, reducing it from 1-25 MHz down to 4-12 MHz. This is a high performance oscillator amplifier, providing a very high negative resistance and wide oscillation amplitude: when this on-chip amplifier is used as reference for real-time clock module, the power-down consumption is dominated by the consumption of the oscillator amplifier itself. A metal option is added to offer a low-power oscillator amplifier working in the range of 4-8 MHz: this will allow a power consumption reduction when real-time clock is running in Power-down mode using as reference the on-chip main oscillator clock.
- A second on-chip oscillator amplifier circuit (32 kHz) is implemented for low-power modes: it can be used to provide the reference to the real-time clock counter (either in Power-down or Standby mode). Pin XTAL3 and XTAL4 replace a couple of V_{DD}/V_{SS} pins of ST10F269.
- Possibility to re-program internal XBUS chip select window characteristics (XRAM2 and XFLASH address window) is added.

Table 5. Flash modules sectorization (write operations or with roms1='1')

Bank	Description	Addresses	Size	ST10 Bus size
B0	Bank 0 Test-Flash (B0TF)	0x0000 0000 - 0x0000 1FFF	8 KB	32-bit (I-BUS)
	Bank 0 Flash 0 (B0F0)	0x0001 0000 - 0x0001 1FFF	8 KB	
	Bank 0 Flash 1 (B0F1)	0x0001 2000 - 0x0001 3FFF	8 KB	
	Bank 0 Flash 2 (B0F2)	0x0001 4000 - 0x0001 5FFF	8 KB	
	Bank 0 Flash 3 (B0F3)	0x0001 6000 - 0x0001 7FFF	8 KB	
	Bank 0 Flash 4 (B0F4)	0x0001 8000 - 0x0001 FFFF	32 KB	
	Bank 0 Flash 5 (B0F5)	0x0002 0000 - 0x0002 FFFF	64 KB	
	Bank 0 Flash 6 (B0F6)	0x0003 0000 - 0x0003 FFFF	64 KB	
	Bank 0 Flash 7 (B0F7)	0x0004 0000 - 0x0004 FFFF	64 KB	
	Bank 0 Flash 8 (B0F8)	0x0005 0000 - 0x0005 FFFF	64 KB	
	Bank 0 Flash 9 (B0F9)	0x0006 0000 - 0x0006 FFFF	64 KB	
B1	Bank 1 Flash 0 (B1F0)	0x0007 0000 - 0x0007 FFFF	64 KB	
	Bank 1 Flash 1 (B1F1)	0x0008 0000 - 0x0008 FFFF	64 KB	
B2	Bank 2 Flash 0 (B2F0)	0x0009 0000 - 0x0009 FFFF	64 KB	16-bit (X-BUS)
	Bank 2 Flash 1 (B2F1)	0x000A 0000 - 0x000A FFFF	64 KB	
	Bank 2 Flash 2 (B2F2)	0x000B 0000 - 0x000B FFFF	64 KB	
B3	Bank 3 Flash 0 (B3F0)	0x000C 0000 - 0x000C FFFF	64 KB	
	Bank 3 Flash 1 (B3F1)	0x000D 0000 - 0x000D FFFF	64 KB	

The table above refers to the configuration when bit ROMS1 of SYSCON register is set. When Bootstrap mode is entered:

- Test-Flash is seen and available for code fetches (address 00'0000h)
- User IFlash is only available for read and write accesses
- Write accesses must be made with addresses starting in segment 1 from 01'0000h, whatever ROMS1 bit in SYSCON value
- Read accesses are made in segment 0 or in segment 1 depending of ROMS1 value.

In Bootstrap mode, by default ROMS1 = 0, so the first 32KBytes of IFlash are mapped in segment 0.

Example

In default configuration, to program address 0, user must put the value 01'0000h in the FARL and FARH registers, but to verify the content of the address 0 a read to 00'0000h must be performed.

Table 6 shows the control register interface composition: this set of registers can be addressed by the CPU.

Erase suspend, program and resume

A Sector Erase operation can be suspended in order to program (Word or Double Word) another Sector.

Example: Sector Erase of sector B3F1 of Bank 3 in XFLASH Module.

```
FCR0H|= 0x0800;/*Set SER in FCR0H*/
FCR1H|= 0x0002;/*Set B3F1*/
FCR0H|= 0x8000;/*Operation start*/
```

Example: Sector Erase Suspend.

```
FCR0H|= 0x4000;/*Set SUSP in FCR0H*/
do         /*Loop to wait for LOCK=0 and WMS=0*/
{tmp1 = FCR0L;
 tmp2 = FCR0H;
} while ((tmp1 && 0x0010) || (tmp2 && 0x8000));
```

Example: Word Program of data 0x5555AAAA at address 0x0C5554 in XFLASH module.

```
FCR0H&= 0xBFFF;/*Rst SUSP in FCR0H*/
FCR0H|= 0x2000;/*Set WPG in FCR0H*/
FARL = 0x5554; /*Load Add in FARL*/
FARH = 0x000C; /*Load Add in FARH*/
FDR0L = 0xAAAA; /*Load Data in FDR0L*/
FDR0H = 0x5555; /*Load Data in FDR0H*/
FCR0H|= 0x8000; /*Operation start*/
```

Once the Program operation is finished, the Erase operation can be resumed in the following way:

```
FCR0H|= 0x0800;/*Set SER in FCR0H*/
FCR0H|= 0x8000;/*Operation resume*/
```

Notice that during the Program Operation in Erase suspend, bits SER and SUSP are low. A Word or Double Word Program during Erase Suspend cannot be suspended.

To summarize:

- A Sector Erase can be suspended by setting SUSP bit
- To perform a Word Program operation during Erase Suspend, firstly bits SUSP and SER must be reset, then bit WPG and WMS can be set
- To resume the Sector Erase operation bit SER must be set again
- In any case it is forbidden to start any write operation with SUSP bit already set

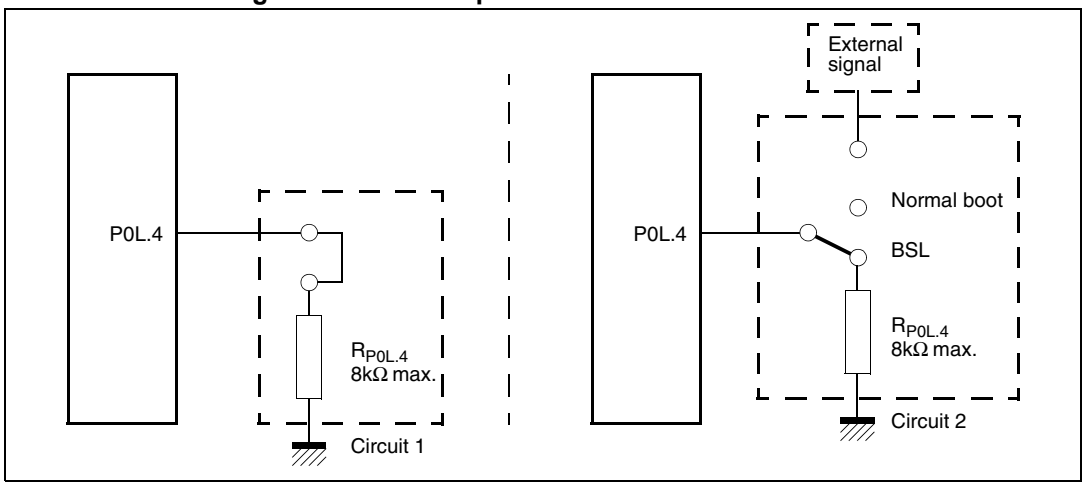
Set protection

Example 1: Enable Write Protection of sectors B0F3-0 of Bank 0 in IFLASH module.

```
FCR0H|= 0x0100;/*Set SPR in FCR0H*/
FARL = 0xDFB4;/*Load Add of register FNVWPIRL in FARL*/
FARH = 0x000E;/*Load Add of register FNVWPIRL in FARH*/
FDR0L = 0xFFF0;/*Load Data in FDR0L*/
FDR0H = 0xFFFF;/*Load Data in FDR0H*/
FCR0H|= 0x8000;/*Operation start*/
```

Notice that bit SMOD of FCR0H must not be set, since Write Protection bits of IFLASH Module are stored in Test-Flash (XFLASH Module).

Figure 7. Hardware provisions to activate the BSL



5.2.5 Memory configuration in bootstrap loader mode

The configuration (that is, the accessibility) of the device memory areas after reset in Bootstrap Loader mode differs from the standard case. Pin $\overline{EA}$ is evaluated when BSL mode is selected to enable or to not enable the external bus:

- If $\overline{EA}$ = 1, the external bus is disabled (BUSACT0 = 0 in BUSCON0 register);
- If $\overline{EA}$ = 0, the external bus is enabled (BUSACT0 = 1 in BUSCON0 register).

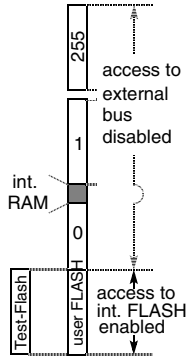
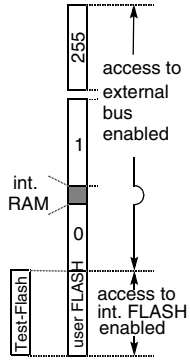
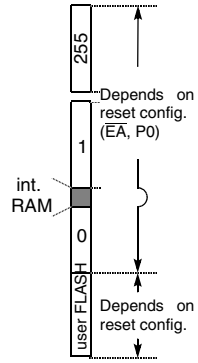
Moreover, while in BSL mode, accesses to the internal IFLASH area are partially redirected:

- All code accesses are made from the special Test-Flash seen in the range 00’0000h to 00’01FFFh;
- User IFLASH is only available for read and write accesses (Test-Flash cannot be read or written);
- Write accesses must be made with addresses starting in segment 1 from 01'0000h, regardless of the value of ROMS1 bit in SYSCON register;
- Read accesses are made in segment 0 or in segment 1 depending on the ROMS1 value;
- In BSL mode, by default, ROMS1 = 0, so the first 32 Kbytes of IFlash are mapped in segment 0.

Example

In default configuration, to program address 0, the user must put the value 01'0000h in the FARL and FARH registers but to verify the content of the address 0 a read to 00'0000h must be performed.

Figure 8. Memory configuration after reset

	16 Mbytes	16 Mbytes	16 Mbytes
			
BSL mode active	**Yes** (P0L.4 = '0')	**Yes** (P0L.4 = '0')	**No** (P0L.4 = '1')
$\overline{EA}$ pin	High	Low	According to application
Code fetch from internal FLASH area	Test-FLASH access	Test-FLASH access	User IFLASH access
Data fetch from internal FLASH area	User IFLASH access	User IFLASH access	User IFLASH access

1. As long as the device is in BSL, the user's software should not try to execute code from the internal IFlash, as the fetches are redirected to the Test-Flash.

5.2.6 Loading the start-up code

After the serial link initialization sequence (see following chapters), the BSL enters a loop to receive 32 bytes (boot via UART) or 128 bytes (boot via CAN).

These bytes are stored sequentially into the device Dual-Port RAM from location 00'FA40h.

To execute the loaded code, the BSL then jumps to location 00'FA40h. The bootstrap sequence running from the Test-Flash is now terminated; however, the microcontroller remains in BSL mode.

Most probably, the initially loaded routine, being the first level user code, will load additional code and data. This first level user code may use the pre-initialized interface (UART or CAN) to receive data and a second level of code, and store it in arbitrary user-defined locations.

This second level of code may be

- The final application code
- Another, more sophisticated, loader routine that adds a transmission protocol to enhance the integrity of the loaded code or data
- A code sequence to change the system configuration and enable the bus interface to store the received data into external memory

In all cases, the device still runs in BSL mode, that is, with the watchdog timer disabled and limited access to the internal IFLASH area.

This second level of loaded code may be

- the final application code
- another, more sophisticated, loader routine that adds a transmission protocol to enhance the integrity of the loaded code or data
- a code sequence to change the system configuration and enable the bus interface to store the received data into external memory

This process may go through several iterations or may directly execute the final application. In all cases the device still runs in BSL mode, that is, with the watchdog timer disabled and limited access to the internal Flash area. All code fetches from the internal IFLASH area ($01'0000_H$...$08'FFFF_H$) are redirected to the special Test-Flash. Data read operations access the internal Flash of the device.

5.3.5 Choosing the baud rate for the BSL via UART

The calculation of the serial baud rate for ASC0 from the length of the first zero byte that is received allows the operation of the bootstrap loader of the device with a wide range of baud rates. However, the upper and lower limits must be kept to ensure proper data transfer.

$$B_{ST10F276} = \frac{f_{CPU}}{32 \cdot (S0BRL + 1)}$$

The device uses timer T6 to measure the length of the initial zero byte. The quantization uncertainty of this measurement implies the first deviation from the real baud rate; the next deviation is implied by the computation of the S0BRL reload value from the timer contents. The formula below shows the association:

$$S0BRL = \frac{T6 - 36}{72}, \quad T6 = \frac{9}{4} \cdot \frac{f_{CPU}}{B_{Host}}$$

For a correct data transfer from the host to the device, the maximum deviation between the internal initialized baud rate for ASC0 and the real baud rate of the host should be below 2.5%. The deviation (F_B, in percent) between host baud rate and device baud rate can be calculated using the formula below:

$$F_B = \left| \frac{B_{Contr} - B_{Host}}{B_{Contr}} \right| \cdot 100\%, \qquad F_B \leq 2.5\ \%$$

Note: Function (F_B) does not consider the tolerances of oscillators and other devices supporting the serial communication.

This baud rate deviation is a nonlinear function depending on the CPU clock and the baud rate of the host. The maxima of the function (F_B) increases with the host baud rate due to the smaller baud rate prescaler factors and the implied higher quantization error (see *Figure 10*).

5.6.6 Exiting alternate boot mode

Once the ABM mode is entered, it can be exited only with a software or hardware reset.

Note: See note from Section 5.2.7 concerning software reset.

5.6.7 Alternate boot user software

If the rules described previously are respected (that is, mapping of variables, disabling of interrupts, exit conditions, predefined vectors in Block 0 of Bank 2, Watchdog usage), then users can write the software they want to execute in this mode starting from 09’0000h.

5.6.8 User/alternate mode signature integrity check

The behavior of the Alternate Boot mode is based on the computing of a signature between the content of two memory locations and a comparison with a reference signature. This requires that users who use Alternate Boot have reserved and programmed the Flash memory locations according to:

User mode signature

- 00'0000h: memory address of *operand0* for the signature computing
- 00’1FFCh: memory address of *operand1* for the signature computing
- 00’1FFEh: memory address for the signature reference

Alternate mode signature

- 09'0000h: memory address of *operand0* for the signature computing
- 09’1FFCh: memory address of *operand1* for the signature computing
- 09’1FFEh: memory address for the signature reference

The values for *operand0, operand1* and the signature should be such that the sequence shown in the figure below is successfully executed.

```
MOV     Rx, CheckBlock1Addr  ; 00’0000h for standard reset
ADD     Rx, CheckBlock2Addr  ; 00’1FFCh for standard reset
CPLB    RLx                  ; 1s complement of the lower
                             ; byte of the sum
CMP     Rx, CheckBlock3Addr  ; 00’1FFEh for standard reset
```

5.6.9 Alternate boot user software aspects

User defined alternate boot code must start at 09’0000h. A new SFR created on the ST10F276Z5 indicates that the device is running in Alternate Boot mode: Bit 5 of EMUCON (mapped at 0xFE0Ah) is set when the alternate boot is selected by the reset configuration. All the other bits are ignored when checking the content of this register to read the value of bit 5.

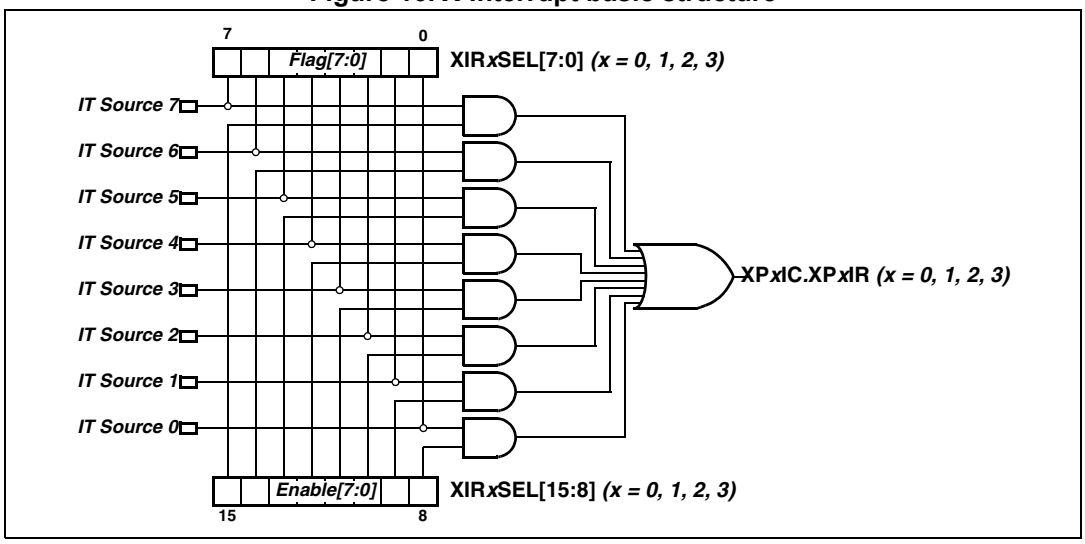
This bit is a read-only bit. It remains set until the next software or hardware reset.

It is based on a set of 16-bit registers XIRxSEL (x=0,1,2,3), divided in two portions each:

- Byte High XIRxSEL[15:8] Interrupt Enable bits
- Byte Low XIRxSEL[7:0] Interrupt Flag bits

When different sources submit an interrupt request, the enable bits (Byte High of XIRxSEL register) define a mask which controls which sources will be associated with the unique available vector. If more than one source is enabled to issue the request, the service routine will have to take care to identify the real event to be serviced. This can easily be done by checking the flag bits (Byte Low of XIRxSEL register). Note that the flag bits can also provide information about events which are not currently serviced by the interrupt controller (since masked through the enable bits), allowing an effective software management also in absence of the possibility to serve the related interrupt request: a periodic polling of the flag bits may be implemented inside the user application.

Figure 16. X-Interrupt basic structure



The *Table 42* summarizes the mapping of the different interrupt sources which shares the four X-interrupt vectors.

Table 42. X-Interrupt detailed mapping

	XP0INT	XP1INT	XP2INT	XP3INT
CAN1 Interrupt	x			x
CAN2 Interrupt		x		x
I2C Receive	x	x	x	
I2C Transmit	x	x	x	
I2C Error				x
SSC1 Receive	x	x	x	
SSC1 Transmit	x	x	x	
SSC1 Error				x

Figure 18. Block diagram of GPT2

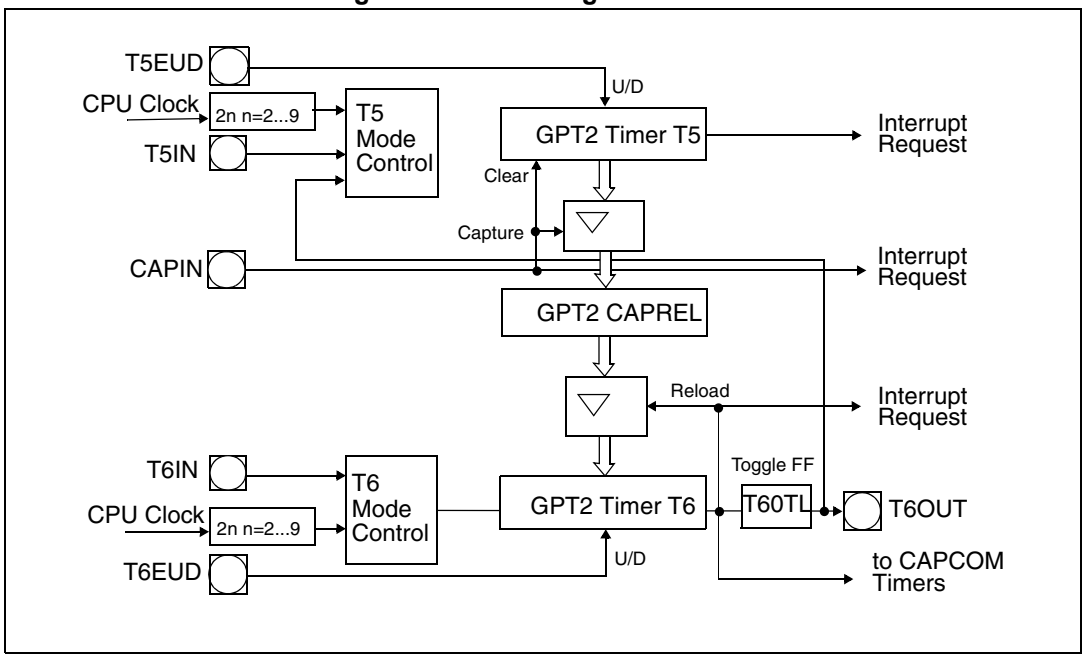
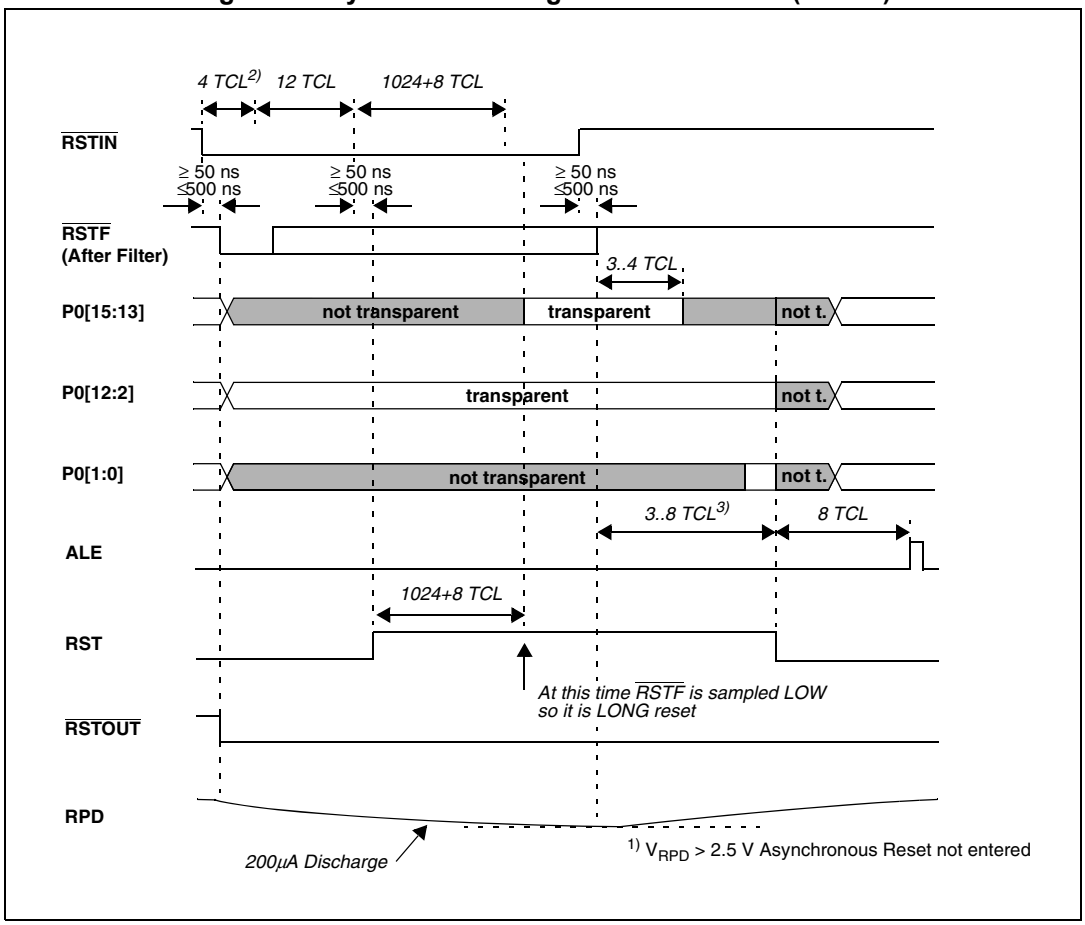


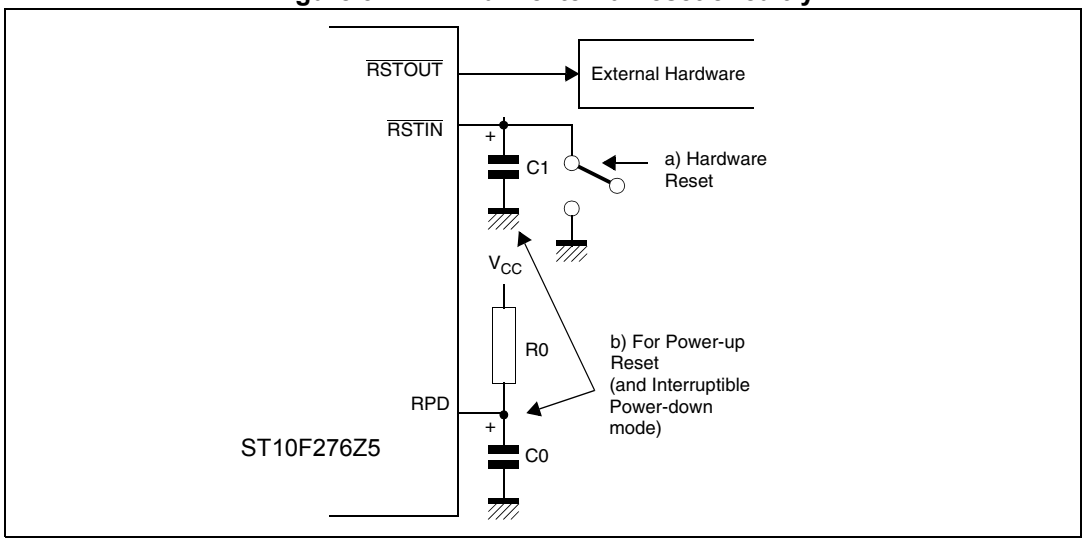
Figure 31. Synchronous long hardware RESET ($\overline{EA}$ = 0)



1. If during the reset condition ($\overline{RSTIN}$ low), RPD voltage drops below the threshold voltage (about 2.5 V for 5 V operation), the asynchronous reset is then immediately entered.
2. Minimum $\overline{RSTIN}$ low pulse duration shall also be longer than 500ns to guarantee the pulse is not masked by the internal filter (refer to *Section 19.6*).
3. 3. 3 to 8 TCL depending on clock source selection.

To ensure correct power-up reset with controlled supply current consumption, specially if clock signal requires a long period of time to stabilize, an asynchronous hardware reset is required during power-up. For this reason, it is recommended to connect the external R0-C0 circuit shown in *Figure 37* to the RPD pin. On power-up, the logical low level on RPD pin forces an asynchronous hardware reset when RSTIN is asserted low. The external pull-up R0 will then charge the capacitor C0. Note that an internal pull-down device on RPD pin is turned on when RSTIN pin is low, and causes the external capacitor (C0) to begin discharging at a typical rate of 100-200µA. With this mechanism, after power-up reset, short low pulses applied on RSTIN produce synchronous hardware reset. If RSTIN is asserted longer than the time needed for C0 to be discharged by the internal pull-down device, then the device is forced in an asynchronous reset. This mechanism insures recovery from very catastrophic failure.

Figure 37. Minimum external reset circuitry



The minimum reset circuit of *Figure 37* is not adequate when the RSTIN pin is driven from the device itself during software or watchdog triggered resets, because of the capacitor C1 that will keep the voltage on RSTIN pin above V_{IL} after the end of the internal reset sequence, and thus will trigger an asynchronous reset sequence.

Figure 38 shows an example of a reset circuit. In this example, R1-C1 external circuit is only used to generate power-up or manual reset, and R0-C0 circuit on RPD is used for power-up reset and to exit from Power-down mode. Diode D1 creates a wired-OR gate connection to the reset pin and may be replaced by open-collector Schmitt trigger buffer. Diode D2 provides a faster cycle time for repetitive power-on resets.

R2 is an optional pull-up for faster recovery and correct biasing of TTL Open Collector drivers.

Before entering Power-down mode (by executing the instruction PWRDN), bit VREGOFF in XMISC register must be set.

Note: Leaving the main voltage regulator active during Power-down may lead to unexpected behavior (ex: CPU wake-up) and power consumption higher than what specified.

20.2.1 Protected Power-down mode

This mode is selected when PWDCFG (bit 5) of SYSCON register is cleared. The Protected Power-down mode is only activated if the NMI pin is pulled low when executing PWRDN instruction (this means that the PWRD instruction belongs to the NMI software routine). This mode is only deactivated with an external hardware reset on RSTIN pin.

20.2.2 Interruptible Power-down mode

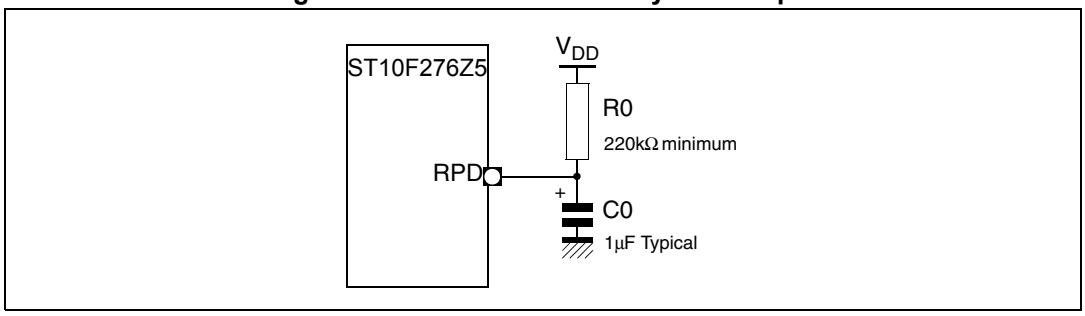
This mode is selected when PWDCFG (bit 5) of SYSCON register is set.

The Interruptible Power-down mode is only activated if all the enabled Fast External Interrupt pins are in their inactive level.

This mode is deactivated with an external reset applied to RSTIN pin or with an interrupt request applied to one of the Fast External Interrupt pins, or with an interrupt generated by the real-time clock, or with an interrupt generated by the activity on CAN's and I^2C module interfaces. To allow the internal PLL and clock to stabilize, the RSTIN pin must be held low according the recommendations described in *Chapter 19: System reset*.

An external RC circuit must be connected to RPD pin, as shown in the *Figure 43*.

Figure 43. External RC circuitry on RPD pin



To exit Power-down mode with an external interrupt, an EXxIN (x = 7...0) pin has to be asserted for at least 40 ns.

20.3 Standby mode

In Standby mode, it is possible to turn off the main V_{DD} provided that V_{STBY} is available through the dedicated pin of the ST10F276Z5.

To enter Standby mode it is mandatory to held the device under reset: once the device is under reset, the RAM is disabled (see XRAM2EN bit of XPERCON register), and its digital interface is frozen in order to avoid any kind of data corruption.

A dedicated embedded low-power voltage regulator is implemented to generate the internal low voltage supply (about 1.65 V in Standby mode) to bias all those circuits that shall remain active: the portion of XRAM (16Kbytes for the ST10F276Z5), the RTC counters and 32 kHz on-chip oscillator amplifier.

22.10 System configuration registers

The ST10F276Z5 registers are used for a different configuration of the overall system. These registers are described below.

SYSCON (FF12h / 89h) SFR Reset value: 0xx0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STKSZ			ROM S1	SGT DIS	ROM EN	BYT DIS	CLK EN	WR CFG	CS CFG	PWD CFG	OWD DIS	BDR STEN	XPEN	VISI BLE	XPER-SHARE
RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Note: SYSCON Reset Value is: 0000 0xx0 0x00 0000b

Table 79. SYSCON description

Bit	Function
XPER-SHARE	XBUS peripheral share mode control '0': External accesses to XBUS peripherals are disabled. '1': XRAM1 and XRAM2 are accessible via the external bus during hold mode. External accesses to the other XBUS peripherals are not guaranteed in terms of AC timings.
VISIBLE	Visible mode control '0': Accesses to XBUS peripherals are done internally. '1': XBUS peripheral accesses are made visible on the external pins.
XPEN	XBUS peripheral enable bit '0': Accesses to the on-chip X-peripherals and XRAM are disabled. '1': The on-chip X-peripherals are enabled.
BDRSTEN	Bidirectional reset enable '0': $\overline{\text{RSTIN}}$ pin is an input pin only. SW Reset or WDT Reset have no effect on this pin. '1': $\overline{\text{RSTIN}}$ pin is a bidirectional pin. This pin is pulled low during internal reset sequence.
OWDDIS	Oscillator watchdog disable control '0': Oscillator Watchdog (OWD) is enabled. If PLL is bypassed, the OWD monitors XTAL1 activity. If there is no activity on XTAL1 for at least 1 µs, the CPU clock is switched automatically to PLL's base frequency (from 750 kHz to 3 MHz). '1': OWD is disabled. If the PLL is bypassed, the CPU clock is always driven by XTAL1 signal. The PLL is turned off to reduce power supply current.
PWDCFG	Power-down mode configuration control '0': Power-down mode can only be entered during PWRDN instruction execution if NMI pin is low, otherwise the instruction has no effect. To exit Power-down mode, an external reset must occur by asserting the $\overline{\text{RSTIN}}$ pin. '1': Power-down mode can only be entered during PWRDN instruction execution if all enabled fast external interrupt EXxIN pins are in their inactive level. Exiting this mode can be done by asserting one enabled EXxIN pin or with external reset.
CSCFG	Chip select configuration control '0': Latched Chip Select lines, CSx changes 1 TCL after rising edge of ALE. '1': Unlatched Chip Select lines, CSx changes with rising edge of ALE.

Table 92. DC characteristics (continued)

Symbol	Parameter	Test Condition	Limit values		Unit
			Min.	Max.	
VHYS **CC**	Input hysteresis (TTL mode) (except RSTIN, EA, NMI, XTAL1, RPD)	(3)	400	700	mV
VHYSS**CC**	Input Hysteresis (CMOS mode) (except RSTIN, EA, NMI, XTAL1, RPD)	(3)	750	1400	
VHYS1**CC**	Input hysteresis RSTIN, EA, NMI	(3)	750	1400	
VHYS2**CC**	Input hysteresis XTAL1	(3)	0	50	
VHYS3**CC**	Input hysteresis READY (TTL only)	(3)	400	700	
VHYS4**CC**	Input hysteresis RPD	(3)	500	1500	
V_{OL} **CC**	Output low voltage (P6[7:0], ALE, RD, WR/WRL, BHE/WRH, CLKOUT, RSTIN, RSTOUT)	I_{OL} = 8 mA I_{OL} = 1 mA	–	0.4 0.05	V
V_{OL1} **CC**	Output low voltage (P0[15:0], P1[15:0], P2[15:0], P3[15,13:0], P4[7:0], P7[7:0], P8[7:0])	I_{OL1} = 4 mA I_{OL1} = 0.5 mA	–	0.4 0.05	
V_{OL2} **CC**	Output low voltage RPD	I_{OL2} = 85 µA I_{OL2} = 80 µA I_{OL2} = 60 µA	–	V_{DD} 0.5 V_{DD} 0.3 V_{DD}	
V_{OH} **CC**	Output high voltage (P6[7:0], ALE, RD, WR/WRL, BHE/WRH, CLKOUT, RSTOUT)	I_{OH} = – 8 mA I_{OH} = – 1 mA	V_{DD} – 0.8 V_{DD} – 0.08	–	
V_{OH1} **CC**	Output high voltage(1) (P0[15:0], P1[15:0], P2[15:0], P3[15,13:0], P4[7:0], P7[7:0], P8[7:0])	I_{OH1} = – 4 mA I_{OH1} = – 0.5 mA	V_{DD} – 0.8 V_{DD} – 0.08	–	
V_{OH2} **CC**	Output high voltage RPD	I_{OH2} = – 2 mA I_{OH2} = – 750 µA I_{OH2} = – 150 µA	0 0.3 V_{DD} 0.5 V_{DD}	–	
$\lvert I_{OZ1} \rvert$ **CC**	Input leakage current (P5[15:0]) (2)	–	–	±0.2	µA
$\lvert I_{OZ2} \rvert$ **CC**	Input leakage current (all except P5[15:0], P2.0, RPD)	–	–	±0.5	
$\lvert I_{OZ3} \rvert$ **CC**	Input leakage current (P2.0) (3)	–	–	+1.0 –0.5	
$\lvert I_{OZ4} \rvert$ **CC**	Input leakage current (RPD)	–	–	±3.0	
$\lvert I_{OV1} \rvert$ **SR**	Overload current (all except P2.0)	(4) (5)	–	±5	mA
$\lvert I_{OV2} \rvert$ **SR**	Overload current (P2.0) (3)	(4)(5)	–	+5 –1	mA
R_{RST} **CC**	RSTIN pull-up resistor	100 kΩ nominal	50	250	kΩ

23.6 Flash characteristics

V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Table 93. Flash characteristics

Parameter	Typical T_A = 25 °C	Maximum T_A = 125 °C		Unit	Notes
	0 cycles (1)	0 cycles (1)	100k cycles		
Word program (32-bit)(2)	35	80	290	µs	–
Double word program (64-bit)(2)	60	150	570	µs	–
Bank 0 program (384K) (double word program)	2.9	7.4	28.0	s	–
Bank 1 program (128K) (double word program)	1.0	2.5	9.3	s	–
Bank 2 program (192K) (double word program)	1.5	3.7	14.0	s	–
Bank 3 program (128K) (double word program)	1.0	2.5	9.3	s	–
Sector erase (8K)	0.6 0.5	0.9 0.8	1.0 0.9	s	not preprogrammed preprogrammed
Sector erase (32K)	1.1 0.8	2.0 1.8	2.7 2.5	s	not preprogrammed preprogrammed
Sector erase (64K)	1.7 1.3	3.7 3.3	5.1 4.7	s	not preprogrammed preprogrammed
Bank 0 erase (384K) (3)	8.2 5.8	20.2 17.7	28.6 26.1	s	not preprogrammed preprogrammed
Bank 1 erase (128K) (3)	3.0 2.2	7.0 6.2	9.8 9.0	s	not preprogrammed preprogrammed
Bank 2 erase (192K) (3)	4.3 3.1	10.3 9.1	14.5 13.3	s	not preprogrammed preprogrammed
Bank 3 erase (128K) (3)	3.0 2.2	7.0 6.2	9.8 9.0	s	not preprogrammed preprogrammed
I-Module erase (512K)(4)	11.2 7.6	27.2 23.5	38.4 34.7	s	not preprogrammed preprogrammed
X-Module erase (320K)(4)	7.3 4.9	17.3 14.8	24.3 21.8	s	not preprogrammed preprogrammed
Chip erase (832K) (5)	18.5 12.0	44.4 37.9	62.6 56.1	s	not preprogrammed preprogrammed
Recovery from Power-down (t_{PD})	–	40	40	µs	(6)
Program suspend latency(6)	–	10	10	µs	

Table 93. Flash characteristics (continued)

Parameter	Typical T_A = 25 °C	Maximum T_A = 125 °C		Unit	Notes
	0 cycles (1)	0 cycles (1)	100k cycles		
Erase suspend latency (6)	–	30	30	µs	
Erase suspend request Rate (6)	20	20	20	ms	Min delay between two requests
Set protection (6)	40	170	170	µs	

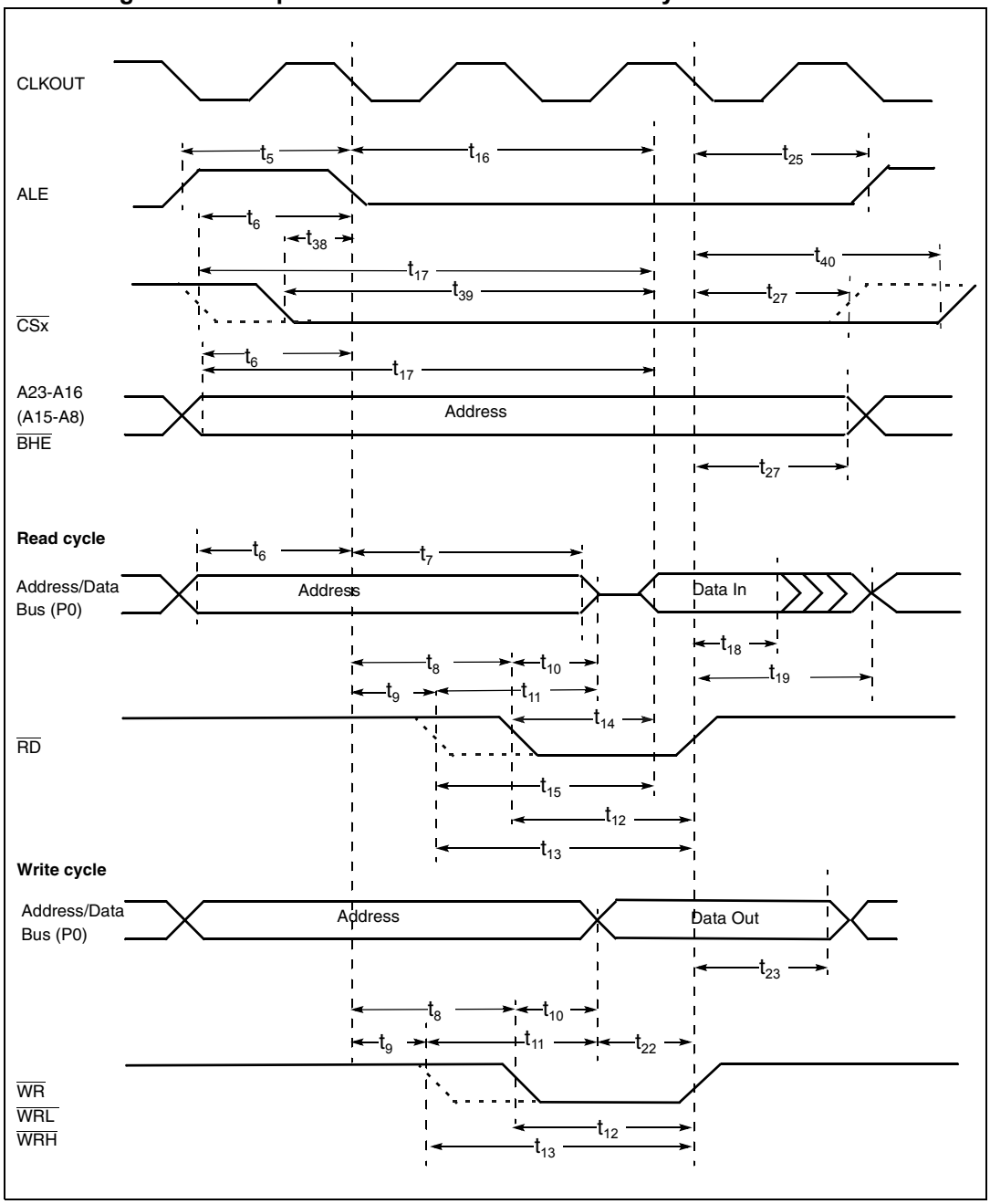
1. The figures are given after about 100 cycles due to testing routines (0 cycles at the final customer).
2. Word and Double Word Programming times are provided as average value derived from a full sector programming time: Absolute value of a Word or Double Word Programming time could be longer than the provided average value.
3. Bank Erase is obtained through a multiple Sector Erase operation (setting bits related to all sectors of the Bank).
4. Module Erase is obtained through a sequence of two Bank Erase operations (since each module is composed by two Banks).
5. Chip Erase is obtained through a sequence of two Module Erase operations on I- and X-Module.
6. Not 100% tested, guaranteed by design characterization

Table 94. Data retention characteristics

Number of program / erase cycles (-40 °C ≤T_A ≤125 °C)	Data retention time (average ambient temperature 60 °C)	
	832 Kbyte (code store)	64 Kbyte (EEPROM emulation)(1)
0 - 100	> 20 years	> 20 years
1000	-	> 20 years
10000	-	10 years
100000	-	1 year

1. Two 64 Kbyte Flash Sectors may be typically used to emulate up to 4, 8 or 16 Kbytes of EEPROM. Therefore, in case of an emulation of a 16 Kbyte EEPROM, 100000 Flash Program / Erase cycles are equivalent to 800000 EEPROM Program/Erase cycles.
For an efficient use of the Read While Write feature and/or EEPROM Emulation please refer to dedicated Application Note document (*AN2061 - EEPROM Emulation with ST10F2xx*). Contact your local field service, local sales person or STMicroelectronics representative to obtain a copy of such a guideline document.

Figure 58. Multiplexed bus with/without R/W delay and extended ALE



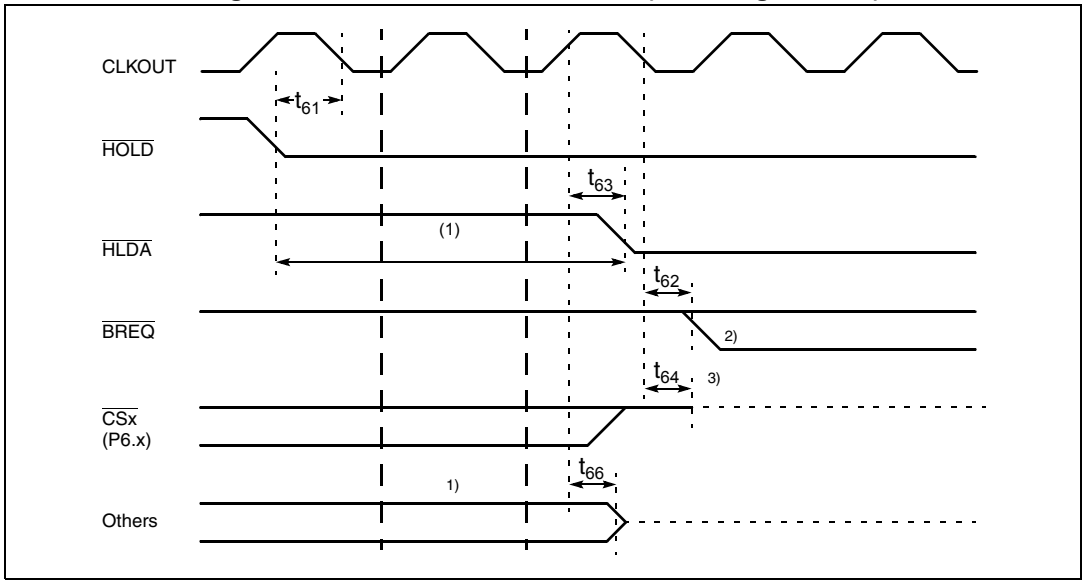
23.8.21 External bus arbitration

V_{DD} = 5 V ±10%, V_{SS} = 0 V, T_A = -40 to +125 °C, C_L = 50 pF

Table 109. External bus arbitration

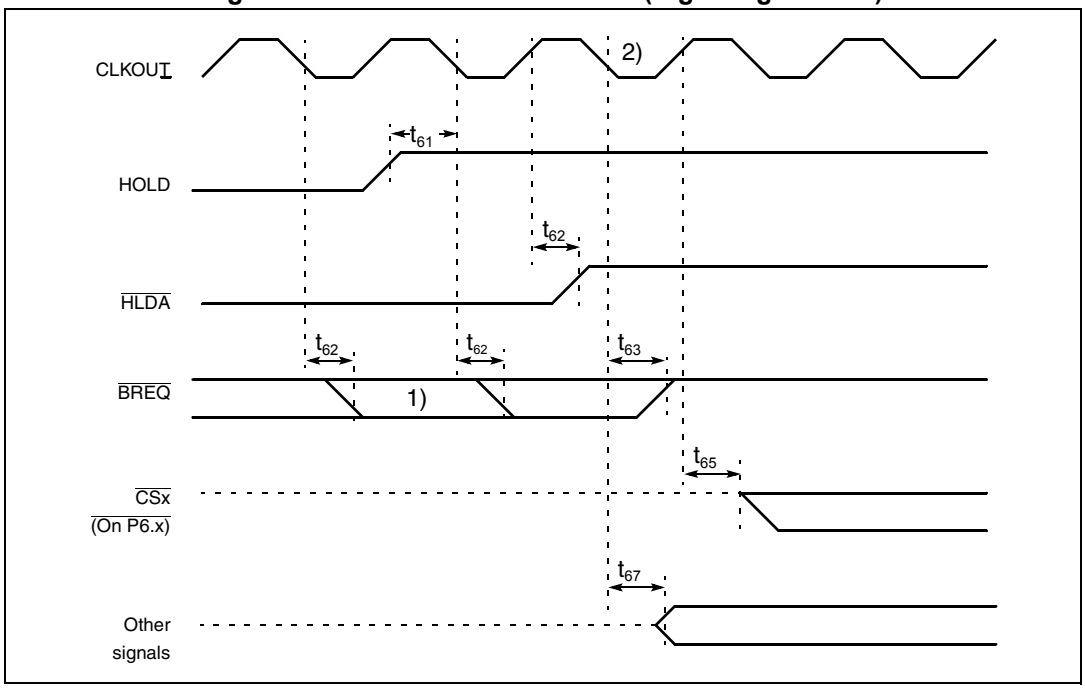
Symbol	Parameter	F_{CPU} = 40 MHz TCL = 12.5 ns		Variable CPU Clock 1/2 TCL = 1 to 64 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{61}**SR**	$\overline{HOLD}$ input setup time to CLKOUT	18.5	–	18.5	–	ns
t_{62}**CC**	CLKOUT to $\overline{HLDA}$ high or $\overline{BREQ}$ low delay	–	12.5	–	12.5	
t_{63}**CC**	CLKOUT to $\overline{HLDA}$ low or $\overline{BREQ}$ high delay					
t_{64}**CC**	$\overline{CSx}$ release		20		20	
t_{65}**CC**	$\overline{CSx}$ drive	– 4	15	– 4	15	
t_{66}**CC**	Other signals release	–	20	–	20	
t_{67}**CC**	Other signals drive	– 4	15	– 4	15	

Figure 66. External bus arbitration (releasing the bus)



1. The device completes the currently running bus cycle before granting bus access.
2. This is the first possibility for $\overline{BREQ}$ to become active.
3. The $\overline{CS}$ outputs will be resistive high (pull-up) after t_{64}.

Figure 67. External bus arbitration (regaining the bus)



1. This is the last chance for $\overline{\text{BREQ}}$ to trigger the indicated regain-sequence. Even if $\overline{\text{BREQ}}$ is activated earlier, the regain-sequence is initiated by HOLD going high. Please note that HOLD may also be deactivated without the device requesting the bus.
2. The next driven bus cycle may start here.