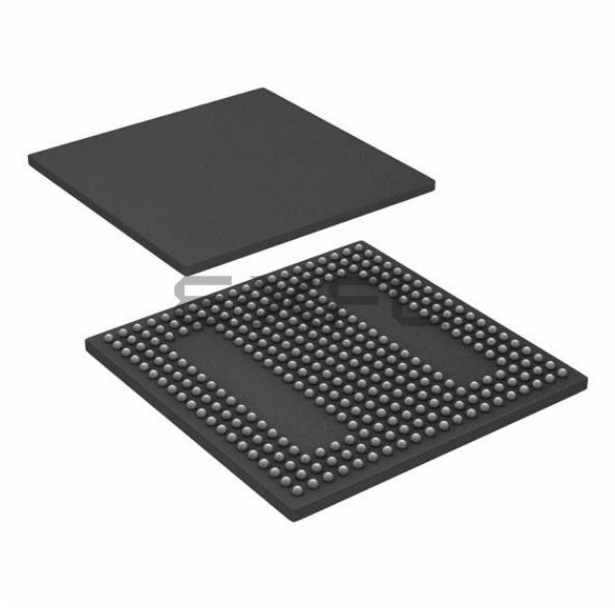

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	148kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	316-LFBGA, CSPBGA
Supplier Device Package	316-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf538bbcz-4a

GENERAL DESCRIPTION

The ADSP-BF538/ADSP-BF538F processors are members of the Blackfin® family of products, incorporating the Analog Devices, Inc./Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction set architecture.

The ADSP-BF538/ADSP-BF538F processors are completely code compatible with other Blackfin processors, differing only with respect to performance, peripherals, and on-chip memory. Specific performance, peripherals, and memory configurations are shown in Table 1.

Ta le 1. Processor Features

Feature	ADSP-BF538	ADSP-BF538F8
SPORTs	*4*	*4*
UARTs	*3*	*3*
SPI	*3*	*3*
TWI	*2*	*2*
CAN	*1*	*1*
PPI	*1*	*1*
Internal 8M bit Parallel Flash	*—*	*1*
Instruction SRAM/Cache	*16K bytes*	*16K bytes*
Instruction SRAM	*64K bytes*	*64K bytes*
Data SRAM/Cache	*32K bytes*	*32K bytes*
Data SRAM	*32K bytes*	*32K bytes*
Scratchpad	*4K bytes*	*4K bytes*
Maximum Frequency	*533 MHz 1066 MMACS*	*533 MHz 1066 MMACS*
Package Option	*BC-316*	*BC-316*

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next generation applications that require RISC-like programmability, multimedia support, and leading edge signal processing in one integrated package.

LOW POWER ARCHITECTURE

Blackfin processors provide world class power management and performance. They are designed using a low power and low voltage methodology and feature dynamic power management, which is the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. Varying the voltage and frequency can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This translates into longer battery life and lower heat dissipation.

SYSTEM INTEGRATION

The ADSP-BF538/ADSP-BF538F processors are highly integrated system-on-a-chip solutions for the next generation of consumer and industrial applications including audio and video signal processing. By combining advanced memory configurations, such as on-chip flash memory, industry-standard interfaces, and a high performance signal processing core, cost-effective solutions can be quickly developed, without the need for costly external components. The system peripherals include three UART ports, three SPI ports, four serial ports (SPORTs), one CAN interface, two 2-wire interfaces (TWI), four general-purpose timers (three with PWM capability), a real-time clock, a watchdog timer, a parallel peripheral interface (PPI), and general-purpose I/O pins.

ADSP-BF538/ADSP-BF538F PROCESSOR PERIPHERALS

The ADSP-BF538/ADSP-BF538F processors contain a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram 1). The general-purpose peripherals include functions such as UART, timers with PWM (pulse-width modulation) and pulse measurement capability, general-purpose I/O pins, a real-time clock, and a watchdog timer. This set of functions satisfies a wide variety of typical system support needs and is augmented by the system expansion capabilities of the device. In addition to these general-purpose peripherals, the processors contain high speed serial and parallel ports for interfacing to a variety of audio, video, and modem codec functions. A CAN 2.0B controller is provided for automotive and industrial control networks. An interrupt controller manages interrupts from the on-chip peripherals or from external sources. Power management control functions tailor the performance and power characteristics of the processors and system to many application scenarios.

All of the peripherals, except for general-purpose I/O, CAN, TWI, real-time clock, and timers, are supported by a flexible DMA structure. There are also four separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses running at up to 133 MHz provide enough bandwidth to keep the processor core running with activity on all of the on-chip and external peripherals.

The ADSP-BF538/ADSP-BF538F processors include an on-chip voltage regulator in support of the processor's dynamic power management capability. The voltage regulator provides a range of core voltage levels from V_{DDEXT}. The voltage regulator can be bypassed as needed.

SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nom	Max	Unit
V_{DDINT}	Internal Supply Voltage	533 MHz Speed Grade Models [1,2]	0.8	1.25	1.375	V
V_{DDINT}	Internal Supply Voltage	400 MHz Speed Grade Models [1,2]	0.8	1.2	1.32	V
V_{DDEXT}	External Supply Voltage	Models with on-chip flash [2]	2.7	3.3	3.6	V
V_{DDEXT}	External Supply Voltage	Models without on-chip flash [2,3]	2.25	3.0	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage		2.25		3.6	V
V_{IH}	High Level Input Voltage [4]	V_{DDEXT} = Maximum	2.0			V
V_{IH5V}	High Level Input Voltage [5]	V_{DDEXT} = Maximum	2.0			V
$V_{IHCLKIN}$	High Level Input Voltage [6]	V_{DDEXT} = Maximum	2.2			V
V_{IL}	Low Level Input Voltage [4,7]	V_{DDEXT} = Minimum			+0.6	V
V_{IL5V}	Low Level Input Voltage [5]	V_{DDEXT} = Minimum			+0.8	V
T_J	Junction Temperature	316-Ball Chip Scale Package Ball Grid Array (CSP_BA) @ $T_{AMBIENT}$ = 40°C to +85°C	40		+110	°C

[1] The regulator can generate V_{DDINT} at levels of 0.85 V to 1.2 V with –5% to +10% tolerance and 1.25 V with –4% to +10% tolerance

[2] See Ordering Guide on Page 58.

[3] When V_{DDEXT} < 2.70 V, on-chip voltage regulation is not supported.

[4] The 3.3 V tolerant pins are capable of accepting up to 3.6 V maximum V_{IH} The following bidirectional pins are 3.3 V tolerant: DATA15–0, SCK2–0, MISO2–0, MOSI2–0, PF15–0, PPI3–0, SPI1SS, SPI1SEL1, PC9–5, SPI2SS, SPI2SEL1, RX2–1, TX2–1, TSCLK3–0, RSCLK3–0, TFS3–0, RFS3–0, DT2PRI, DT2SEC, DR2PRI, DR2SEC, DT3PRI, DT3SEC, DR3PRI, DR3SEC, and TMR2–0. The following input-only pins are 3.3 V tolerant: RESET, RX0, TCK, TDI, TMS, TRST, ARDY, BMODE1–0, BR, DR0PRI, DR0SEC, DR1PRI, DR1SEC, NMI, PPI_CLK, and RTXI.

[5] The 5 V tolerant pins are capable of accepting up to 5.5 V maximum V_{IH}. The following bidirectional pins are 5 V tolerant: SCL0, SCL1, SDA0, SDA1, CANTX, CANRX, and PC4. The following input-only pin is 5 V tolerant: GPW.

[6] Parameter value applies to the CLKIN input pin.

[7] Parameter value applies to all input and bidirectional pins.

The following tables describe the voltage/frequency requirements for the ADSP-BF538/ADSP-BF538F processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock (Table 11 and Table 12) and system clock (Table 14) specifications. Table 13 describes phase-locked loop operating conditions.

Table 11. Core Clock (CCLK) Requirements — 400 MHz Models

Parameter		Internal Regulator Setting	Max	Unit
f_{CCLK}	CLK Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	400	MHz
f_{CCLK}	CLK Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	364	MHz
f_{CCLK}	CLK Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	333	MHz
f_{CCLK}	CLK Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V	280	MHz
f_{CCLK}	CLK Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V	250	MHz

Table 12. Core Clock (CCLK) Requirements — 533 MHz Models

Parameter		Internal Regulator Setting	Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.2 V Minimum)	1.25 V	533	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	500	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	444	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	400	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.85 V Minimum)	0.95 V	333	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V	250	MHz

Table 13. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	50	Max f_{CCLK}	MHz

Table 14. System Clock (SCLK) Requirements

Parameter[1]		Max	Unit
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} ≥ 1.14 V)	133[2]	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.14 V)	100	MHz

[1] t_{SCLK} (= $1/f_{SCLK}$) must be greater than or equal to t_{CCLK}.
[2] Guaranteed to t_{SCLK} = 7.5 ns. See Table 27 on page 33.

ELECTRICAL CHARACTERISTICS

Parameter[1]		Test Conditions	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage [2]	V_{DDEXT} = +3.0 V, I_{OH} = 0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage [2]	V_{DDEXT} = 3.0 V, I_{OL} = 2.0 mA			0.4	V
I_{IH}	High Level Input Current [3]	V_{DDEXT} = Maximum, V_{IN} = V_{DD} Maximum			10.0	µA
I_{IHP}	High Level Input Current JTAG [4]	V_{DDEXT} = Maximum, V_{IN} = V_{DD} Maximum			50.0	µA
I_{IL}	Low Level Input Current [3]	V_{DDEXT} = Maximum, V_{IN} = 0 V			10.0	µA
I_{OZH}	Three-State Leakage Current [5]	V_{DDEXT} = Maximum, V_{IN} = V_{DD} Maximum			10.0	µA
I_{OZL}	Three-State Leakage Current [5]	V_{DDEXT} = Maximum, V_{IN} = 0 V			10.0	µA
C_{IN}	Input Capacitance [6, 7]	f_{CCLK} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		4	8	pF
$I_{DDDEEPSLEEP}$ [8]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.0 V, f_{CCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		7.5		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 0.8 V, T_J = 25°C, SCLK = 25 MHz			10	mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.14 V, f_{CCLK} = 400 MHz, T_J = 25°C		130		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.2 V, f_{CCLK} = 500 MHz, T_J = 25°C		168		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.2 V, f_{CCLK} = 533 MHz, T_J = 25°C		180		mA
$I_{DDHIBERNATE}$ [8]	V_{DDEXT} Current in Hibernate State	V_{DDEXT} = 3.6 V, CLKIN = 0 MHz, T_J = Max, voltage regulator off (V_{DDINT} = 0 V)		50	100	µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J = 25°C		20		µA
$I_{DDDEEPSLEEP}$ [8]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz		6	Table 15	mA
I_{DDINT} [9]	V_{DDINT} Current	f_{CCLK} > 0 MHz			$I_{DDDEEPSLEEP}$ + (Table 17 uASF)	mA

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins.
[3] Applies to input pins except JTAG inputs.
[4] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{TRST}$).
[5] Applies to three-statable pins.
[6] Applies to all signal pins.
[7] Guaranteed, but not tested.
[8] See the ADSP-BF538/538F Blackfin Processor Hardware Reference for conditions of sleep, deep sleep, and hibernate operating modes.
[9] See Table 16 for the list of I_{DDINT} power vectors covered by various Activity Scaling Factors (ASF).

System designers should refer to Estimating Power for the ADSP-BF538/BF539 Blackfin Processors (EE-298) provides detailed information for optimizing designs for lowest power. All topics discussed in this section are described in detail in EE-298. Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 25 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 15), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 17).

The dynamic component is also subject to an Activity Scaling Factor (ASF) which represents application code running on the processor (Table 16).

Table 15. Static Current (mA)

	V_{DDINT} (V)												
T_J (°C)	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V
40	6.4	7.7	8.8	10.4	12.0	14.0	16.1	18.9	21.9	25.2	28.7	30.6	35.9
25	9.2	10.9	12.5	14.5	16.7	19.3	22.1	25.6	29.5	33.7	38.1	40.5	47.2
0	16.8	18.9	21.5	24.4	27.7	31.7	35.8	40.5	45.8	51.6	58.2	61.0	69.8
25	32.9	37.2	41.4	46.2	51.8	57.4	64.2	72.3	80.0	89.3	98.9	103.3	116.4
40	48.4	54.8	60.5	67.1	74.7	82.9	91.6	101.5	112.4	123.2	136.2	142.0	158.7
55	71.2	78.6	86.5	95.8	104.9	115.7	127.1	139.8	153.6	168.0	183.7	191.0	211.8
70	102.3	112.2	122.1	133.5	146.1	159.2	173.9	189.8	206.7	225.5	245.6	254.1	279.6
85	140.7	153.0	167.0	182.5	198.0	216.0	234.3	254.0	276.0	299.1	324.3	334.8	366.6
100	190.6	207.1	224.6	244.0	265.6	285.7	309.0	333.7	360.0	387.8	417.3	431.1	469.3
105	210.2	228.1	245.1	265.6	285.8	309.2	334.0	360.1	385.6	417.2	448.0	461.5	501.1

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.

Table 16. Activity Scaling Factors

I_{DDINT} Power Vector[1]	Activity Scaling Factor (ASF)[2]
$I_{DD-PEAK}$	1.30
$I_{DD-HIGH}$	1.28
I_{DD-TYP}	1.00
I_{DD-APP}	0.88
I_{DD-NOP}	0.74
$I_{DD-IDLE}$	0.48

[1] See EE-298 for power vector definitions.
[2] All ASF values determined using a 10:1 CCLK:SCLK ratio.

Table 17. Dynamic Current (mA, with ASF = 1.0)[1]

Frequency (MHz)	Voltage (V_{DDINT})												
	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V
50	13.6	14.9	16.4	17.5	19.1	20.5	22.0	23.5	25.4	27.1	29.1	29.7	31.6
100	23.6	26.0	27.9	30.1	32.3	34.4	37.0	39.2	41.7	44.3	46.4	47.6	50.3
200	44.1	47.5	51.0	54.8	58.4	61.8	65.6	69.7	74.3	76.2	82.2	83.4	87.8
250	54.6	58.7	62.8	66.8	71.2	75.7	79.9	84.5	89.8	94.2	99.4	101.2	106.5
300	N/A	69.8	74.1	79.3	84.5	89.0	94.7	100.0	105.5	111.6	116.8	119.3	125.5
375	N/A	N/A	91.9	97.9	103.9	109.9	116.5	122.2	129.7	136.0	142.9	145.9	153.6
400	N/A	N/A	N/A	103.8	110.3	116.9	123.7	130.0	137.5	144.2	151.2	154.5	162.4
425	N/A	N/A	N/A	N/A	116.6	123.7	130.9	137.2	144.7	152.7	159.9	163.3	171.8
475	N/A	N/A	N/A	N/A	N/A	N/A	145.0	151.8	161.4	169.4	177.8	181.1	190.4
500	N/A	N/A	N/A	N/A	N/A	N/A	N/A	159.9	168.9	177.8	186.3	190.0	199.6
533	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	179.8	188.9	198.8	202.2	212.5

[1] The values are not guaranteed as standalone maximum specifications, they must be combined with static current per the equations of Electrical Characteristics on Page 25.

TIMING SPECIFICATIONS

Component specifications are subject to change with PCN notice.

Clock and Reset Timing

Table 21 and Figure 10 describe clock and reset operations. Per Absolute Maximum Ratings on Page 27, combinations of CLKIN and clock multipliers must not select core/peripheral clocks that exceed maximum operating conditions.

Table 21. Clock and Reset Timing

Parameter			Min	Max	Unit
Timing Requirement					
f_{CKIN}	CLKIN Frequency (Commercial/Industrial Models)	[1,2,3,4]	10	50	MHz
t_{CKINL}	CLKIN Low Pulse	[1]	8		ns
t_{CKINH}	CLKIN High Pulse	[1]	8		ns
t_{WRST}	$\overline{RESET}$ Asserted Pulse Width Low	[5]	11 × t_{CKIN}		ns
t_{NOBOOT}	$\overline{RESET}$ Deassertion to First External Access Delay	[6]	3 × t_{CKIN}	5 × t_{CKIN}	ns

[1] Applies to PLL bypass mode and PLL nonbypass mode.
[2] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 11 on Page 24 through Table 16 on Page 26.
[3] The t_{CKIN} period (see Figure 10) equals $1/f_{CKIN}$.
[4] If the DF bit in the PLL_CTL register is set, the minimum f_{CKIN} specification is 24 MHz for commercial/industrial models.
[5] Applies after power-up sequence is complete. See Table 22 and Figure 11 for power-up reset timing.
[6] Applies when processor is configured in No Boot Mode (BMODE2-0 = b#000).

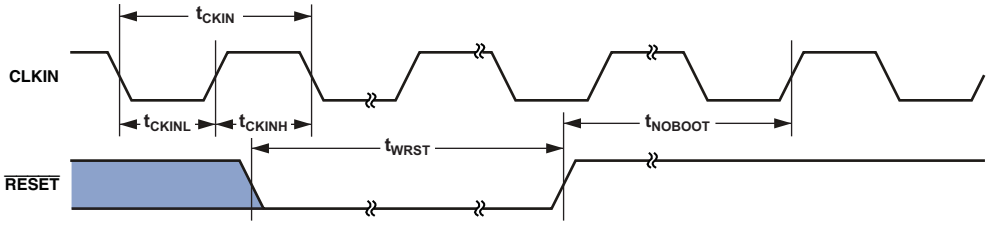
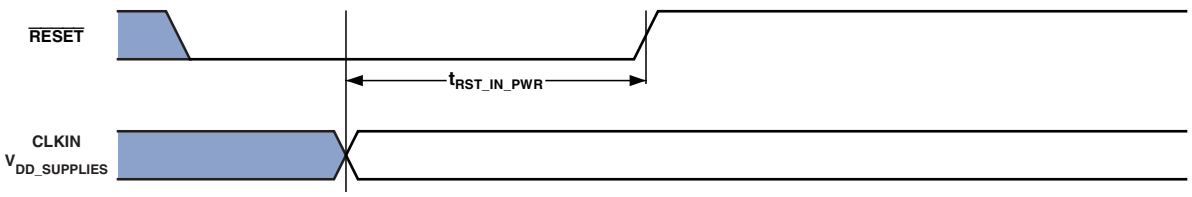


Figure 10. Clock and Reset Timing

Table 22. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{RESET}$ Deasserted after the V_{DDINT}, V_{DDEXT}, V_{DDRTC}, and CLKIN Pins are Stable and Within Specification	3500 × t_{CKIN}		ns



In Figure 11, $V_{DD\_SUPPLIES}$ is V_{DDINT}, V_{DDEXT}, V_{DDRTC}

Figure 11. Power-Up Reset Timing

Table 24. Asynchronous Memory Read Cycle Timing with Asynchronous ARDY

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA15–0 Setup Before CLKOUT	2.1		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
t_{DANR}	ARDY Negated Delay from $\overline{AMSx}$ Asserted [1]		(S + RA – 2) × t_{SCLK}	ns
t_{HAA}	ARDY Asserted Hold After $\overline{ARE}$ Negated	0.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT [2]		6.0	ns
t_{HO}	Output Hold After CLKOUT [2]	0.8		ns

[1] S = number of programmed setup cycles, RA = number of programmed read access cycles.
[2] Output pins include $\overline{AMS3–0}$, $\overline{ABE1–0}$, ADDR19–1, $\overline{AOE}$, $\overline{ARE}$.

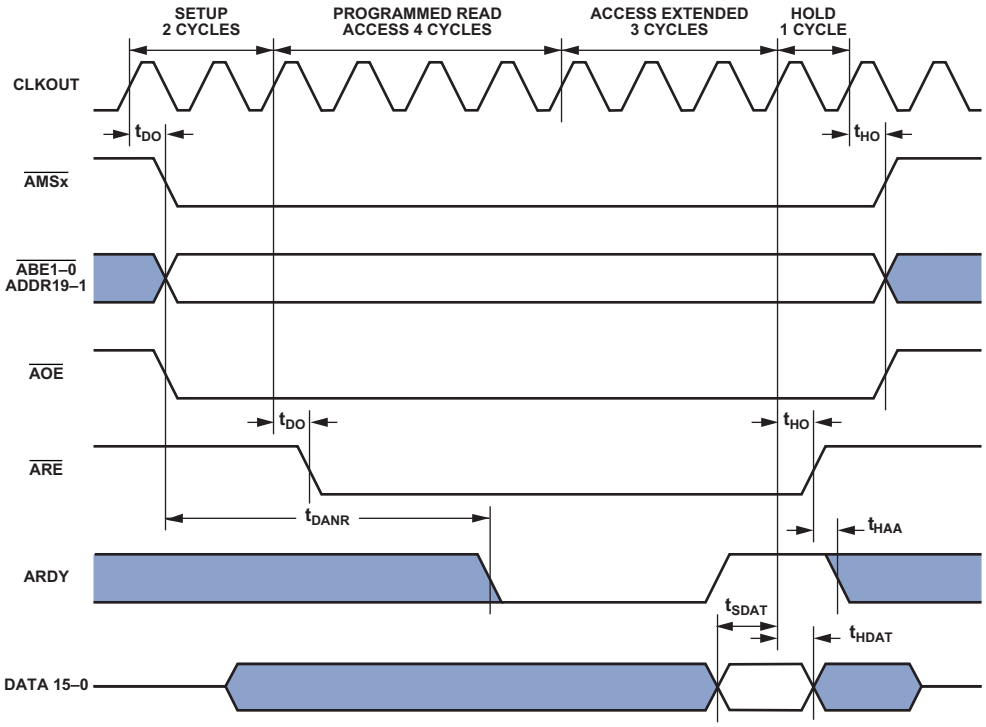


Figure 13. Asynchronous Memory Read Cycle Timing with Asynchronous ARDY

Table 26. Asynchronous Memory Write Cycle Timing with Asynchronous ARDY

Parameter		Min	Max	Unit
Timing Requirements				
t_{DANW}	ARDY Negated Delay from $\overline{AMSx}$ Asserted [1]		(S + WA 2) × t_{SCLK}	ns
t_{HAA}	ARDY Asserted Hold After $\overline{ARE}$ Negated	0.0		ns
Switching Characteristics				
t_{DDAT}	DATA15 0 Disable After CLKOUT		6.0	ns
t_{ENDAT}	DATA15 0 Enable After CLKOUT	1.0		ns
t_{DO}	Output Delay After CLKOUT [2]		6.0	ns
t_{HO}	Output Hold After CLKOUT [2]	0.8		ns

[1] S = number of programmed setup cycles, WA = number of programmed write access cycles.
[2] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, DATA15–0, $\overline{AOE}$, $\overline{AWE}$.

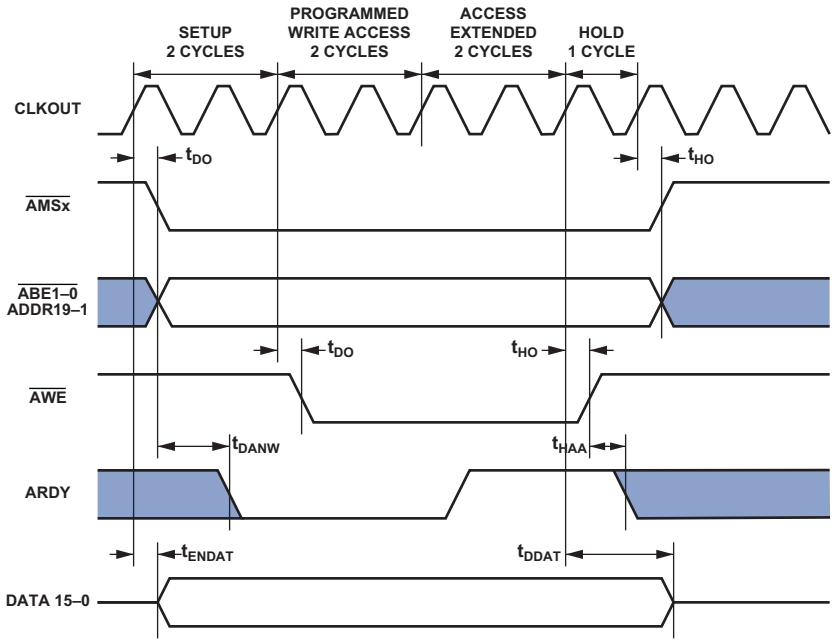


Figure 15. Asynchronous Memory Write Cycle Timing with Asynchronous ARDY

SDRAM Interface Timing

Ta le 27. SDRAM Interface Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{SSDAT}	DATA Setup Before CLKOUT	2.1		ns
t_{HSDAT}	DATA Hold After CLKOUT	0.8		ns
Switching Characteristics				
t_{SCLK}	CLKOUT Period	7.5		ns
t_{SCLKH}	CLKOUT Width High	2.5		ns
t_{SCLKL}	CLKOUT Width Low	2.5		ns
t_{DCAD}	Command, ADDR, Data Delay After CLKOUT[1]		6.0	ns
t_{HCAD}	Command, ADDR, Data Hold After CLKOUT[1]	0.8		ns
t_{DSDAT}	Data Disable After CLKOUT		6.0	ns
t_{ENSDAT}	Data Enable After CLKOUT	1.0		ns

[1] Command pins include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS}$, SA10, SCKE.

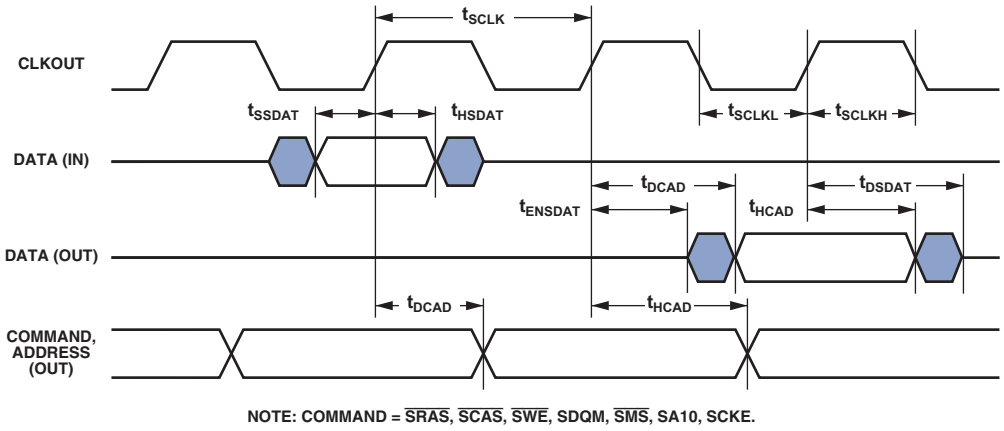


Figure 16. SDRAM Interface Timing

Table 33. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	*Data Enable Delay from External TSCLKx* [1]	*0*		*ns*
t_{DDTTE}	*Data Disable Delay from External TSCLKx* [1, 2, 3]		*10*	*ns*
t_{DTENI}	*Data Enable Delay from Internal TSCLKx* [1]	*2*		*ns*
t_{DDTTI}	*Data Disable Delay from Internal TSCLKx* [1, 2, 3]		*3*	*ns*

[1] Referenced to drive edge.
[2] Applicable to multichannel mode only.
[3] TSCLKx is tied to RSCLKx.

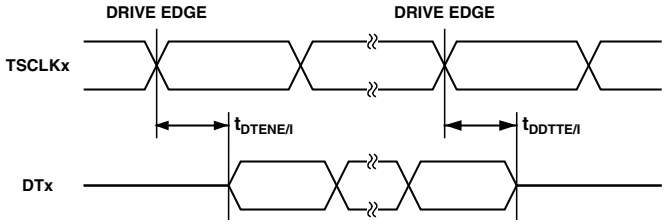


Figure 25. Serial Ports„Enable and Three-State

Table 34. External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFSx or External RFSx in multichannel mode, MFD = 0 [1, 2]		10.0	ns
$t_{DTENLFS}$	Data Enable from Late FS or multichannel mode, MFD = 0 [1, 2]	0		ns

[1] In multichannel mode, TFSx enable and TFSx valid follow $t_{DTENLFS}$ and $t_{DDTLFSE}$.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$, then $t_{DDTTE/I}$ and $t_{DTENE/I}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

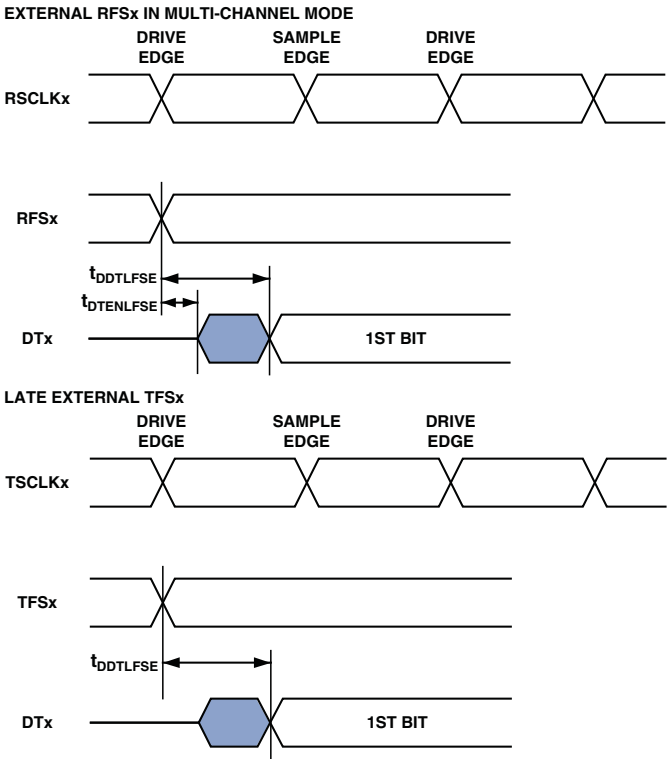


Figure 26. External Late Frame Sync

Timer Cycle Timing

Table 39 and Figure 31 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an absolute maximum input frequency of (f_{SCLK}/2) MHz.

Table 39. Timer Cycle Timing

Parameter		Min	Max	Unit
Timing Characteristics				
t_{WL}	Timer Pulse Width Input Low [1]	1× t_{SCLK}		ns
t_{WH}	Timer Pulse Width Input High [1]	1× t_{SCLK}		ns
t_{TIS}	Timer Input Setup Time Before CLKOUT Low [2]	6.5		ns
t_{TIH}	Timer Input Hold Time After CLKOUT Low [2]	1		ns
Switching Characteristics				
t_{HTO}	Timer Pulse Width Output	1× t_{SCLK}	(2^{32} 1) × t_{SCLK}	ns
t_{TOD}	Timer Output Delay After CLKOUT High		6	ns

[1] The minimum pulse widths apply for TMRx signals in width capture and external clock modes.
[2] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize timer flag inputs.

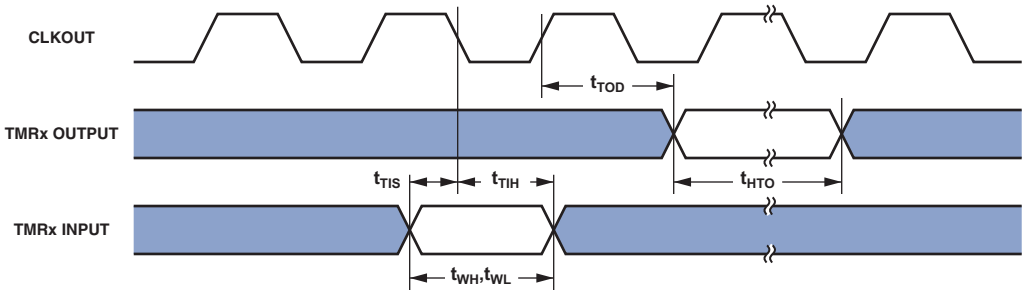


Figure 31. Timer Cycle Timing

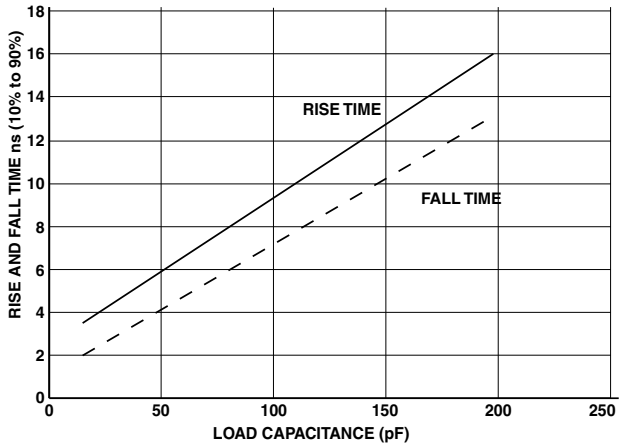


Figure 52. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at V_{DDEXT} = 2.7 V (Min)

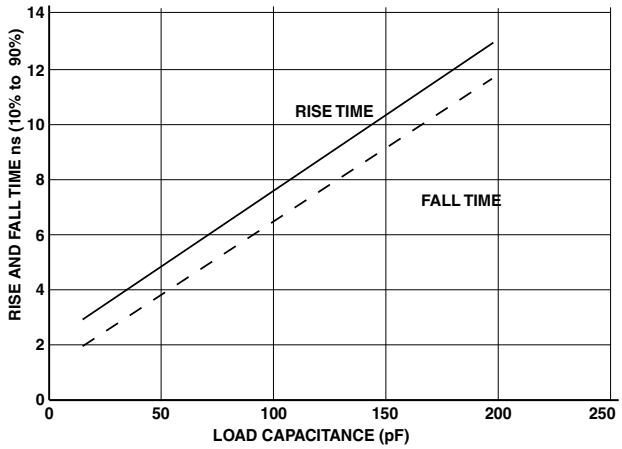


Figure 53. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D at V_{DDEXT} = 3.6 V (Max)

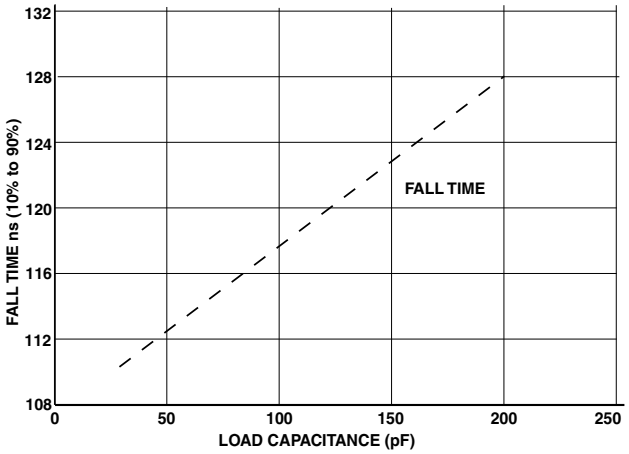


Figure 54. Typical Fall Time (10% to 90%) vs. Load Capacitance for Driver E at V_{DDEXT} = 2.7 V (Min)

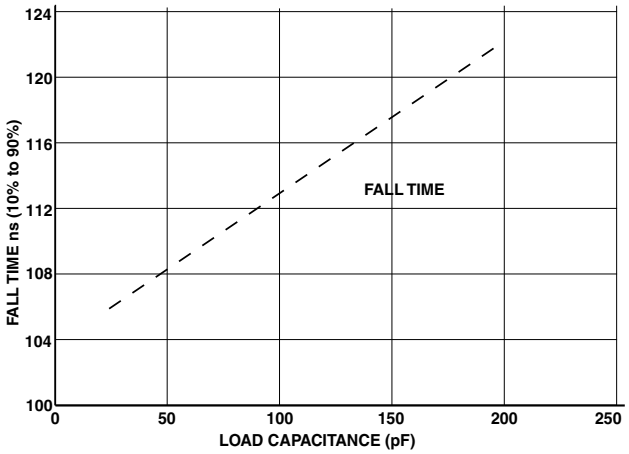


Figure 55. Typical Fall Time (10% to 90%) vs. Load Capacitance for Driver E at V_{DDEXT} = 3.6 V (Max)

THERMAL CHARACTERISTICS

To determine the junction temperature on the application printed circuit board use

$$T_J = T_{CASE} + \Psi_{JT} \times P_D$$

where:

T_J = junction temperature (°C)

T_{CASE} = case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = from Table 41 or Table 42

P_D = power dissipation (see Electrical Characteristics on Page 25 for the method to calculate P_D)

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation

$$T_J = T_A + \theta_{JA} \times P_D$$

where:

T_A = ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and printed circuit board design considerations when an external heatsink is required.

Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

In Table 41 and Table 42, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Table 41. Thermal Characteristics BC-316-2 without Flash

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	25.4	°C/W
θ_{JMA}	1 Linear m/s Airflow	22.8	°C/W
θ_{JMA}	2 Linear m/s Airflow	22.0	°C/W
θ_{JC}		6.7	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.18	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.38	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.40	°C/W

Table 42. Thermal Characteristics BC-316-2 with Flash

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	24.3	°C/W
θ_{JMA}	1 Linear m/s Airflow	21.8	°C/W
θ_{JMA}	2 Linear m/s Airflow	21.0	°C/W
θ_{JC}		6.3	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.17	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.36	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.38	°C/W