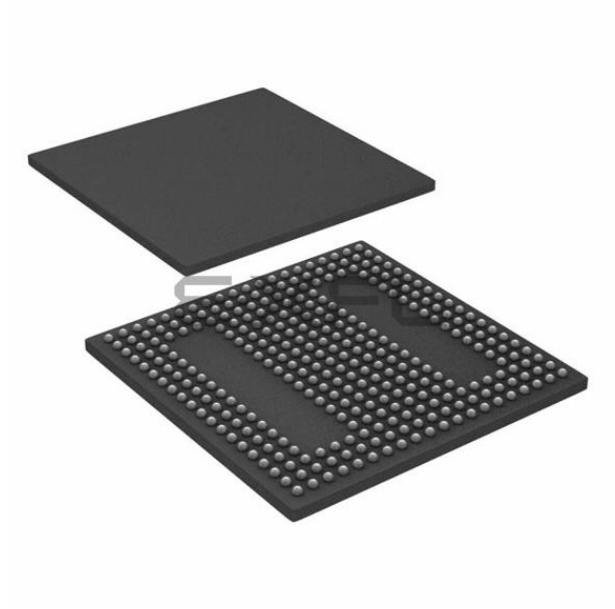


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART
Clock Rate	533MHz
Non-Volatile Memory	External
On-Chip RAM	148kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	316-LFBGA, CSPBGA
Supplier Device Package	316-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf538bbcz-5a

GENERAL DESCRIPTION

The ADSP-BF538/ADSP-BF538F processors are members of the Blackfin® family of products, incorporating the Analog Devices, Inc./Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction set architecture.

The ADSP-BF538/ADSP-BF538F processors are completely code compatible with other Blackfin processors, differing only with respect to performance, peripherals, and on-chip memory. Specific performance, peripherals, and memory configurations are shown in Table 1.

Table 1. Processor Features

Feature	ADSP-BF538	ADSP-BF538F8
SPORTs	4	4
UARTs	3	3
SPI	3	3
TWI	2	2
CAN	1	1
PPI	1	1
Internal 8M bit Parallel Flash	—	1
Instruction SRAM/Cache	16K bytes	16K bytes
Instruction SRAM	64K bytes	64K bytes
Data SRAM/Cache	32K bytes	32K bytes
Data SRAM	32K bytes	32K bytes
Scratchpad	4K bytes	4K bytes
Maximum Frequency	533 MHz 1066 MMACS	533 MHz 1066 MMACS
Package Option	BC-316	BC-316

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next generation applications that require RISC-like programmability, multimedia support, and leading edge signal processing in one integrated package.

LOW POWER ARCHITECTURE

Blackfin processors provide world class power management and performance. They are designed using a low power and low voltage methodology and feature dynamic power management, which is the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. Varying the voltage and frequency can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This translates into longer battery life and lower heat dissipation.

SYSTEM INTEGRATION

The ADSP-BF538/ADSP-BF538F processors are highly integrated system-on-a-chip solutions for the next generation of consumer and industrial applications including audio and video signal processing. By combining advanced memory configurations, such as on-chip flash memory, industry-standard interfaces, and a high performance signal processing core, cost-effective solutions can be quickly developed, without the need for costly external components. The system peripherals include three UART ports, three SPI ports, four serial ports (SPORTs), one CAN interface, two 2-wire interfaces (TWI), four general-purpose timers (three with PWM capability), a real-time clock, a watchdog timer, a parallel peripheral interface (PPI), and general-purpose I/O pins.

ADSP-BF538/ADSP-BF538F PROCESSOR PERIPHERALS

The ADSP-BF538/ADSP-BF538F processors contain a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram 1). The general-purpose peripherals include functions such as UART, timers with PWM (pulse-width modulation) and pulse measurement capability, general-purpose I/O pins, a real-time clock, and a watchdog timer. This set of functions satisfies a wide variety of typical system support needs and is augmented by the system expansion capabilities of the device. In addition to these general-purpose peripherals, the processors contain high speed serial and parallel ports for interfacing to a variety of audio, video, and modem codec functions. A CAN 2.0B controller is provided for automotive and industrial control networks. An interrupt controller manages interrupts from the on-chip peripherals or from external sources. Power management control functions tailor the performance and power characteristics of the processors and system to many application scenarios.

All of the peripherals, except for general-purpose I/O, CAN, TWI, real-time clock, and timers, are supported by a flexible DMA structure. There are also four separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses running at up to 133 MHz provide enough bandwidth to keep the processor core running with activity on all of the on-chip and external peripherals.

The ADSP-BF538/ADSP-BF538F processors include an on-chip voltage regulator in support of the processor's dynamic power management capability. The voltage regulator provides a range of core voltage levels from V_{DDEXT}. The voltage regulator can be bypassed as needed.

External (Off-Chip) Memory

External memory is accessed via the external bus interface unit (EBIU). This 16-bit interface provides a glueless connection to a bank of synchronous DRAM (SDRAM) as well as up to four banks of asynchronous memory devices including flash, EPROM, ROM, SRAM, and memory mapped I/O devices.

The PC133-compliant SDRAM controller can be programmed to interface to up to 128M bytes of SDRAM. The SDRAM controller allows one row to be open for each internal SDRAM bank, for up to four internal SDRAM banks, improving overall system performance.

The asynchronous memory controller can be programmed to control up to four banks of devices with very flexible timing parameters for a wide variety of devices. Each bank occupies a 1M byte segment regardless of the size of the devices used, so that these banks will only be contiguous if each is fully populated with 1M byte of memory.

Flash Memory (ADSP-BF538F8 Only)

The ADSP-BF538F8 processor contains a separate flash die, connected to the EBIU bus, within the package of the processor. Figure 4 shows how the flash memory die and Blackfin processor die are connected.

The ADSP-BF538F8 contains an 8M bit (512K × 16-bit) bottom boot sector Spansion S29AL008J known good die flash memory. For additional information, visit www.spansion.com. Features include the following:

- Access times as fast as 70 ns (EBIU registers must be set appropriately)
- Sector protection
- One million write cycles per sector
- 20 year data retention

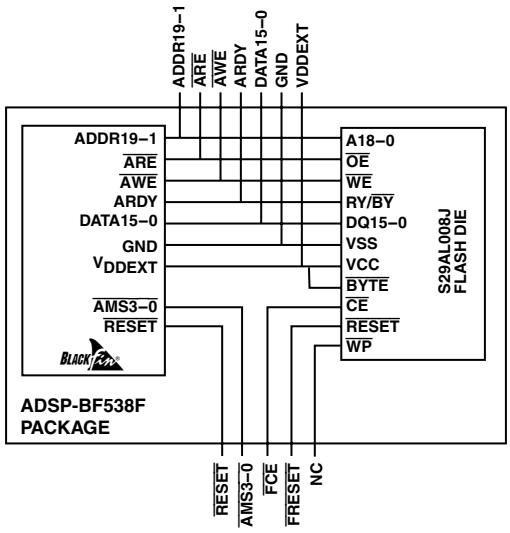


Figure 4. Internal Connection of Flash Memory (ADSP-BF538F8)

The Blackfin processor connects to the flash memory die with address, data, chip enable, write enable, and output enable controls as if it were an external memory device. Note that the write-protect input pin to the flash is not connected and inaccessible, disabling this feature.

The flash chip enable pin $\overline{\text{FCE}}$ must be connected to $\overline{\text{AMS0}}$ or $\overline{\text{AMS3–1}}$ through a printed circuit board trace. When connected to $\overline{\text{AMS0}}$, the Blackfin processor can boot from the flash die. When connected to $\overline{\text{AMS3–1}}$, the flash memory appears as nonvolatile memory in the processor memory map, shown in Figure 3.

Flash Memory Programming

The ADSP-BF538F8 flash memory can be programmed before or after mounting on the printed circuit board.

To program the flash prior to mounting on the printed circuit board, use a hardware programming tool that can provide the data, address, and control stimuli to the flash die through the external pins on the package. During this programming, V_{DDEXT} and GND must be provided to the package and the Blackfin must be held in reset with bus request ($\overline{\text{BR}}$) asserted and a CLKIN provided.

The VisualDSP++ tools can be used to program the flash memory after the device is mounted on a printed circuit board.

Flash Memory Sector Protection

To use the sector protection feature, a high voltage (+12 V nominal) must be applied to the flash $\overline{\text{FRESET}}$ pin. Refer to the flash data sheet for details.

I/O Memory Space

Blackfin processors do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one which contains the control MMRs for all core functions, and the other which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting

The ADSP-BF538/ADSP-BF538F processors contain a small boot kernel, which configures the appropriate peripheral for booting. If the processor is configured to boot from boot ROM memory space, the processor starts executing from the on-chip boot ROM. For more information, see Booting Modes on Page 16.

Event Handling

The event controller on the ADSP-BF538/ADSP-BF538F processors handle all asynchronous and synchronous events to the processors. The processor provides event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization

timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the PF1 pin (TACLK), an external clock input to the PPI_CLK pin (TMRCLK), or to the internal SCLK.

The timer units can be used in conjunction with UART0 to measure the width of the pulses in the data stream to provide an auto-baud detect function for a serial channel.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the three general-purpose programmable timers, a fourth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

SERIAL PORTS (SPORTs)

The ADSP-BF538/ADSP-BF538F processors incorporate four dual-channel synchronous serial ports for serial and multiprocessor communications. The SPORTs support the following features:

- I^2S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling 16 channels of I^2S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131,070) Hz to (f_{SCLK}/2) Hz.
- Word length – Each SPORT supports serial data words from 3 bits to 32 bits in length, transferred most significant bit first or least significant bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer or buffers through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1024 channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

SERIAL PERIPHERAL INTERFACE (SPI) PORTS

The ADSP-BF538/ADSP-BF538F processors incorporate three SPI-compatible ports that enable the processor to communicate with multiple SPI compatible devices.

The SPI interface uses three pins for transferring data: two data pins (master output-slave input, MOSIx, and master input-slave output, MISOx) and a clock pin (serial clock, SCKx). An SPI chip select input pin ($\overline{\text{SPIxSS}}$) lets other SPI devices select the processor. For SPI0, seven SPI chip select output pins ($\overline{\text{SPI0SEL7–1}}$) let the processor select other SPI devices. SPI1 and SPI2 each have a single SPI chip select output pin ($\overline{\text{SPI1SEL1}}$ and $\overline{\text{SPI2SEL1}}$) for SPI point-to-point communication. Each of the SPI select pins are reconfigured GPIO pins. Using these pins, the SPI ports provide a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI ports' baud rate and clock phase/polarities are programmable, and they each have an integrated DMA controller, configurable to support transmit or receive data streams. Each SPI's DMA controller can only service unidirectional accesses at any given time.

The SPI port's clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPIx\_BAUD}$$

where the 16-bit *SPIx_BAUD* register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

2-WIRE INTERFACE

The ADSP-BF538/ADSP-BF538F processors have two 2-wire interface (TWI) modules that are compatible with the Philips Inter-IC bus standard. The TWI modules offer the capabilities of simultaneous master and slave operation, support for 7-bit addressing and multimedia data arbitration. The TWI also includes master clock synchronization and support for clock low extension.

The TWI interface uses two pins for transferring clock (SCLx) and data (SDAx) and supports the protocol at speeds up to 400 kbps.

The TWI interface pins are compatible with 5 V logic levels.

UART PORTS

The ADSP-BF538/ADSP-BF538F processors incorporate three full-duplex universal asynchronous receiver/transmitter (UART) ports, which are fully compatible with PC standard UARTs. The UART ports provide a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA supported, asynchronous transfers of serial data. The UART ports include support for 5 data bits to 8 data bits, 1 stop bit or 2 stop bits, and none, even, or odd parity. The UART ports support two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O mapped UART registers. The data is double buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. Each UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

Each UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) to (f_{SCLK}/16) bits per second.
- Supporting data formats from 7 to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

Each UART port's clock rate is calculated as:

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16 \times UART\_Divisor}$$

where the 16-bit *UART_Divisor* comes from the UARTx_DLH register (most significant 8 bits) and UARTx_DLL register (least significant 8 bits).

In conjunction with the general-purpose timer functions, autobaud detection is supported on UART0.

The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) Serial Infrared Physical Layer Link Specification (SIR) protocol.

GENERAL-PURPOSE PORTS

The ADSP-BF538/ADSP-BF538F processors have up to 54 general-purpose I/O pins that are multiplexed with other peripherals. They are arranged into Ports C, D, E, and F as shown in Table 4.

The general-purpose I/O pins may be individually controlled by manipulation of the control and status registers. These pins may be polled to determine their status.

- GPIO direction control register – Specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers – The processor employs a "write one to modify" mechanism that allows any combination of individual GPIO to be modified in a single instruction, without affecting the level of any other GPIO. Four control registers and a data register are provided for each GPIO port. One register is written in order to set GPIO values, one register is written in order to clear GPIO values, one register is written in order to toggle GPIO values, and one register is written in order to specify a GPIO input or output. Reading the GPIO data allows software to determine the state of the input GPIO pins.

In addition to the GPIO function described above, the 16 Port F pins can be individually configured to generate interrupts.

- GPIO pin interrupt mask registers – The two GPIO pin interrupt mask registers allow each individual PFx pin to function as an interrupt to the processor. Similar to the two GPIO control registers that are used to set and clear individual GPIO pin values, one GPIO pin interrupt mask register sets bits to enable interrupt function, and the other GPIO pin interrupt mask register clears bits to disable interrupt function. PFx pins defined as inputs can be configured to generate hardware interrupts, while output PFx pins can be triggered by software interrupts.
- GPIO pin interrupt sensitivity registers – The two GPIO pin interrupt sensitivity registers specify whether individual PFx pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

Table 4. GPIO Ports

Peripheral	Alternate GPIO Port Function
PPI	GPIO Port F15–3
SPORT2	GPIO Port E7–0
SPORT3	GPIO Port E15–8
SPI0	GPIO Port F7–0
SPI1	GPIO Port D4–0
SPI2	GPIO Port D9–5
UART1	GPIO Port D11–10
UART2	GPIO Port D13–12
CAN	GPIO Port C1–0
GPIO	GPIO Port C9–4[1]

[1] These pins are GPIO only and cannot be reconfigured through software. PC1 and PC4 are open-drain when configured as GPIO outputs.

PARALLEL PERIPHERAL INTERFACE

The ADSP-BF538/ADSP-BF538F processors provide a parallel peripheral interface (PPI) that can connect directly to parallel ADC and DAC converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to 3 frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates at up to f_{SCLK}/2 MHz, and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bidirectional data transfer with up to 16 bits of data. Up to 3 frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex, bi-directional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. Three distinct submodes are supported:

- Input mode – frame syncs and data are inputs into the PPI.
- Frame capture mode – frame syncs are outputs from the PPI, but data are inputs.
- Output mode – frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit, and 10-bit through 16-bit data, and is programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (e.g., for frame capture). The ADSP-BF538/ADSP-BF538F processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct submodes are supported:

- Active video only mode
- Vertical blanking only mode
- Entire field mode

Active Video Only Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1.

CONTROLLER AREA NETWORK (CAN) INTERFACE

The ADSP-BF538/ADSP-BF538F processors provide a CAN controller that is a communication controller implementing the Controller Area Network (CAN) V2.0B protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. CAN is well suited for control applications due to its capability to communicate reliably over a network since the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The CAN controller is based on a 32-entry mailbox RAM and supports both the standard and extended identifier (ID) message formats specified in the CAN protocol specification, revision 2.0, part B.

Each mailbox consists of eight 16-bit data words. The data is divided into fields, which includes a message identifier, a time stamp, a byte count, up to 8 bytes of data, and several control bits. Each node monitors the messages being passed on the network. If the identifier in the transmitted message matches an identifier in one of its mailboxes, then the module knows that the message was meant for it, passes the data into its appropriate mailbox, and signals the processor of message arrival with an interrupt.

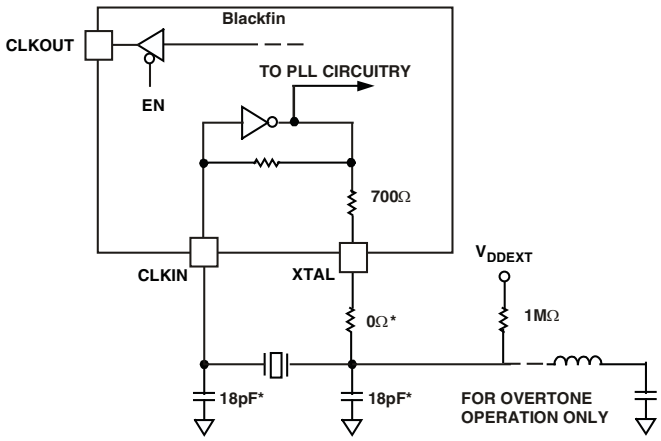
The CAN controller can wake up the processor from sleep mode upon generation of a wake-up event, such that the processor can be maintained in a low power mode during idle conditions. Additionally, a CAN wake-up event can wake up the on-chip internal voltage regulator from the powered-down hibernate state.

The electrical characteristics of each network connection are very stringent, therefore the CAN interface is typically divided into 2 parts: a controller and a transceiver. This allows a single controller to support different drivers and CAN networks. The ADSP-BF538/ADSP-BF538F CAN module represents the controller part of the interface. This module's network I/O is a single transmit output and a single receive input, which connect to a line transceiver.

If an external clock is used, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the ADSP-BF538/ADSP-BF538F processors include an on-chip oscillator circuit, an external crystal may be used. For fundamental frequency operation, use the circuit shown in Figure 7. A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kW range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor, shown in Figure 7, fine tune the phase and amplitude of the sine frequency. The capacitor and resistor values, shown in Figure 7, are typical values only. The capacitor values are dependent upon the crystal manufacturer's load capacitance recommendations and the physical PCB layout. The resistor value depends on the drive level specified by the crystal manufacturer. System designs should verify the customized values based on careful investigation on multiple devices over the allowed temperature range.

A third-overtone crystal can be used at frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 7.



NOTE: VALUES MARKED WITH * MUST BE CUSTOMIZED DEPENDING ON THE CRYSTAL AND LAYOUT. PLEASE ANALYZE CAREFULLY.

Figure 7. External Crystal Connections

As shown in Figure 8, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a user programmable 0.5× to 64× multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 10×, but it can be modified by a software instruction sequence. On-the-fly frequency changes can be effected by simply writing to the PLL_DIV register.

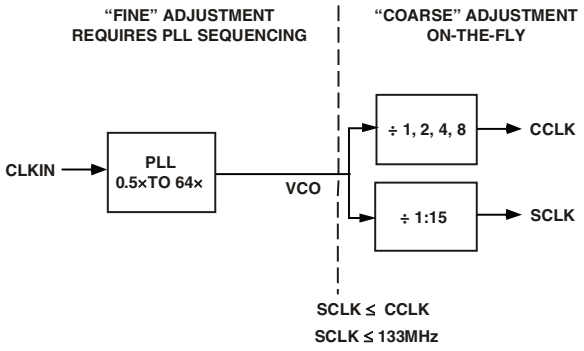


Figure 8. Frequency Modification Methods

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15.

Table 7 illustrates typical system clock ratios:

Table 7. Example System Clock Ratios

Signal Name SSEL3–0	Divider Ratio VCO/SCLK	Example Frequency Ratios (MHz)	
		VCO	SCLK
0001	1:1	100	100
0110	6:1	300	50
1010	10:1	500	50

The maximum frequency of the system clock is f_{SCLK}. Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV).

Note that when the SSEL value is changed, it will affect all the peripherals that derive their clock signals from the SCLK signal.

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 8. This programmable core clock capability is useful for fast core frequency modifications.

Table 8. Core Clock Ratios

Signal Name CSEL1–0	Divider Ratio VCO/CCLK	Example Frequency Ratios	
		VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	500	125
11	8:1	200	25

PIN DESCRIPTIONS

The ADSP-BF538/ADSP-BF538F processors pin definitions are listed in Table 10.

All pins are three-stated during and immediately after reset, except the memory interface, asynchronous memory control, and synchronous memory control pins. These pins are all driven high, with the exception of CLKOUT, which toggles at the system clock rate. If $\overline{BR}$ is active (whether or not $\overline{RESET}$ is asserted), the memory pins are also three-stated. All unused I/O pins have their input buffers disabled with the exception of the pins that need pull-ups or pull-downs, as noted in the table. During hibernate, all outputs are three-stated unless otherwise noted in Table 10.

In order to maintain maximum functionality and reduce package size and pin count, some pins have dual, multiplexed functionality. In cases where pin functionality is reconfigurable, the default state is shown in plain text, while alternate functionality is shown in italics.

Table 10. Pin Descriptions

Pin Name	I/O	Function	Driver Type[1]
Memory Interface			
ADDR19–1	O	Address Bus for Async/Sync Access	A
DATA15–0	I/O	Data Bus for Async/Sync Access	A
$\overline{ABE1–0}$/SDQM1–0	O	Byte Enables/Data Masks for Async/Sync Access	A
$\overline{BR}$	I	Bus Request (This pin should be pulled high when not used.)	
$\overline{BG}$	O	Bus Grant	A
$\overline{BGH}$	O	Bus Grant Hang	A
Asynchronous Memory Control			
$\overline{AMS3–0}$	O	Bank Select (Require pull-ups if hibernate is used.)	A
ARDY	I	Hardware Ready Control	
$\overline{AOE}$	O	Output Enable	A
$\overline{ARE}$	O	Read Enable	A
$\overline{AWE}$	O	Write Enable	A
Flash Control			
$\overline{FCE}$	I	Flash Enable (This pin is internally connected to GND on the ADSP-BF538.)	
$\overline{FRESET}$	I	Flash Reset (This pin is internally connected to GND on the ADSP-BF538.)	
Synchronous Memory Control			
$\overline{SRAS}$	O	Row Address Strobe	A
$\overline{SCAS}$	O	Column Address Strobe	A
$\overline{SWE}$	O	Write Enable	A
SCKE	O	Clock Enable (This pin must be pulled low through a 10 kΩ resistor if hibernate state is used and SDRAM contents need to be preserved during hibernate.)	A
CLKOUT	O	Clock Output	B
SA10	O	A10 Pin	A
$\overline{SMS}$	O	Bank Select	A
Timers			
TMR0	I/O	Timer 0	C
TMR1/*PPI_FS1*	I/O	Timer 1/*PPI Frame Sync1*	C
TMR2/*PPI_FS2*	I/O	Timer 2/*PPI Frame Sync2*	C

Table 10. Pin Descriptions (Continued)

Pin Name	I/O	Function	Driver Type[1]
2-Wire Interface Port		These pins are open-drain and require a pull-up resistor. See version 2.1 of the I^2C specification for proper resistor values.	
SDA0	I/O 5 V	TWI0 Serial Data	E
SCL0	I/O 5 V	TWI0 Serial Clock	E
SDA1	I/O 5 V	TWI1 Serial Data	E
SCL1	I/O 5 V	TWI1 Serial Clock	E
Serial Port0			
RSCLK0	I/O	SPORT0 Receive Serial Clock	D
RFS0	I/O	SPORT0 Receive Frame Sync	C
DR0PRI	I	SPORT0 Receive Data Primary	
DR0SEC	I	SPORT0 Receive Data Secondary	
TSCLK0	I/O	SPORT0 Transmit Serial Clock	D
TFS0	I/O	SPORT0 Transmit Frame Sync	C
DT0PRI	O	SPORT0 Transmit Data Primary	C
DT0SEC	O	SPORT0 Transmit Data Secondary	C
Serial Port1			
RSCLK1	I/O	SPORT1 Receive Serial Clock	D
RFS1	I/O	SPORT1 Receive Frame Sync	C
DR1PRI	I	SPORT1 Receive Data Primary	
DR1SEC	I	SPORT1 Receive Data Secondary	
TSCLK1	I/O	SPORT1 Transmit Serial Clock	D
TFS1	I/O	SPORT1 Transmit Frame Sync	C
DT1PRI	O	SPORT1 Transmit Data Primary	C
DT1SEC	O	SPORT1 Transmit Data Secondary	C
SPI0 Port			
MOSI0	I/O	SPI0 Master Out Slave In	C
MISO0	I/O	SPI0 Master In Slave Out (This pin should always be pulled high through a 4.7 kΩ resistor if booting via the SPI port.)	C
SCK0	I/O	SPI0 Clock	D
UART0 Port			
RX0	I	UART0 Receive	
TX0	O	UART0 Transmit	C
PPI Port			
PPI3–0	I/O	PPI3–0	C
PPI_CLK/*TMRCLK*	I	PPI Clock/*External Timer Reference*	
Port C: *Controller Area Network/GPIO*			
CANTX/*PC0*	I/O 5 V	CAN Transmit/*GPIO*	C
CANRX/*PC1*	I/OD 5 V	CAN Receive/*GPIO*	C[2]
PC[9-5]	I/O	GPIO	C
PC4	I/OD 5 V	GPIO	C[2]

Table 10. Pin Descriptions (Continued)

Pin Name	I/O	Function	Driver Type[1]
PF7/PPI12/*SPI0SEL7*	I/O	GPIO/PPI12/*SPI0 Slave Select Enable 7*	C
PF8/PPI11	I/O	GPIO/PPI11	C
PF9/PPI10	I/O	GPIO/PPI10	C
PF10/PPI9	I/O	GPIO/PPI9	C
PF11/PPI8	I/O	GPIO/PPI8	C
PF12/PPI7	I/O	GPIO/PPI7	C
PF13/PPI6	I/O	GPIO/PPI6	C
PF14/PPI5	I/O	GPIO/PPI5	C
PF15/PPI4	I/O	GPIO/PPI4	C
Real-Time Clock			
RTXI	I	RTC Crystal Input (This pin should be pulled low when not used.)	
RTXO	O	RTC Crystal Output (Does not three-state in hibernate.)	
JTAG Port			
TCK	I	JTAG Clock	
TDO	O	JTAG Serial Data Out	C
TDI	I	JTAG Serial Data In	
TMS	I	JTAG Mode Select	
$\overline{\text{TRST}}$	I	JTAG Reset (This pin should be pulled low if the JTAG port will not be used.)	
$\overline{\text{EMU}}$	O	Emulation Output	C
Clock			
CLKIN	I	Clock/Crystal Input	
XTAL	O	Crystal Output	
Mode Controls			
$\overline{\text{RESET}}$	I	Reset	
$\overline{\text{NMI}}$	I	Nonmaskable Interrupt (This pin should be pulled high when not used.)	
BMODE1–0	I	Boot Mode Strap (These pins must be pulled to the state required for the desired boot mode.)	
Voltage Regulator			
VROUT1–0	O	External FET Drive 0 (These pins should be left unconnected when not used and are driven high during hibernate.)	
$\overline{\text{GPW}}$	I 5 V	General-Purpose Regulator Wake-Up (This pin should be pulled high when not used.)	
Supplies			
V_{DDEXT}	P	I/O Power Supply	
V_{DDINT}	P	Internal Power Supply	
V_{DDRTC}	P	Real-Time Clock Power Supply (This pin should be connected to V_{DDEXT} when not used and should remain powered at all times.)	
GND	G	Ground	

[1] Refer to Figure 33 on Page 47 to Figure 43 on Page 49.

[2] This pin is 5 V-tolerant when configured as an input and an open-drain when configured as an output; therefore, only the VOL curves in Figure 37 on Page 48 and Figure 38 on Page 48 and the Fall Time curves in Figure 50 on Page 51 and Figure 51 on Page 51 apply when configured as an output.

SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nom	Max	Unit
V_{DDINT}	Internal Supply Voltage	533 MHz Speed Grade Models[1, 2]	0.8	1.25	1.375	V
V_{DDINT}	Internal Supply Voltage	400 MHz Speed Grade Models[1, 2]	0.8	1.2	1.32	V
V_{DDEXT}	External Supply Voltage	Models with on-chip flash[2]	2.7	3.3	3.6	V
V_{DDEXT}	External Supply Voltage	Models without on-chip flash[2, 3]	2.25	3.0	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage		2.25		3.6	V
V_{IH}	High Level Input Voltage[4]	V_{DDEXT} = Maximum	2.0			V
V_{IH5V}	High Level Input Voltage[5]	V_{DDEXT} = Maximum	2.0			V
$V_{IHCLKIN}$	High Level Input Voltage[6]	V_{DDEXT} = Maximum	2.2			V
V_{IL}	Low Level Input Voltage[4, 7]	V_{DDEXT} = Minimum			+0.6	V
V_{IL5V}	Low Level Input Voltage [5]	V_{DDEXT} = Minimum			+0.8	V
T_J	Junction Temperature	316-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+110	°C

[1] The regulator can generate V_{DDINT} at levels of 0.85 V to 1.2 V with –5% to +10% tolerance and 1.25 V with –4% to +10% tolerance

[2] See Ordering Guide on Page 58.

[3] When V_{DDEXT} < 2.70 V, on-chip voltage regulation is not supported.

[4] The 3.3 V tolerant pins are capable of accepting up to 3.6 V maximum V_{IH} The following bidirectional pins are 3.3 V tolerant: DATA15–0, SCK2–0, MISO2–0, MOSI2–0, PF15–0, PPI3–0, SPI1SS, SPI1SEL1, PC9–5, SPI2SS, SPI2SEL1, RX2–1, TX2–1, TSCLK3–0, RSCLK3–0, TFS3–0, RFS3–0, DT2PRI, DT2SEC, DR2PRI, DR2SEC, DT3PRI, DT3SEC, DR3PRI, DR3SEC, and TMR2–0. The following input-only pins are 3.3 V tolerant: RESET, RX0, TCK, TDI, TMS, TRST, ARDY, BMODE1–0, BR, DR0PRI, DR0SEC, DR1PRI, DR1SEC, NMI, PPI_CLK, and RTXI.

[5] The 5 V tolerant pins are capable of accepting up to 5.5 V maximum V_{IH}. The following bidirectional pins are 5 V tolerant: SCL0, SCL1, SDA0, SDA1, CANTX, CANRX, and PC4. The following input-only pin is 5 V tolerant: GPW.

[6] Parameter value applies to the CLKIN input pin.

[7] Parameter value applies to all input and bidirectional pins.

The following tables describe the voltage/frequency requirements for the ADSP-BF538/ADSP-BF538F processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock (Table 11 and Table 12) and system clock (Table 14) specifications. Table 13 describes phase-locked loop operating conditions.

Table 11. Core Clock (CCLK) Requirements — 400 MHz Models

Parameter		Internal Regulator Setting	Max	Unit
f_{CCLK}	CLK Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	400	MHz
f_{CCLK}	CLK Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	364	MHz
f_{CCLK}	CLK Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	333	MHz
f_{CCLK}	CLK Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V	280	MHz
f_{CCLK}	CLK Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V	250	MHz

Table 12. Core Clock (CCLK) Requirements — 533 MHz Models

Parameter		Internal Regulator Setting	Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.2 V Minimum)	1.25 V	533	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	500	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	444	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	400	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.85 V Minimum)	0.95 V	333	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V	250	MHz

Table 13. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	50	Max f_{CCLK}	MHz

Table 14. System Clock (SCLK) Requirements

Parameter[1]		Max	Unit
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} ≥ 1.14 V)	133[2]	MHz
f_{SCLK}	CLKOUT/SCLK Frequency (V_{DDINT} < 1.14 V)	100	MHz

[1] t_{SCLK} (= $1/f_{SCLK}$) must be greater than or equal to t_{CCLK}.
[2] Guaranteed to t_{SCLK} = 7.5 ns. See Table 27 on page 33.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed below may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 18. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	−0.3 V to +1.4 V
External (I/O) Supply Voltage (V_{DDEXT})[1]	−0.3 V to +3.8 V
Input Voltage[2, 3]	−0.5 V to +3.6 V
Input Voltage[4, 4]	−0.5 V to +5.5 V
Output Voltage Swing	−0.5 V to V_{DDEXT} + 0.5 V
Junction Temperature While Biased	+125°C
Storage Temperature Range	−65°C to +150°C

[1] Parameter value applies also to V_{DDRTC}.
[2] Applies to 100% transient duty cycle. For other duty cycles, see Table 19.
[3] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2 V.
[4] Applies to pins designated as 5 V tolerant only.

Table 19. Maximum Duty Cycle for Input Transient Voltage[1]

V_{IN} Min (V)[2]	V_{IN} Max (V)[2]	Maximum Duty Cycle[3]
−0.50	+3.80	100%
−0.70	+4.00	40%
−0.80	+4.10	25%
−0.90	+4.20	15%
−1.00	+4.30	10%

[1] Applies to all signal pins with the exception of CLKIN, XTAL, and VROUT1–0.
[2] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.
[3] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 9 and Table 20 provides information about how to read the package brand and relate it to specific product features. For a complete listing of product offerings, see the Ordering Guide on Page 58.

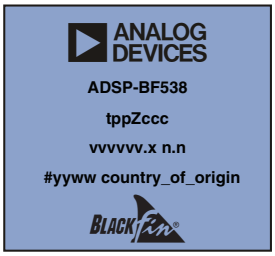


Figure 9. Product Information on Package

Table 20. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

Asynchronous Memory Write Cycle Timing

Table 25 and Table 26 on Page 32 and Figure 14 and Figure 15 on Page 32 describe asynchronous memory write cycle operations for synchronous and for asynchronous ARDY.

Table 25. Asynchronous Memory Write Cycle Timing with Synchronous ARDY

Parameter		Min	Max	Unit
Timing Requirements				
t_{SARDY}	ARDY Setup Before the Falling Edge of CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After the Falling Edge of CLKOUT	0.0		ns
Switching Characteristics				
t_{DDAT}	DATA15–0 Disable After CLKOUT		6.0	ns
t_{ENDAT}	DATA15–0 Enable After CLKOUT	1.0		ns
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT[1]	0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, DATA15–0, $\overline{AOE}$, $\overline{AWE}$.

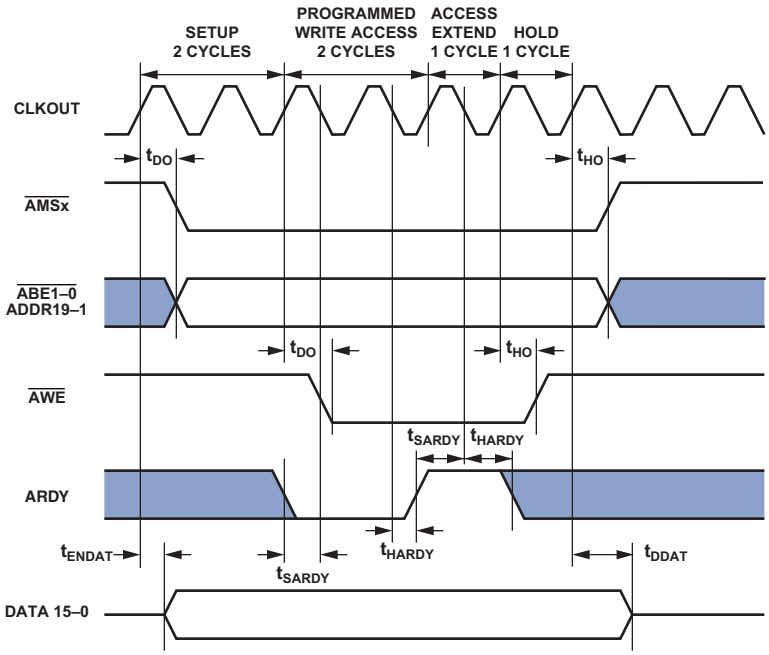


Figure 14. Asynchronous Memory Write Cycle Timing with Synchronous ARDY

External Port Bus Request and Grant Cycle Timing

Table 28 and Table 29 on Page 35 and Figure 17 and Figure 18 on Page 35 describe external port bus request and grant cycle operations for synchronous and for asynchronous $\overline{BR}$.

Table 28. External Port Bus Request and Grant Cycle Timing with Synchronous $\overline{BR}$

Parameter		Min	Max	Unit
Timing Requirements				
t_{BS}	$\overline{BR}$ Setup to Falling Edge of CLKOUT	4.6		ns
t_{BH}	Falling Edge of CLKOUT to $\overline{BR}$ Deasserted Hold Time	1.0		ns
Switching Characteristics				
t_{SD}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Disable		4.5	ns
t_{SE}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Enable		4.5	ns
t_{DBG}	CLKOUT High to $\overline{BG}$ High Setup		4.0	ns
t_{EBG}	CLKOUT High to $\overline{BG}$ Deasserted Hold Time		4.0	ns
t_{DBH}	CLKOUT High to $\overline{BGH}$ High Setup		4.0	ns
t_{EBH}	CLKOUT High to $\overline{BGH}$ Deasserted Hold Time		4.0	ns

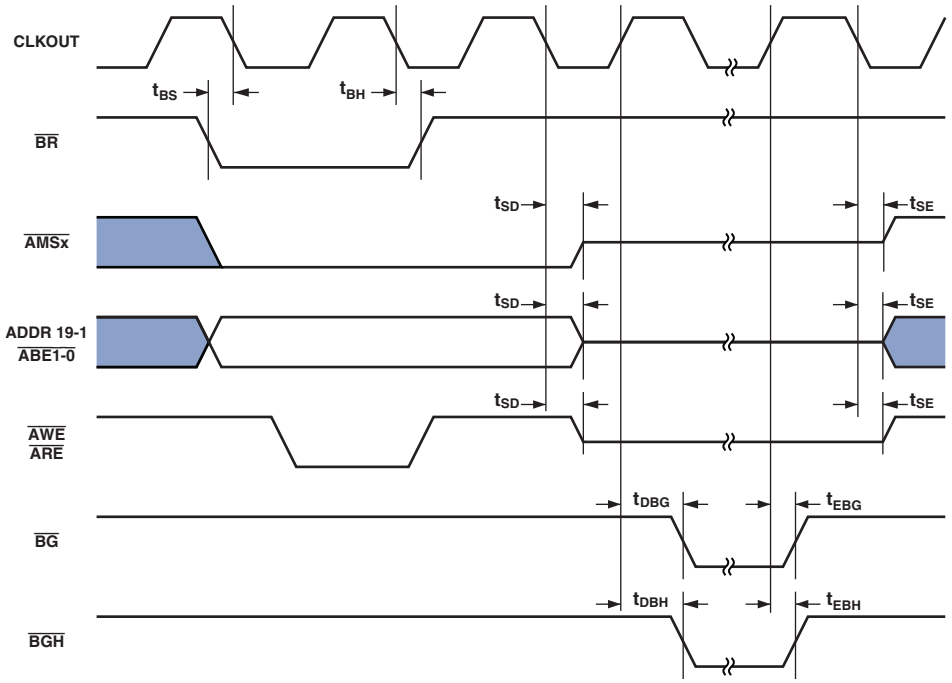


Figure 17. External Port Bus Request and Grant Cycle Timing with Synchronous $\overline{BR}$

Table 33. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	Data Enable Delay from External TSCLKx[1]	0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx[1, 2, 3]		10	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx[1]	–2		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx[1, 2, 3]		3	ns

[1] Referenced to drive edge.
[2] Applicable to multichannel mode only.
[3] TSCLKx is tied to RSCLKx.

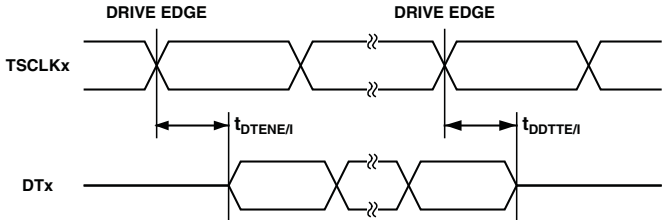


Figure 25. Serial Ports—Enable and Three-State

Serial Peripheral Interface Ports—Slave Timing

Table 36 and Figure 28 describe SPI ports slave operations.

Table 36. Serial Peripheral Interface (SPI) Ports—Slave Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK}$		ns
t_{HDS}	Last SCKx Edge to $\overline{\text{SPIxSS}}$ Not Asserted	$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{\text{SPIxSS}}$ Assertion to First SCKx Edge	$2 \times t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SCKx Edge (Data Input Setup)	2.0		ns
t_{HSPID}	SCKx Sampling Edge to Data Input Invalid	2.0		ns
Switching Characteristics				
t_{DSOE}	$\overline{\text{SPIxSS}}$ Assertion to Data Out Active	0	8	ns
t_{DSDHI}	$\overline{\text{SPIxSS}}$ Deassertion to Data High impedance	0	8	ns
t_{DDSPID}	SCKx Edge to Data Out Valid (Data Out Delay)		10	ns
t_{HDSPID}	SCKx Edge to Data Out Invalid (Data Out Hold)	0		ns

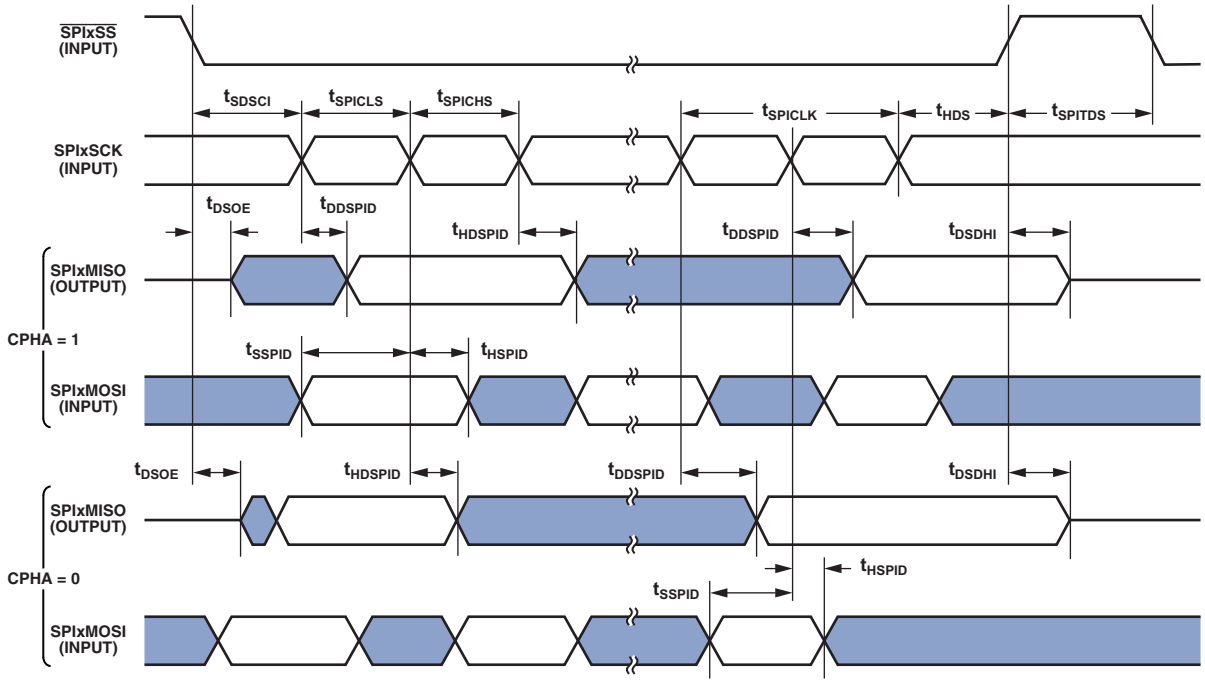


Figure 28. Serial Peripheral Interface (SPI) Ports—Slave Timing

General-Purpose Port Timing

Table 37 and Figure 29 describe general-purpose operations.

Table 37. General-Purpose Port Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WFI}	GP Port Pin Input Pulse Width	t_{SCLK} + 1		ns
Switching Characteristic				
t_{GPOD}	GP Port Pin Output Delay from CLKOUT Low		6	ns

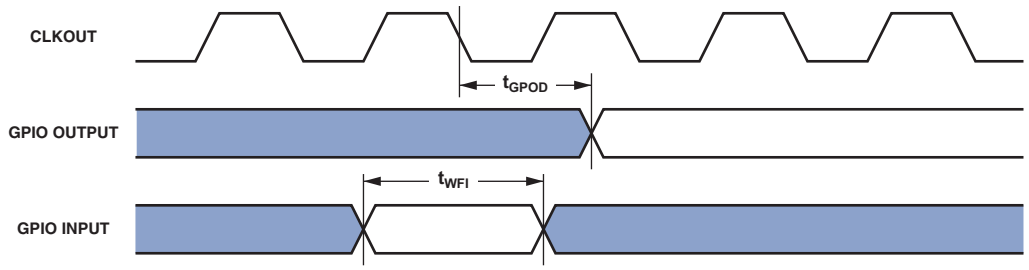


Figure 29. General-Purpose Port Cycle Timing

Timer Clock Timing

Table 38 and Figure 30 describe timer clock timing.

Table 38. Timer Clock Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TODP}	Timer Output Update Delay After PPI_CLK High		12	ns

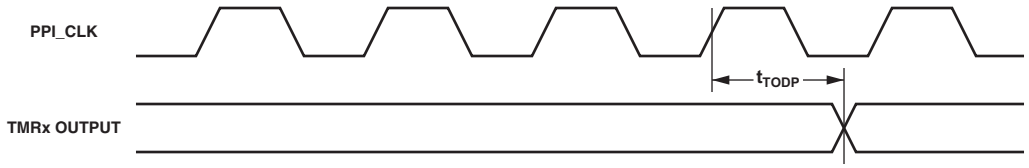


Figure 30. Timer Clock Timing

Timer Cycle Timing

Table 39 and Figure 31 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an absolute maximum input frequency of (f_{SCLK}/2) MHz.

Table 39. Timer Cycle Timing

Parameter		Min	Max	Unit
Timing Characteristics				
t_{WL}	Timer Pulse Width Input Low[1]	1× t_{SCLK}		ns
t_{WH}	Timer Pulse Width Input High[1]	1× t_{SCLK}		ns
t_{TIS}	Timer Input Setup Time Before CLKOUT Low[2]	6.5		ns
t_{TIH}	Timer Input Hold Time After CLKOUT Low[2]	–1		ns
Switching Characteristics				
t_{HTO}	Timer Pulse Width Output	1× t_{SCLK}	(2^{32} – 1) × t_{SCLK}	ns
t_{TOD}	Timer Output Delay After CLKOUT High		6	ns

[1] The minimum pulse widths apply for TMRx signals in width capture and external clock modes.
[2] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize timer flag inputs.

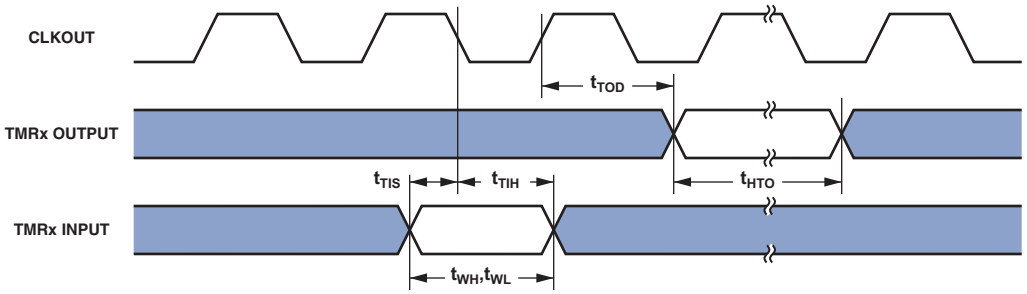


Figure 31. Timer Cycle Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

For information on the UART port receive and transmit operations, see the *ADSP-BF538 Blackfin Processor Hardware Reference*.

JTAG Test and Emulation Port Timing

Table 40 and Figure 32 describe JTAG port operations.

Table 40. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	6		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width[2] (Measured in TCK Cycles)	4		TCK
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3,4]	0	12	ns

[1] System Inputs=ARDY, BMODE1–0, $\overline{\text{BR}}$, DATA15–0, DR0PRI, DR0SEC, $\overline{\text{NMI}}$, PF15–0, PPI_CLK, PPI3–0, SCL1–0, SDA1–0, SCK2–0, MISO2–0, MOSI2–0, $\overline{\text{SPI1SS}}$, $\overline{\text{SPI1SEL1}}$, $\overline{\text{SPI2SS}}$, $\overline{\text{SPI2SEL1}}$, RX2–0, TX2–1, DT2PRI, DT2SEC, DR2PRI, DR2SEC, DT3PRI, DT3SEC, TSCLK3–0, DR3PRI, DR3SEC, RSCLK3–0, RFS3–0, TFS3–0, CANTX, CANRX, $\overline{\text{RESET}}$, PC9–4, $\overline{\text{GPW}}$, and TMR2–0.

[2] 50 MHz maximum

[3] System Outputs = $\overline{\text{AMS}}$, $\overline{\text{AOE}}$, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$, $\overline{\text{ABE}}$, $\overline{\text{BG}}$, DATA15–0, PF15–0, PC9–5, PPI3-0, $\overline{\text{SPI1SS}}$, $\overline{\text{SPI1SEL1}}$, SCK2–0, MISO2–0, MOSI2–0, $\overline{\text{SPI2SS}}$, $\overline{\text{SPI2SEL1}}$, RX2–1, TX2–0, DT2PRI, DT2SEC, DR2PRI, DR2SEC, DT3PRI, DT3SEC, DR3PRI, DR3SEC, RSCLK3–0, RFS3–0, TSCLK3–0, TFS3–0, CANTX, CLKOUT, SA10, $\overline{\text{SCAS}}$, SCKE, $\overline{\text{SMS}}$, $\overline{\text{SRAS}}$, $\overline{\text{SWE}}$, and TMR2–0.

[4] System open-drain outputs: CANRX (when configured as PC1) and PC4.

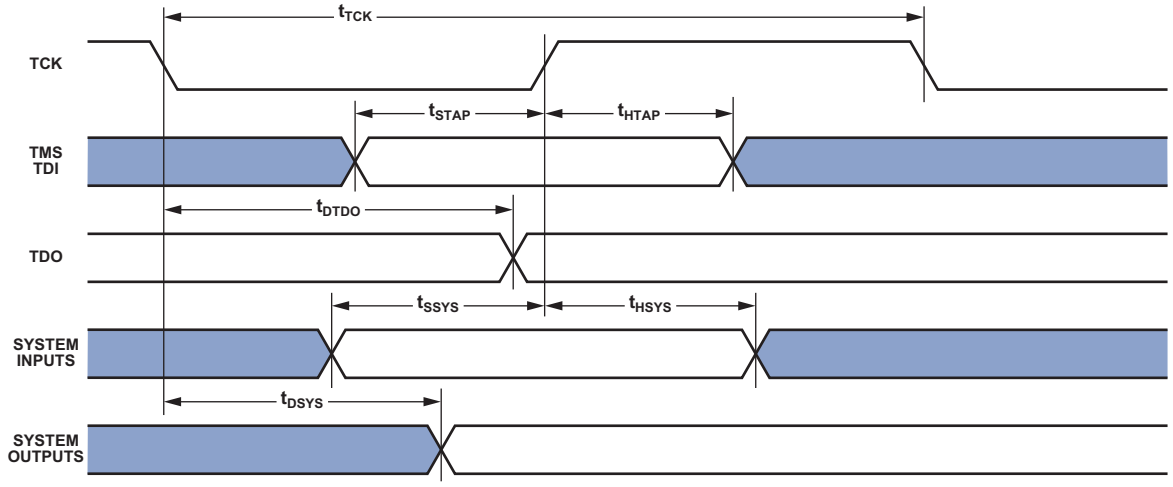


Figure 32. JTAG Port Timing

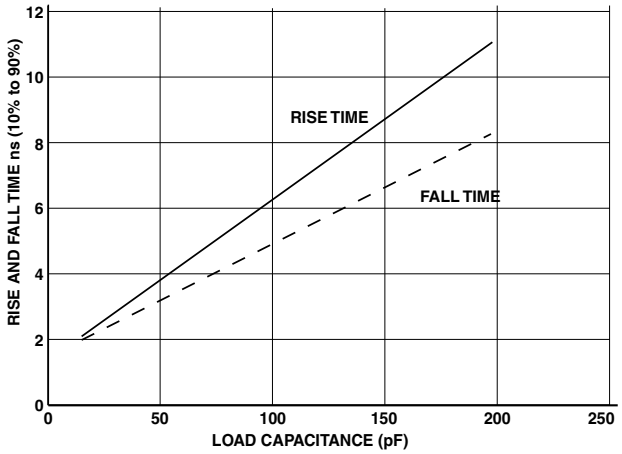


Figure 48. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 2.7 V (Min)

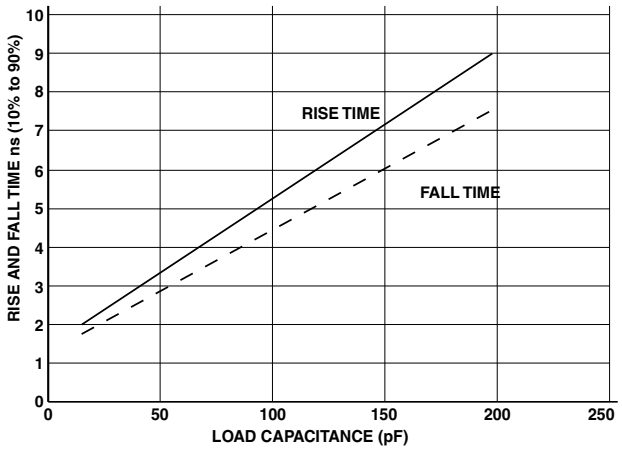


Figure 49. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 3.6 V (Max)

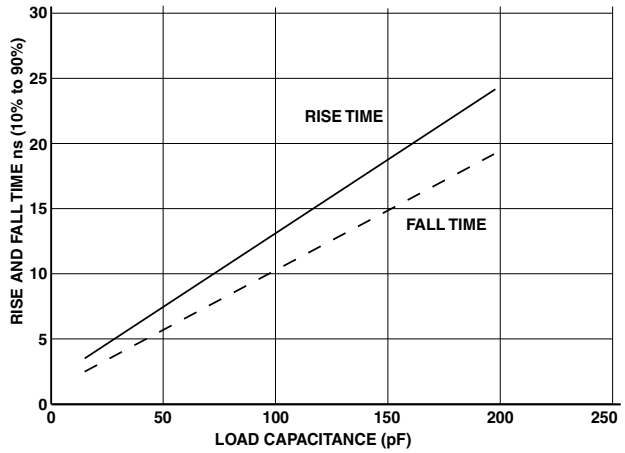


Figure 50. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 2.7 V (Min)

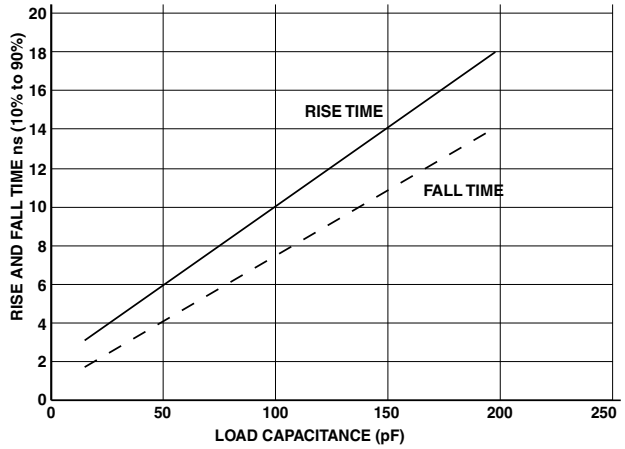


Figure 51. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 3.6 V (Max)