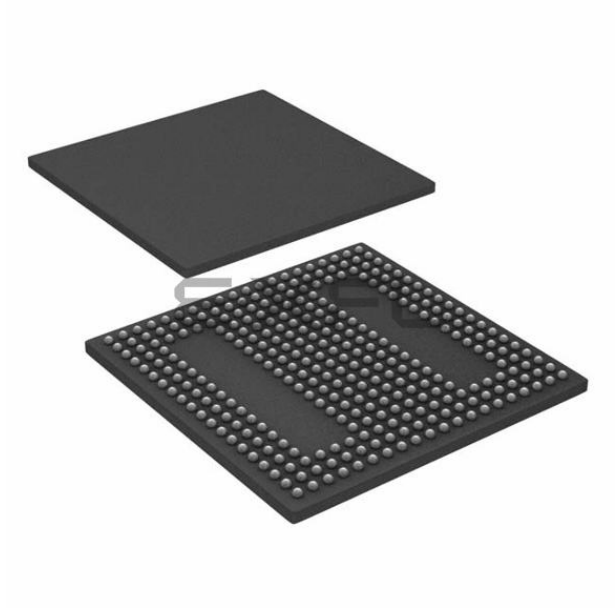

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART
Clock Rate	533MHz
Non-Volatile Memory	FLASH (1MB)
On-Chip RAM	148kB
Voltage - I/O	3.00V, 3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	316-LFBGA, CSPBGA
Supplier Device Package	316-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf538bbcz-5f8

GENERAL DESCRIPTION

The ADSP-BF538/ADSP-BF538F processors are members of the Blackfin® family of products, incorporating the Analog Devices, Inc./Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction set architecture.

The ADSP-BF538/ADSP-BF538F processors are completely code compatible with other Blackfin processors, differing only with respect to performance, peripherals, and on-chip memory. Specific performance, peripherals, and memory configurations are shown in Table 1.

Table 1. Processor Features

Feature	ADSP-BF538	ADSP-BF538F8
SPORTs	4	4
UARTs	3	3
SPI	3	3
TWI	2	2
CAN	1	1
PPI	1	1
Internal 8M bit Parallel Flash	—	1
Instruction SRAM/Cache	16K bytes	16K bytes
Instruction SRAM	64K bytes	64K bytes
Data SRAM/Cache	32K bytes	32K bytes
Data SRAM	32K bytes	32K bytes
Scratchpad	4K bytes	4K bytes
Maximum Frequency	533 MHz 1066 MMACS	533 MHz 1066 MMACS
Package Option	BC-316	BC-316

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next generation applications that require RISC-like programmability, multimedia support, and leading edge signal processing in one integrated package.

LOW POWER ARCHITECTURE

Blackfin processors provide world class power management and performance. They are designed using a low power and low voltage methodology and feature dynamic power management, which is the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. Varying the voltage and frequency can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This translates into longer battery life and lower heat dissipation.

SYSTEM INTEGRATION

The ADSP-BF538/ADSP-BF538F processors are highly integrated system-on-a-chip solutions for the next generation of consumer and industrial applications including audio and video signal processing. By combining advanced memory configurations, such as on-chip flash memory, industry-standard interfaces, and a high performance signal processing core, cost-effective solutions can be quickly developed, without the need for costly external components. The system peripherals include three UART ports, three SPI ports, four serial ports (SPORTs), one CAN interface, two 2-wire interfaces (TWI), four general-purpose timers (three with PWM capability), a real-time clock, a watchdog timer, a parallel peripheral interface (PPI), and general-purpose I/O pins.

ADSP-BF538/ADSP-BF538F PROCESSOR PERIPHERALS

The ADSP-BF538/ADSP-BF538F processors contain a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram 1). The general-purpose peripherals include functions such as UART, timers with PWM (pulse-width modulation) and pulse measurement capability, general-purpose I/O pins, a real-time clock, and a watchdog timer. This set of functions satisfies a wide variety of typical system support needs and is augmented by the system expansion capabilities of the device. In addition to these general-purpose peripherals, the processors contain high speed serial and parallel ports for interfacing to a variety of audio, video, and modem codec functions. A CAN 2.0B controller is provided for automotive and industrial control networks. An interrupt controller manages interrupts from the on-chip peripherals or from external sources. Power management control functions tailor the performance and power characteristics of the processors and system to many application scenarios.

All of the peripherals, except for general-purpose I/O, CAN, TWI, real-time clock, and timers, are supported by a flexible DMA structure. There are also four separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses running at up to 133 MHz provide enough bandwidth to keep the processor core running with activity on all of the on-chip and external peripherals.

The ADSP-BF538/ADSP-BF538F processors include an on-chip voltage regulator in support of the processor's dynamic power management capability. The voltage regulator provides a range of core voltage levels from V_{DDEXT}. The voltage regulator can be bypassed as needed.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C style indexed stack manipulation).

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management Unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

MEMORY ARCHITECTURE

The ADSP-BF538/ADSP-BF538F processors view memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low latency on-chip memory as cache or SRAM, and larger, lower cost and performance off-chip memory systems. See Figure 3.

The L1 memory system is the primary highest performance memory available to the Blackfin processor. The off-chip memory system, accessed through the External Bus Interface Unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing up to 132M bytes of physical memory.

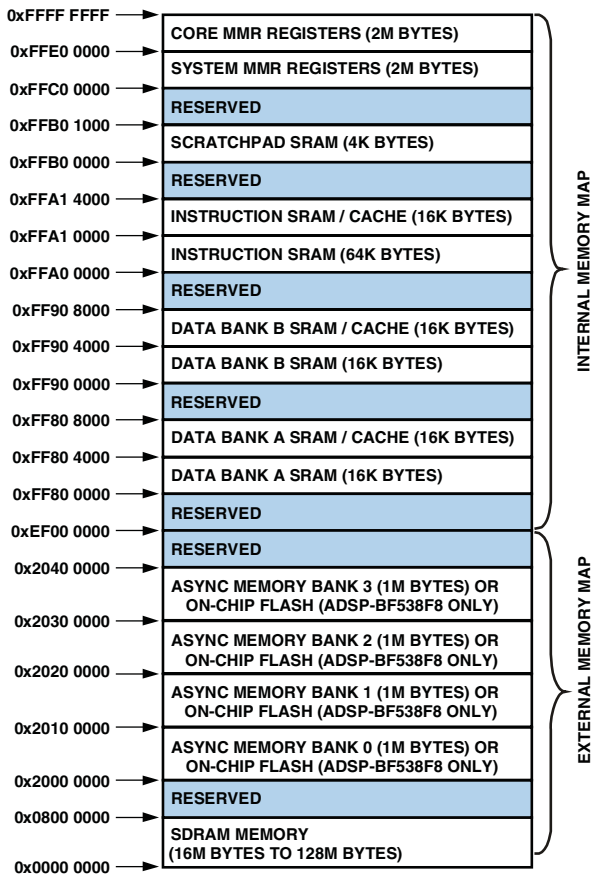


Figure 3. ADSP-BF538/ADSP-BF538F Internal/External Memory Map

The memory DMA controllers provide high bandwidth data movement capability. They can perform block transfers of code or data between the internal memory and the external memory spaces.

Internal (On-Chip) Memory

The ADSP-BF538/ADSP-BF538F processors have three blocks of on-chip memory, providing high bandwidth access to the core.

The first is the L1 instruction memory, consisting of 80K bytes SRAM, of which 16K bytes can be configured as a four way set-associative cache. This memory is accessed at full processor speed.

The second on-chip memory block is the L1 data memory, consisting of two banks of up to 32K bytes each. Each memory bank is configurable, offering both two-way set-associative cache and SRAM functionality. This memory block is accessed at full processor speed.

The third memory block is a 4K byte scratchpad SRAM, which runs at the same speed as the L1 memories, but is only accessible as data SRAM and cannot be configured as cache memory.

Table 3. System and Core Event Mapping (Continued)

Event Source	Core Event Name
DMA10 Interrupt (SPORT3 Rx)	IVG9
DMA11 Interrupt (SPORT3 Tx)	IVG9
DMA5 Interrupt (SPI0)	IVG10
DMA14 Interrupt (SPI1)	IVG10
DMA15 Interrupt (SPI2)	IVG10
DMA6 Interrupt (UART0 Rx)	IVG10
DMA7 Interrupt (UART0 Tx)	IVG10
DMA16 Interrupt (UART1 Rx)	IVG10
DMA17 Interrupt (UART1 Tx)	IVG10
DMA18 Interrupt (UART2 Rx)	IVG10
DMA19 Interrupt (UART2 Tx)	IVG10
Timer0, Timer1, Timer2 Interrupts	IVG11
TWI0 Interrupt	IVG11
TWI1 Interrupt	IVG11
CAN Receive Interrupt	IVG11
CAN Transmit Interrupt	IVG11
Port F GPIO Interrupts A and B	IVG12
MDMA0 Stream 0 Interrupt	IVG13
MDMA0 Stream 1 Interrupt	IVG13
MDMA1 Stream 0 Interrupt	IVG13
MDMA1 Stream 1 Interrupt	IVG13
Software Watchdog Timer	IVG13

Event Control

The ADSP-BF538/ADSP-BF538F processors provide the user with a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 32 bits wide:

- CEC interrupt latch register (ILAT) – The ILAT register indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it may also be written to clear (cancel) latched events. This register may be read while in supervisor mode and may only be written while in supervisor mode when the corresponding IMASK bit is cleared.
- CEC interrupt mask register (IMASK) – The IMASK register controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and will be processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be latched in the ILAT register. This register may be read or written while in supervisor mode. General-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.
- CEC interrupt pending register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but may be read while in supervisor mode.

The SIC allows further control of event processing by providing three 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in Table 3 on Page 7.

- SIC interrupt mask registers (SIC_IMASKx) – These registers control the masking and unmasking of each peripheral interrupt event. When a bit is set in these registers, that peripheral event is unmasked and will be processed by the system when asserted. A cleared bit in these registers masks the peripheral event, preventing the processor from servicing the event.
- SIC interrupt status registers (SIC_ISRx) – As multiple peripherals can be mapped to a single event, these registers allow the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt, and a cleared bit indicates the peripheral is not asserting the event.
- SIC interrupt wake-up enable registers (SIC_IWRx) – By enabling the corresponding bit in these registers, a peripheral can be configured to wake up the processor, should the core be idled or in sleep mode when the event is generated. (For more information, see Dynamic Power Management on Page 13.)

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SICs as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC will recognize and queue the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

DMA CONTROLLERS

The ADSP-BF538/ADSP-BF538F processors have two, independent DMA controllers that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor internal memories and any of its DMA capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA capable peripherals and external devices connected to the external memory inter-

timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the PF1 pin (TACLK), an external clock input to the PPI_CLK pin (TMRCLK), or to the internal SCLK.

The timer units can be used in conjunction with UART0 to measure the width of the pulses in the data stream to provide an auto-baud detect function for a serial channel.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the three general-purpose programmable timers, a fourth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

SERIAL PORTS (SPORTs)

The ADSP-BF538/ADSP-BF538F processors incorporate four dual-channel synchronous serial ports for serial and multiprocessor communications. The SPORTs support the following features:

- I^2S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling 16 channels of I^2S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131,070) Hz to (f_{SCLK}/2) Hz.
- Word length – Each SPORT supports serial data words from 3 bits to 32 bits in length, transferred most significant bit first or least significant bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer or buffers through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1024 channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

SERIAL PERIPHERAL INTERFACE (SPI) PORTS

The ADSP-BF538/ADSP-BF538F processors incorporate three SPI-compatible ports that enable the processor to communicate with multiple SPI compatible devices.

The SPI interface uses three pins for transferring data: two data pins (master output-slave input, MOSIx, and master input-slave output, MISOx) and a clock pin (serial clock, SCKx). An SPI chip select input pin ($\overline{\text{SPIxSS}}$) lets other SPI devices select the processor. For SPI0, seven SPI chip select output pins ($\overline{\text{SPI0SEL7–1}}$) let the processor select other SPI devices. SPI1 and SPI2 each have a single SPI chip select output pin ($\overline{\text{SPI1SEL1}}$ and $\overline{\text{SPI2SEL1}}$) for SPI point-to-point communication. Each of the SPI select pins are reconfigured GPIO pins. Using these pins, the SPI ports provide a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI ports' baud rate and clock phase/polarities are programmable, and they each have an integrated DMA controller, configurable to support transmit or receive data streams. Each SPI's DMA controller can only service unidirectional accesses at any given time.

The SPI port's clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPIx\_BAUD}$$

where the 16-bit *SPIx_BAUD* register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

2-WIRE INTERFACE

The ADSP-BF538/ADSP-BF538F processors have two 2-wire interface (TWI) modules that are compatible with the Philips Inter-IC bus standard. The TWI modules offer the capabilities of simultaneous master and slave operation, support for 7-bit addressing and multimedia data arbitration. The TWI also includes master clock synchronization and support for clock low extension.

The TWI interface uses two pins for transferring clock (SCLx) and data (SDAx) and supports the protocol at speeds up to 400 kbps.

The TWI interface pins are compatible with 5 V logic levels.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bidirectional data transfer with up to 16 bits of data. Up to 3 frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex, bi-directional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. Three distinct submodes are supported:

- Input mode – frame syncs and data are inputs into the PPI.
- Frame capture mode – frame syncs are outputs from the PPI, but data are inputs.
- Output mode – frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit, and 10-bit through 16-bit data, and is programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (e.g., for frame capture). The ADSP-BF538/ADSP-BF538F processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct submodes are supported:

- Active video only mode
- Vertical blanking only mode
- Entire field mode

Active Video Only Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1.

CONTROLLER AREA NETWORK (CAN) INTERFACE

The ADSP-BF538/ADSP-BF538F processors provide a CAN controller that is a communication controller implementing the Controller Area Network (CAN) V2.0B protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. CAN is well suited for control applications due to its capability to communicate reliably over a network since the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The CAN controller is based on a 32-entry mailbox RAM and supports both the standard and extended identifier (ID) message formats specified in the CAN protocol specification, revision 2.0, part B.

Each mailbox consists of eight 16-bit data words. The data is divided into fields, which includes a message identifier, a time stamp, a byte count, up to 8 bytes of data, and several control bits. Each node monitors the messages being passed on the network. If the identifier in the transmitted message matches an identifier in one of its mailboxes, then the module knows that the message was meant for it, passes the data into its appropriate mailbox, and signals the processor of message arrival with an interrupt.

The CAN controller can wake up the processor from sleep mode upon generation of a wake-up event, such that the processor can be maintained in a low power mode during idle conditions. Additionally, a CAN wake-up event can wake up the on-chip internal voltage regulator from the powered-down hibernate state.

The electrical characteristics of each network connection are very stringent, therefore the CAN interface is typically divided into 2 parts: a controller and a transceiver. This allows a single controller to support different drivers and CAN networks. The ADSP-BF538/ADSP-BF538F CAN module represents the controller part of the interface. This module's network I/O is a single transmit output and a single receive input, which connect to a line transceiver.

internal logic except for the RTC logic. The 3.3 V V_{DDEXT} power domain supplies all the I/O except for the RTC crystal. There are no sequencing requirements for the various power domains.

Table 6. Power Domains

Power Domain	V_{DD} Range
RTC Crystal I/O and Logic	V_{DDRTC}
All Internal Logic Except RTC	V_{DDINT}
All I/O Except RTC	V_{DDEXT}

The V_{DDRTC} should either be connected to a battery (if the RTC is to operate while the rest of the chip is powered down) or should be connected to the V_{DDEXT} plane on the board. The V_{DDRTC} should remain powered when the processor is in hibernate state, and should also be powered even if the RTC functionality is not being used in an application.

The power dissipated by a processor is largely a function of the clock frequency of the processor and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic.

The dynamic power management feature of the processor allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The savings in power dissipation can be modeled using the power savings factor and % power savings calculations.

The power savings factor is calculated as

$$\text{Power Savings Factor} = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{t_{RED}}{t_{NOM}}\right)$$

where:

$f_{CCLKNOM}$ is the nominal core clock frequency.

$f_{CCLKRED}$ is the reduced core clock frequency.

$V_{DDINTNOM}$ is the nominal internal supply voltage.

$V_{DDINTRED}$ is the reduced internal supply voltage.

t_{NOM} is the duration running at $f_{CCLKNOM}$.

t_{RED} is the duration running at $f_{CCLKRED}$.

The power savings factor is calculated as

$$\%\ \text{Power Savings} = (1 - \text{Power Savings Factor}) \times 100\%$$

VOLTAGE REGULATION

The Blackfin processors provide an on-chip voltage regulator that can generate appropriate V_{DDINT} voltage levels from the V_{DDEXT} supply. See Operating Conditions on Page 23 for regulator tolerances and acceptable V_{DDEXT} ranges for specific models.

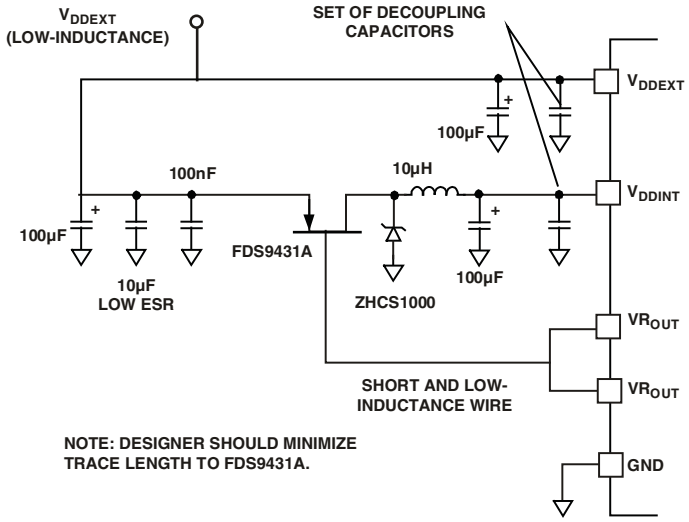


Figure 6. Voltage Regulator Circuit

The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while I/O power (V_{DDRTC}, V_{DDEXT}) is still supplied. While in the hibernate state, I/O power is still being applied, eliminating the need for external buffers. The voltage regulator can be activated from this power-down state either through an RTC wake-up, a CAN wake-up, a general-purpose wake-up, or by asserting $\overline{\text{RESET}}$, all of which will then initiate a boot sequence. The regulator can also be disabled and bypassed at the user's discretion.

Voltage Regulator Layout Guidelines

Regulator external component placement, board routing, and bypass capacitors all have a significant effect on noise injected into the other analog circuits on-chip. The VROUT1–0 traces and voltage regulator external components should be considered as noise sources when doing board layout and should not be routed or placed near sensitive circuits or components on the board. All internal and I/O power supplies should be well bypassed with bypass capacitors placed as close to the ADSPBF538/ADSP-BF538F processors as possible.

For further details on the on-chip voltage regulator and related board design guidelines, see the Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processor (EE-228) applications note on the Analog Devices website (www.analog.com)—use site search on "EE-228".

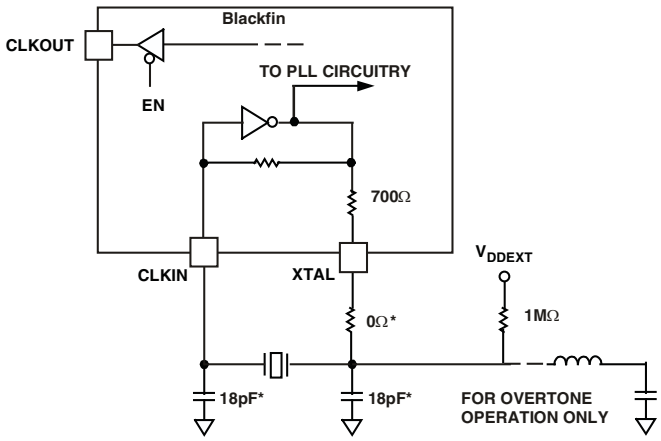
CLOCK SIGNALS

The ADSP-BF538/ADSP-BF538F processors can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the ADSP-BF538/ADSP-BF538F processors include an on-chip oscillator circuit, an external crystal may be used. For fundamental frequency operation, use the circuit shown in Figure 7. A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kW range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor, shown in Figure 7, fine tune the phase and amplitude of the sine frequency. The capacitor and resistor values, shown in Figure 7, are typical values only. The capacitor values are dependent upon the crystal manufacturer's load capacitance recommendations and the physical PCB layout. The resistor value depends on the drive level specified by the crystal manufacturer. System designs should verify the customized values based on careful investigation on multiple devices over the allowed temperature range.

A third-overtone crystal can be used at frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 7.



NOTE: VALUES MARKED WITH * MUST BE CUSTOMIZED DEPENDING ON THE CRYSTAL AND LAYOUT. PLEASE ANALYZE CAREFULLY.

Figure 7. External Crystal Connections

As shown in Figure 8, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a user programmable 0.5× to 64× multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 10×, but it can be modified by a software instruction sequence. On-the-fly frequency changes can be effected by simply writing to the PLL_DIV register.

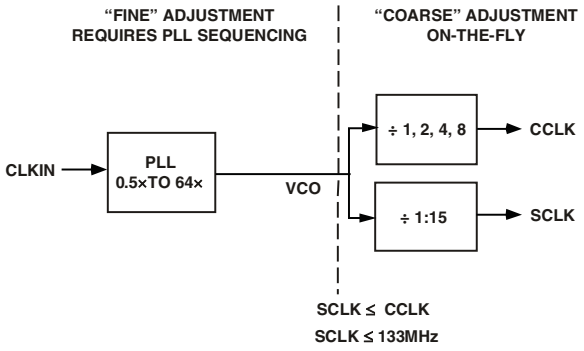


Figure 8. Frequency Modification Methods

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15.

Table 7 illustrates typical system clock ratios:

Table 7. Example System Clock Ratios

Signal Name SSEL3–0	Divider Ratio VCO/SCLK	Example Frequency Ratios (MHz)	
		VCO	SCLK
0001	1:1	100	100
0110	6:1	300	50
1010	10:1	500	50

The maximum frequency of the system clock is f_{SCLK}. Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV).

Note that when the SSEL value is changed, it will affect all the peripherals that derive their clock signals from the SCLK signal.

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 8. This programmable core clock capability is useful for fast core frequency modifications.

Table 8. Core Clock Ratios

Signal Name CSEL1–0	Divider Ratio VCO/CCLK	Example Frequency Ratios	
		VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	500	125
11	8:1	200	25

ELECTRICAL CHARACTERISTICS

Parameter[1]		Test Conditions	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage[2]	V_{DDEXT} = +3.0 V, I_{OH} = –0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage[2]	V_{DDEXT} = 3.0 V, I_{OL} = 2.0 mA			0.4	V
I_{IH}	High Level Input Current[3]	V_{DDEXT}= Maximum, V_{IN} = V_{DD} Maximum			10.0	µA
I_{IHP}	High Level Input Current JTAG[4]	V_{DDEXT} = Maximum, V_{IN} = V_{DD} Maximum			50.0	µA
I_{IL}	Low Level Input Current[3]	V_{DDEXT} = Maximum, V_{IN} = 0 V			10.0	µA
I_{OZH}	Three-State Leakage Current[5]	V_{DDEXT} = Maximum, V_{IN} = V_{DD} Maximum			10.0	µA
I_{OZL}	Three-State Leakage Current[5]	V_{DDEXT} = Maximum, V_{IN} = 0 V			10.0	µA
C_{IN}	Input Capacitance[6, 7]	f_{CCLK} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		4	8	pF
$I_{DDDEEPSLEEP}$[8]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.0 V, f_{CCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		7.5		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 0.8 V, T_J = 25°C, SCLK = 25 MHz			10	mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.14 V, f_{CCLK} = 400 MHz, T_J = 25°C		130		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.2 V, f_{CCLK} = 500 MHz, T_J = 25°C		168		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.2 V, f_{CCLK} = 533 MHz, T_J = 25°C		180		mA
$I_{DDHIBERNATE}$[8]	V_{DDEXT} Current in Hibernate State	V_{DDEXT} = 3.6 V, CLKIN = 0 MHz, T_J = Max, voltage regulator off (V_{DDINT} = 0 V)		50	100	µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J = 25°C		20		µA
$I_{DDDEEPSLEEP}$[8]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz		6	Table 15	mA
I_{DDINT}[9]	V_{DDINT} Current	f_{CCLK} > 0 MHz			$I_{DDDEEPSLEEP}$ + (Table 17 × ASF)	mA

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins.
[3] Applies to input pins except JTAG inputs.
[4] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{TRST}$).
[5] Applies to three-statable pins.
[6] Applies to all signal pins.
[7] Guaranteed, but not tested.
[8] See the *ADSP-BF538/538F Blackfin Processor Hardware Reference* for definitions of sleep, deep sleep, and hibernate operating modes.
[9] See Table 16 for the list of I_{DDINT} power vectors covered by various Activity Scaling Factors (ASF).

System designers should refer to *Estimating Power for the ADSP-BF538/BF539 Blackfin Processors (EE-298)*, which provides detailed information for optimizing designs for lowest power. All topics discussed in this section are described in detail in EE-298. Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 25 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 15), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 17).

The dynamic component is also subject to an Activity Scaling Factor (ASF) which represents application code running on the processor (Table 16).

Table 15. Static Current (mA)[1]

	V_{DDINT} (V)												
T_J (°C)	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V
–40	6.4	7.7	8.8	10.4	12.0	14.0	16.1	18.9	21.9	25.2	28.7	30.6	35.9
–25	9.2	10.9	12.5	14.5	16.7	19.3	22.1	25.6	29.5	33.7	38.1	40.5	47.2
0	16.8	18.9	21.5	24.4	27.7	31.7	35.8	40.5	45.8	51.6	58.2	61.0	69.8
25	32.9	37.2	41.4	46.2	51.8	57.4	64.2	72.3	80.0	89.3	98.9	103.3	116.4
40	48.4	54.8	60.5	67.1	74.7	82.9	91.6	101.5	112.4	123.2	136.2	142.0	158.7
55	71.2	78.6	86.5	95.8	104.9	115.7	127.1	139.8	153.6	168.0	183.7	191.0	211.8
70	102.3	112.2	122.1	133.5	146.1	159.2	173.9	189.8	206.7	225.5	245.6	254.1	279.6
85	140.7	153.0	167.0	182.5	198.0	216.0	234.3	254.0	276.0	299.1	324.3	334.8	366.6
100	190.6	207.1	224.6	244.0	265.6	285.7	309.0	333.7	360.0	387.8	417.3	431.1	469.3
105	210.2	228.1	245.1	265.6	285.8	309.2	334.0	360.1	385.6	417.2	448.0	461.5	501.1

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.

Table 16. Activity Scaling Factors

I_{DDINT} Power Vector[1]	Activity Scaling Factor (ASF)[2]
$I_{DD-PEAK}$	1.30
$I_{DD-HIGH}$	1.28
I_{DD-TYP}	1.00
I_{DD-APP}	0.88
I_{DD-NOP}	0.74
$I_{DD-IDLE}$	0.48

[1] See EE-298 for power vector definitions.
[2] All ASF values determined using a 10:1 CCLK:SCLK ratio.

Table 17. Dynamic Current (mA, with ASF = 1.0)[1]

Frequency (MHz)	Voltage (V_{DDINT})												
	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V
50	13.6	14.9	16.4	17.5	19.1	20.5	22.0	23.5	25.4	27.1	29.1	29.7	31.6
100	23.6	26.0	27.9	30.1	32.3	34.4	37.0	39.2	41.7	44.3	46.4	47.6	50.3
200	44.1	47.5	51.0	54.8	58.4	61.8	65.6	69.7	74.3	76.2	82.2	83.4	87.8
250	54.6	58.7	62.8	66.8	71.2	75.7	79.9	84.5	89.8	94.2	99.4	101.2	106.5
300	N/A	69.8	74.1	79.3	84.5	89.0	94.7	100.0	105.5	111.6	116.8	119.3	125.5
375	N/A	N/A	91.9	97.9	103.9	109.9	116.5	122.2	129.7	136.0	142.9	145.9	153.6
400	N/A	N/A	N/A	103.8	110.3	116.9	123.7	130.0	137.5	144.2	151.2	154.5	162.4
425	N/A	N/A	N/A	N/A	116.6	123.7	130.9	137.2	144.7	152.7	159.9	163.3	171.8
475	N/A	N/A	N/A	N/A	N/A	N/A	145.0	151.8	161.4	169.4	177.8	181.1	190.4
500	N/A	N/A	N/A	N/A	N/A	N/A	N/A	159.9	168.9	177.8	186.3	190.0	199.6
533	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	179.8	188.9	198.8	202.2	212.5

[1] The values are not guaranteed as standalone maximum specifications, they must be combined with static current per the equations of Electrical Characteristics on Page 25.

Asynchronous Memory Write Cycle Timing

Table 25 and Table 26 on Page 32 and Figure 14 and Figure 15 on Page 32 describe asynchronous memory write cycle operations for synchronous and for asynchronous ARDY.

Table 25. Asynchronous Memory Write Cycle Timing with Synchronous ARDY

Parameter		Min	Max	Unit
Timing Requirements				
t_{SARDY}	ARDY Setup Before the Falling Edge of CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After the Falling Edge of CLKOUT	0.0		ns
Switching Characteristics				
t_{DDAT}	DATA15–0 Disable After CLKOUT		6.0	ns
t_{ENDAT}	DATA15–0 Enable After CLKOUT	1.0		ns
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT[1]	0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, DATA15–0, $\overline{AOE}$, $\overline{AWE}$.

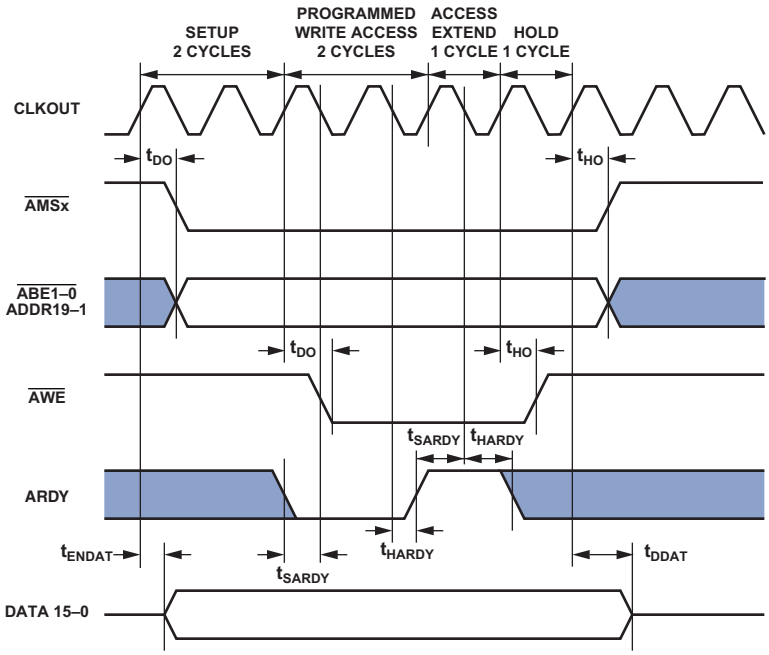


Figure 14. Asynchronous Memory Write Cycle Timing with Synchronous ARDY

External Port Bus Request and Grant Cycle Timing

Table 28 and Table 29 on Page 35 and Figure 17 and Figure 18 on Page 35 describe external port bus request and grant cycle operations for synchronous and for asynchronous $\overline{BR}$.

Table 28. External Port Bus Request and Grant Cycle Timing with Synchronous $\overline{BR}$

Parameter		Min	Max	Unit
Timing Requirements				
t_{BS}	$\overline{BR}$ Setup to Falling Edge of CLKOUT	4.6		ns
t_{BH}	Falling Edge of CLKOUT to $\overline{BR}$ Deasserted Hold Time	1.0		ns
Switching Characteristics				
t_{SD}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Disable		4.5	ns
t_{SE}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Enable		4.5	ns
t_{DBG}	CLKOUT High to $\overline{BG}$ High Setup		4.0	ns
t_{EBG}	CLKOUT High to $\overline{BG}$ Deasserted Hold Time		4.0	ns
t_{DBH}	CLKOUT High to $\overline{BGH}$ High Setup		4.0	ns
t_{EBH}	CLKOUT High to $\overline{BGH}$ Deasserted Hold Time		4.0	ns

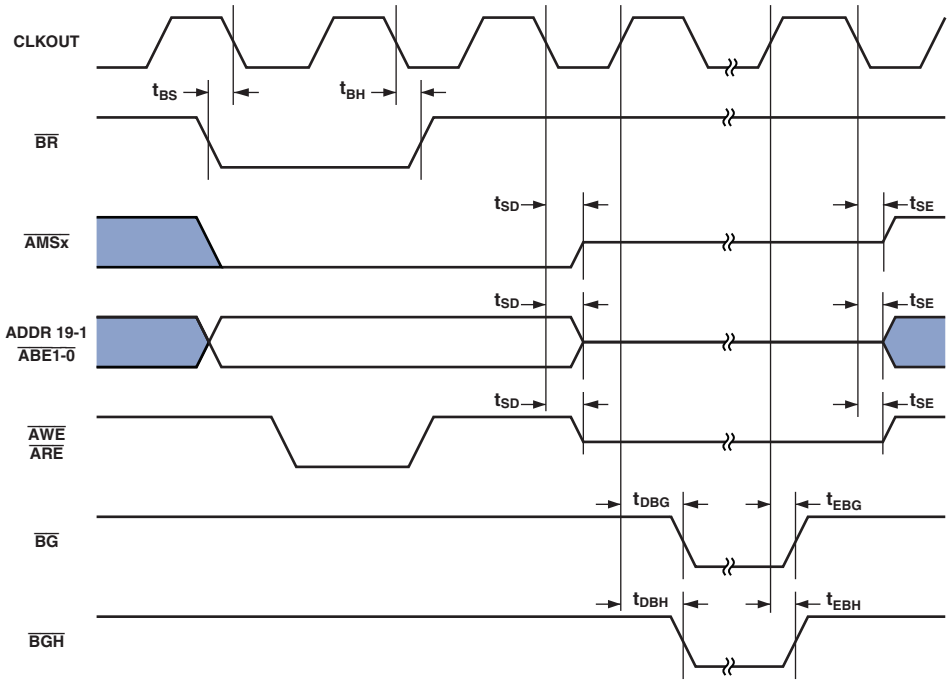


Figure 17. External Port Bus Request and Grant Cycle Timing with Synchronous $\overline{BR}$

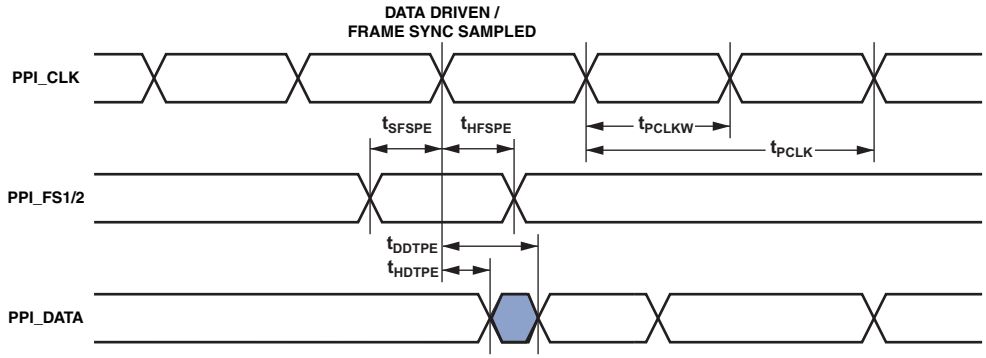


Figure 21. PPI GP Tx Mode with External Frame Sync Timing

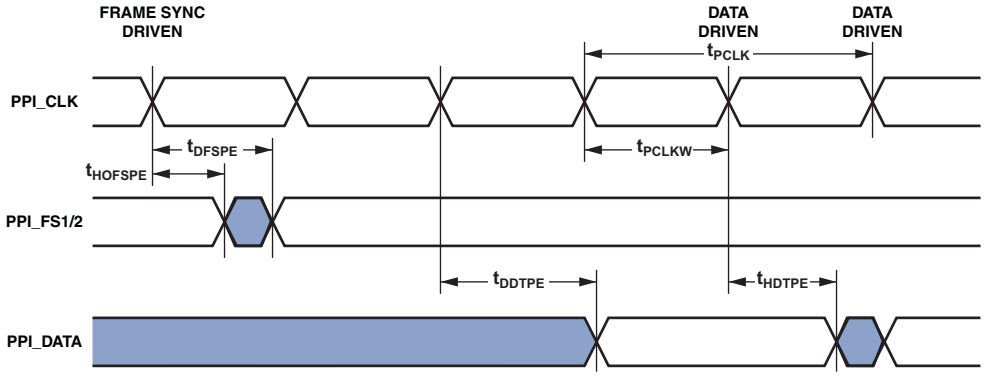


Figure 22. PPI GP Tx Mode with Internal Frame Sync Timing

Serial Port Timing

Table 31 through Table 34 on Page 41 and Figure 23 on Page 39 through Figure 26 on Page 41 describe serial port operations.

Table 31. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}	TFSx/RFSx Setup Before TSCLKx/RSCLKx (Externally Generated TFSx/RFSx)[1]	3.0		ns
t_{HFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Externally Generated TFSx/RFSx)[1]	3.0		ns
t_{SDRE}	Receive Data Setup Before RSCLKx[1]	3.0		ns
t_{HDRE}	Receive Data Hold After RSCLKx[1]	3.0		ns
t_{SCLKEW}	TSCLKx/RSCLKx Width	4.5		ns
t_{SCLKE}	TSCLKx/RSCLKx Period	15.0		ns
t_{SUDTE}	Start-Up Delay From SPORT Enable To First External TFSx[2]	$4.0 \times t_{SCLKE}$		ns
t_{SUDRE}	Start-Up Delay From SPORT Enable To First External RFSx[2]	$4.0 \times t_{SCLKE}$		ns
Switching Characteristics				
t_{DFSE}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[3]		10.0	ns
t_{HOFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[3]	0.0		ns
t_{DDTE}	Transmit Data Delay After TSCLKx[3]		10.0	ns
t_{HDTE}	Transmit Data Hold After TSCLKx[3]	0.0		ns

[1] Referenced to sample edge.
[2] Verified in design but untested. After being enabled, the serial port requires external clock pulses—before the first external frame sync edge—to initialize the serial port.
[3] Referenced to drive edge.

Table 32. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}	TFSx/RFSx Setup Before TSCLKx/RSCLKx (Externally Generated TFSx/RFSx)[1]	9.0		ns
t_{HFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Externally Generated TFSx/RFSx)[1]	–1.5		ns
t_{SDRI}	Receive Data Setup Before RSCLKx[1]	9.0		ns
t_{HDRI}	Receive Data Hold After RSCLKx[1]	–1.5		ns
Switching Characteristics				
t_{DFSI}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]		3.5	ns
t_{HOFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]	–1.0		ns
t_{DDTI}	Transmit Data Delay After TSCLKx[2]		3.0	ns
t_{HDTI}	Transmit Data Hold After TSCLKx[2]	–2.0		ns
t_{SCLKIW}	TSCLKx/RSCLKx Width	4.5		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Serial Peripheral Interface Ports—Master Timing

Table 35 and Figure 27 describe SPI ports master operations.

Table 35. Serial Peripheral Interface (SPI) Ports—Master Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SCKx Edge (Data Input Setup)	9.0		ns
t_{HSPIDM}	SCKx Sampling Edge to Data Input Invalid	–1.5		ns
Switching Characteristics				
t_{SDSCIM}	$\overline{SPIxSELy}$ Low to First SCKx edge	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCKx Edge to $\overline{SPIxSELy}$ High	$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCKx Edge to Data Out Valid (Data Out Delay)		5	ns
$t_{HDSPIDM}$	SCKx Edge to Data Out Invalid (Data Out Hold)	–1.0		ns

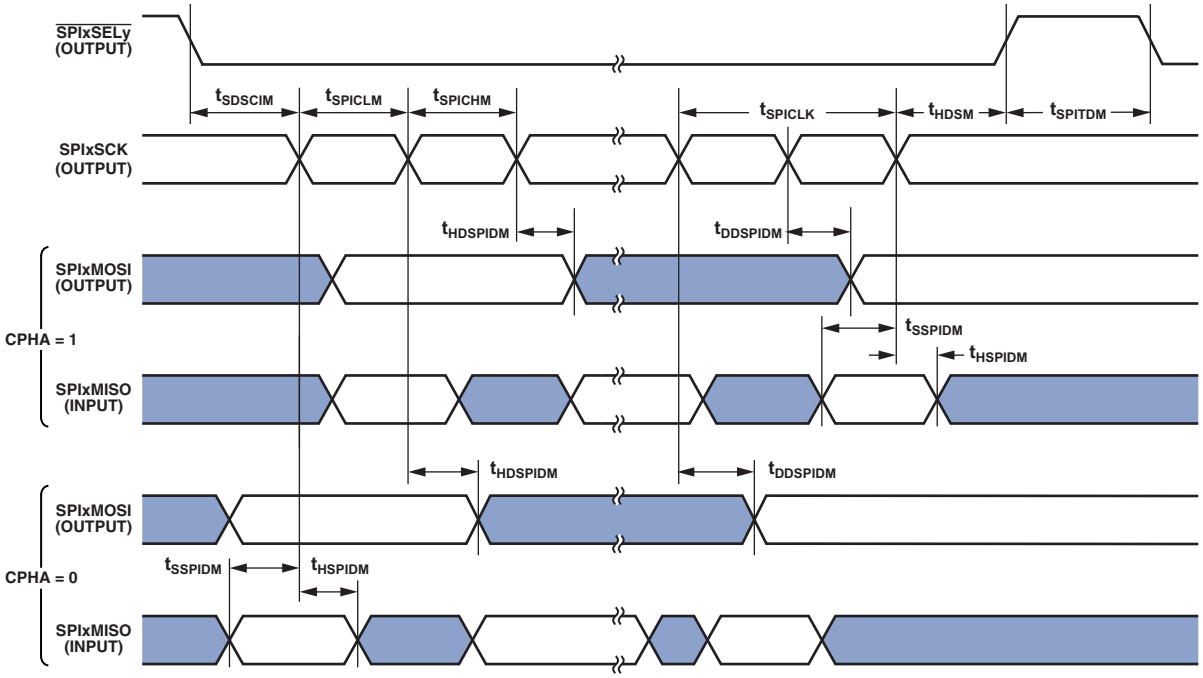


Figure 27. Serial Peripheral Interface (SPI) Ports—Master Timing

General-Purpose Port Timing

Table 37 and Figure 29 describe general-purpose operations.

Table 37. General-Purpose Port Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WFI}	GP Port Pin Input Pulse Width	t_{SCLK} + 1		ns
Switching Characteristic				
t_{GPOD}	GP Port Pin Output Delay from CLKOUT Low		6	ns

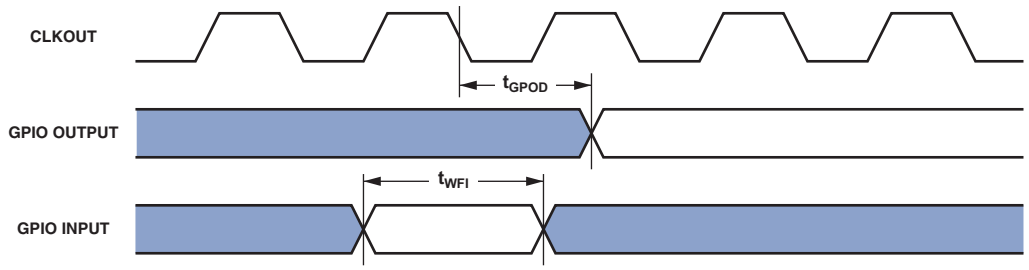


Figure 29. General-Purpose Port Cycle Timing

Timer Clock Timing

Table 38 and Figure 30 describe timer clock timing.

Table 38. Timer Clock Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TODP}	Timer Output Update Delay After PPI_CLK High		12	ns

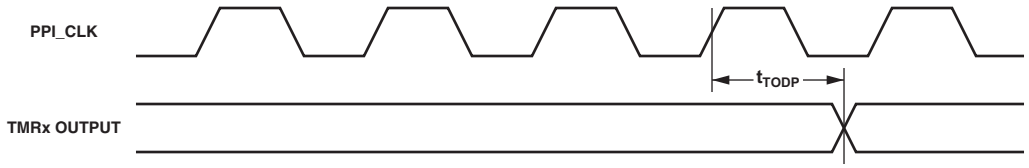


Figure 30. Timer Clock Timing

Timer Cycle Timing

Table 39 and Figure 31 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an absolute maximum input frequency of (f_{SCLK}/2) MHz.

Table 39. Timer Cycle Timing

Parameter		Min	Max	Unit
Timing Characteristics				
t_{WL}	Timer Pulse Width Input Low[1]	1× t_{SCLK}		ns
t_{WH}	Timer Pulse Width Input High[1]	1× t_{SCLK}		ns
t_{TIS}	Timer Input Setup Time Before CLKOUT Low[2]	6.5		ns
t_{TIH}	Timer Input Hold Time After CLKOUT Low[2]	–1		ns
Switching Characteristics				
t_{HTO}	Timer Pulse Width Output	1× t_{SCLK}	(2^{32} – 1) × t_{SCLK}	ns
t_{TOD}	Timer Output Delay After CLKOUT High		6	ns

[1] The minimum pulse widths apply for TMRx signals in width capture and external clock modes.
[2] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize timer flag inputs.

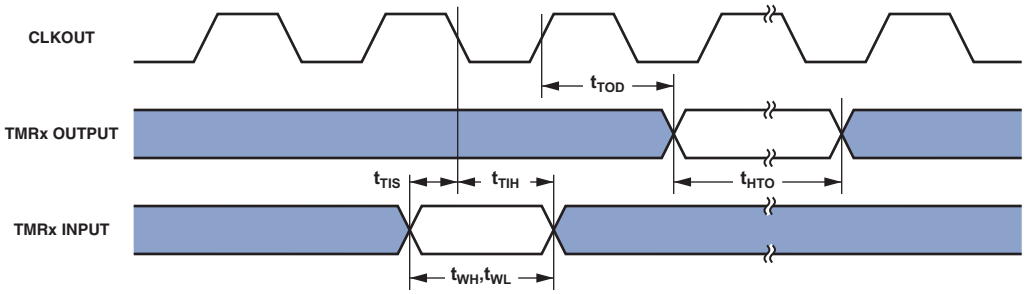


Figure 31. Timer Cycle Timing

OUTPUT DRIVE CURRENTS

Figure 33 through Figure 40 on Page 48 show typical current-voltage characteristics for the output drivers of the ADSP-BF538/ADSP-BF538F processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

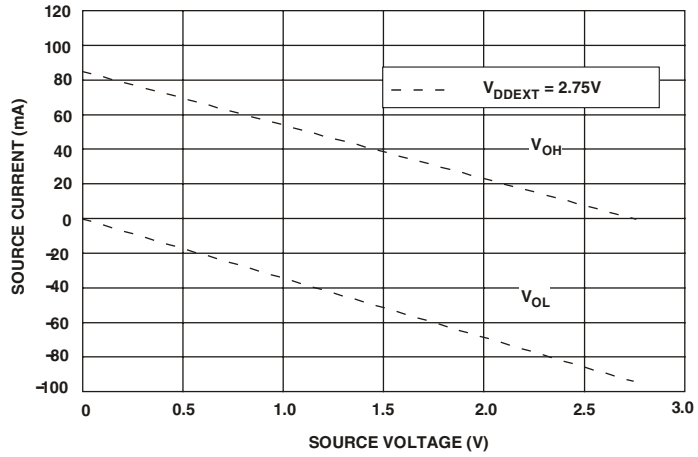


Figure 33. Drive Current A (Low V_{DDEXT})

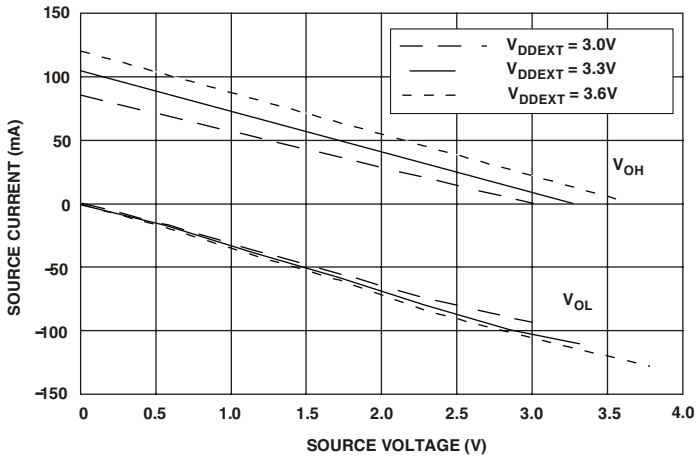


Figure 34. Drive Current A (High V_{DDEXT})

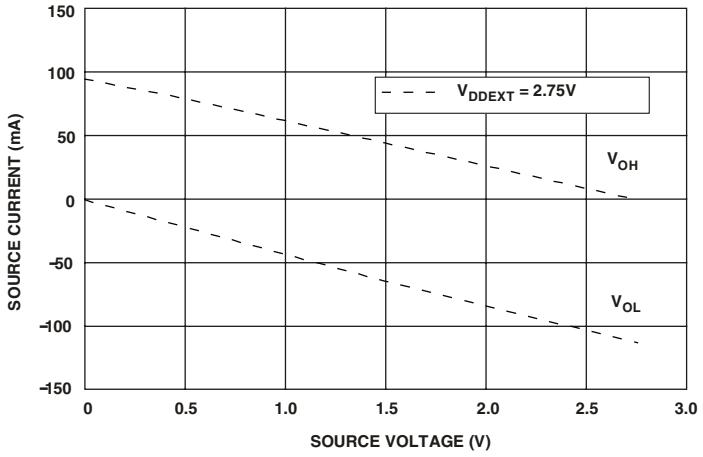


Figure 35. Drive Current B (Low V_{DDEXT})

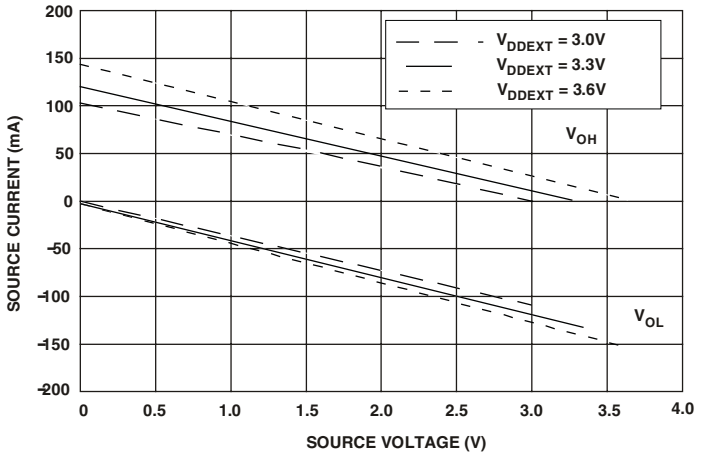


Figure 36. Drive Current B (High V_{DDEXT})

Table 43. 316-Ball CSP_BGA Ball Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	GND	C7	SPI2SEL1	F8	GND	J12	GND	M19	ABE0	T3	GND	W1	TCK
A2	PF10	C8	SPI2SS	F9	GND	J13	GND	M20	ABE1	T7	V_{DDEXT}	W2	GND
A3	PF11	C9	MOSI2	F10	GND	J14	GND	N1	TFS0	T8	V_{DDEXT}	W3	DATA15
A4	PPI_CLK	C10	MISO2	F11	GND	J18	AMS0	N2	DR0PRI	T9	V_{DDEXT}	W4	DATA13
A5	PPI0	C11	SCK2	F12	GND	J19	AMS2	N3	GND	T10	V_{DDEXT}	W5	DATA11
A6	PPI2	C12	V_{DDINT}	F13	GND	J20	SA10	N7	V_{DDEXT}	T11	V_{DDEXT}	W6	DATA9
A7	PF15	C13	SPI1SEL1	F14	GND	K1	RFS1	N8	GND	T12	V_{DDINT}	W7	DATA7
A8	PF13	C14	MISO1	F18	DT3PRI	K2	TMR2	N9	GND	T13	V_{DDINT}	W8	DATA5
A9	V_{DDRTC}	C15	SPI1SS	F19	PC4	K3	V_{DDEXT}	N10	GND	T14	V_{DDINT}	W9	DATA3
A10	RTXO	C16	MOSI1	F20	PC8	K7	GND	N11	GND	T18	RFS3	W10	DATA1
A11	RTXI	C17	SCK1	G1	SCK0	K8	GND	N12	GND	T19	ADDR7	W11	RSCLK2
A12	GND	C18	GND	G2	MOSI0	K9	GND	N13	GND	T20	ADDR8	W12	DR2PRI
A13	CLKIN	C19	PC6	G3	DT0SEC	K10	GND	N14	V_{DDINT}	U1	TRST	W13	DT2PRI
A14	XTAL	C20	SCKE	G7	GND	K11	GND	N18	DT3SEC	U2	TMS	W14	RX2
A15	GND	D1	PF4	G8	GND	K12	GND	N19	ADDR1	U3	GND	W15	TX2
A16	NC	D2	PF5	G9	GND	K13	GND	N20	ADDR2	U7	V_{DDEXT}	W16	ADDR18
A17	GND	D3	DT1SEC	G10	GND	K14	GND	P1	TSCLK0	U8	V_{DDEXT}	W17	ADDR15
A18	GPW	D7	GND	G11	GND	K18	AMS3	P2	RFS0	U9	V_{DDEXT}	W18	ADDR13
A19	VROUT1	D8	GND	G12	GND	K19	AMS1	P3	GND	U10	V_{DDEXT}	W19	GND
A20	GND	D9	GND	G13	GND	K20	AOE	P7	V_{DDEXT}	U11	V_{DDEXT}	W20	ADDR14
B1	PF8	D10	GND	G14	GND	L1	RSCLK1	P8	GND	U12	V_{DDINT}	Y1	GND
B2	GND	D11	GND	G18	BR	L2	TMR1	P9	GND	U13	V_{DDINT}	Y2	TDO
B3	PF9	D12	GND	G19	CLKOUT	L3	GND	P10	GND	U14	V_{DDINT}	Y3	DATA14
B4	PF3	D13	GND	G20	SRAS	L7	GND	P11	GND	U18	RSCLK3	Y4	DATA12
B5	PPI1	D14	GND	H1	DT1PRI	L8	GND	P12	GND	U19	ADDR9	Y5	DATA10
B6	PPI3	D18	GND	H2	TSCLK1	L9	GND	P13	GND	U20	ADDR10	Y6	DATA8
B7	PF14	D19	PC7	H3	DR1SEC	L10	GND	P14	V_{DDINT}	V1	TDI	Y7	DATA6
B8	PF12	D20	SMS	H7	GND	L11	GND	P18	DR3SEC	V2	GND	Y8	DATA4
B9	SCL0	E1	PF1	H8	GND	L12	GND	P19	ADDR3	V3	GND	Y9	DATA2
B10	SDA0	E2	PF2	H9	GND	L13	GND	P20	ADDR4	V4	BMODE1	Y10	DATA0
B11	CANRX	E3	GND	H10	GND	L14	GND	R1	TX0	V5	BMODE0	Y11	RFS2
B12	CANTX	E7	GND	H11	GND	L18	TSCLK3	R2	RSCLK0	V6	GND	Y12	TSCLK2
B13	NMI	E8	GND	H12	GND	L19	ARE	R3	GND	V7	V_{DDEXT}	Y13	TFS2
B14	RESET	E9	GND	H13	GND	L20	AWE	R7	V_{DDEXT}	V8	V_{DDEXT}	Y14	FRESET
B15	V_{DDEXT}	E10	GND	H14	GND	M1	DT0PRI	R8	GND	V9	V_{DDEXT}	Y15	SCL1
B16	GND	E11	GND	H18	FCE	M2	TMR0	R9	GND	V10	V_{DDEXT}	Y16	SDA1
B17	PC9	E12	GND	H19	SCAS	M3	GND	R10	GND	V11	V_{DDEXT}	Y17	ADDR19
B18	GND	E13	GND	H20	SWE	M7	V_{DDEXT}	R11	GND	V12	V_{DDINT}	Y18	ADDR17
B19	GND	E14	GND	J1	TFS1	M8	GND	R12	GND	V13	DR2SEC	Y19	ADDR16
B20	VROUT0	E18	GND	J2	DR1PRI	M9	GND	R13	GND	V14	BG	Y20	GND
C1	PF6	E19	PC5	J3	DR0SEC	M10	GND	R14	V_{DDINT}	V15	BGH		
C2	PF7	E20	ARDY	J7	GND	M11	GND	R18	DR3PRI	V16	DT2SEC		
C3	GND	F1	PF0	J8	GND	M12	GND	R19	ADDR5	V17	GND		
C4	GND	F2	MISO0	J9	GND	M13	GND	R20	ADDR6	V18	GND		
C5	RX1	F3	GND	J10	GND	M14	V_{DDINT}	T1	RX0	V19	ADDR11		
C6	TX1	F7	GND	J11	GND	M18	TFS3	T2	EMU	V20	ADDR12		

Table 44. 316-Ball CSP_BGA Ball Assignment (Alphabetically by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{ABE0}$	M19	DATA8	Y6	GND	D14	GND	K8	GND	V2	RFS0	P2	TX0	R1
$\overline{ABE1}$	M20	DATA9	W6	GND	D18	GND	K9	GND	V3	RFS1	K1	TX1	C6
ADDR1	N19	DATA10	Y5	GND	E3	GND	K10	GND	V6	RFS2	Y11	TX2	W15
ADDR2	N20	DATA11	W5	GND	E7	GND	K11	GND	V17	RFS3	T18	V_{DDEXT}	K3
ADDR3	P19	DATA12	Y4	GND	E8	GND	K12	GND	V18	RSCLK0	R2	V_{DDEXT}	B15
ADDR4	P20	DATA13	W4	GND	E9	GND	K13	GND	W2	RSCLK1	L1	V_{DDEXT}	T8
ADDR5	R19	DATA14	Y3	GND	F8	GND	L13	GND	W19	RSCLK2	W11	V_{DDEXT}	T9
ADDR6	R20	DATA15	W3	GND	F9	GND	L14	GND	Y1	RSCLK3	U18	V_{DDEXT}	T10
ADDR7	T19	DR0PRI	N2	GND	F10	GND	M3	GND	Y20	RTXI	A11	V_{DDEXT}	T11
ADDR8	T20	DR0SEC	J3	GND	F11	GND	M8	$\overline{GPW}$	A18	RTXO	A10	V_{DDEXT}	U7
ADDR9	U19	DR1PRI	J2	GND	F12	GND	M9	MISO0	F2	RX0	T1	V_{DDEXT}	U8
ADDR10	U20	DR1SEC	H3	GND	F13	GND	M10	MISO1	C14	RX1	C5	V_{DDEXT}	U9
ADDR11	V19	DR2PRI	W12	GND	F14	GND	M11	MISO2	C10	RX2	W14	V_{DDEXT}	U10
ADDR12	V20	DR2SEC	V13	GND	G7	GND	M12	MOSI0	G2	SA10	J20	V_{DDEXT}	U11
ADDR13	W18	DR3PRI	R18	GND	G8	GND	M13	MOSI1	C16	$\overline{SCAS}$	H19	V_{DDEXT}	V7
ADDR14	W20	DR3SEC	P18	GND	G9	GND	N3	MOSI2	C9	SCK0	G1	V_{DDEXT}	M7
ADDR15	W17	DT0PRI	M1	GND	E10	GND	K14	NC	A16	SCK1	C17	V_{DDEXT}	N7
ADDR16	Y19	DT0SEC	G3	GND	E11	GND	L3	$\overline{NMI}$	B13	SCK2	C11	V_{DDEXT}	P7
ADDR17	Y18	DT1PRI	H1	GND	E12	GND	L7	PC4	F19	SCKE	C20	V_{DDEXT}	R7
ADDR18	W16	DT1SEC	D3	GND	E13	GND	L8	PC5	E19	SCL0	B9	V_{DDEXT}	T7
ADDR19	Y17	DT2PRI	W13	GND	E14	GND	L9	PC6	C19	SCL1	Y15	V_{DDEXT}	V8
$\overline{AMS0}$	J18	DT2SEC	V16	GND	E18	GND	L10	PC7	D19	SDA0	B10	V_{DDEXT}	V9
$\overline{AMS1}$	K19	DT3PRI	F18	GND	F3	GND	L11	PC8	F20	SDA1	Y16	V_{DDEXT}	V10
$\overline{AMS2}$	J19	DT3SEC	N18	GND	F7	GND	L12	PC9	B17	$\overline{SMS}$	D20	V_{DDEXT}	V11
$\overline{AMS3}$	K18	$\overline{EMU}$	T2	GND	G10	GND	N8	PF0	F1	$\overline{SPI1SEL1}$	C13	V_{DDINT}	C12
$\overline{AOE}$	K20	$\overline{FCE}$	H18	GND	G11	GND	N9	PF1	E1	$\overline{SPI1SS}$	C15	V_{DDINT}	M14
ARDY	E20	$\overline{FRESET}$	Y14	GND	G12	GND	N10	PF2	E2	$\overline{SPI2SEL1}$	C7	V_{DDINT}	N14
$\overline{ARE}$	L19	GND	A1	GND	G13	GND	N11	PF3	B4	$\overline{SPI2SS}$	C8	V_{DDINT}	P14
$\overline{AWE}$	L20	GND	A12	GND	G14	GND	N12	PF4	D1	$\overline{SRAS}$	G20	V_{DDINT}	R14
$\overline{BG}$	V14	GND	A15	GND	H7	GND	N13	PF5	D2	$\overline{SWE}$	H20	V_{DDINT}	T12
$\overline{BGH}$	V15	GND	A17	GND	H8	GND	P3	PF6	C1	TCK	W1	V_{DDINT}	T13
BMODE0	V5	GND	A20	GND	H9	GND	P8	PF7	C2	TDI	V1	V_{DDINT}	T14
BMODE1	V4	GND	B16	GND	H10	GND	P9	PF8	B1	TDO	Y2	V_{DDINT}	U12
$\overline{BR}$	G18	GND	B18	GND	H11	GND	P10	PF9	B3	TFS0	N1	V_{DDINT}	U13
CANRX	B11	GND	B19	GND	H12	GND	P11	PF10	A2	TFS1	J1	V_{DDINT}	U14
CANTX	B12	GND	B2	GND	H13	GND	P12	PF11	A3	TFS2	Y13	V_{DDINT}	V12
CLKIN	A13	GND	C18	GND	H14	GND	P13	PF12	B8	TFS3	M18	V_{DDRTC}	A9
CLKOUT	G19	GND	C3	GND	J7	GND	R3	PF13	A8	TMR0	M2	VROUT0	B20
DATA0	Y10	GND	C4	GND	J8	GND	R8	PF14	B7	TMR1	L2	VROUT1	A19
DATA1	W10	GND	D7	GND	J9	GND	R9	PF15	A7	TMR2	K2	XTAL	A14
DATA2	Y9	GND	D8	GND	J10	GND	R10	PPI_CLK	A4	TMS	U2		
DATA3	W9	GND	D9	GND	J11	GND	R11	PPI0	A5	$\overline{TRST}$	U1		
DATA4	Y8	GND	D10	GND	J12	GND	R12	PPI1	B5	TSCLK0	P1		
DATA5	W8	GND	D11	GND	J13	GND	R13	PPI2	A6	TSCLK1	H2		
DATA6	Y7	GND	D12	GND	J14	GND	T3	PPI3	B6	TSCLK2	Y12		
DATA7	W7	GND	D13	GND	K7	GND	U3	$\overline{RESET}$	B14	TSCLK3	L18		