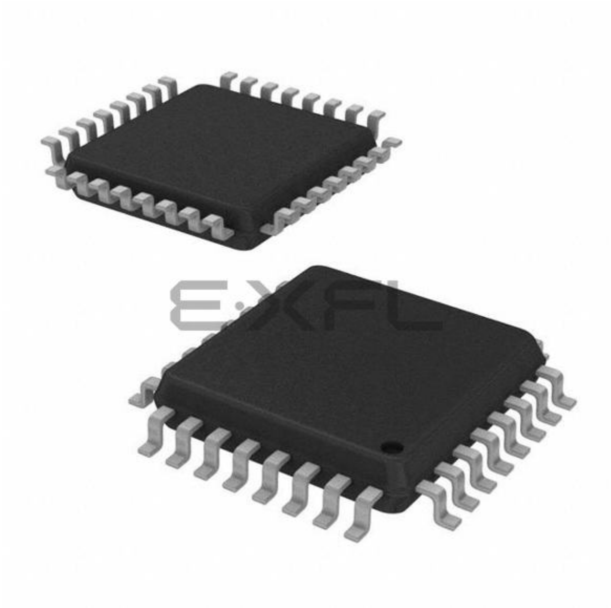


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.25V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f410-gq

1.13. Programmable Counter Array

The Programmable Counter Array (PCA0) provides enhanced timer functionality while requiring less CPU intervention than the standard 8051 counter/timers. The PCA consists of a dedicated 16-bit counter/timer and six 16-bit capture/compare modules. The counter/timer is driven by a programmable timebase that can select between seven sources: system clock, system clock divided by four, system clock divided by twelve, the external oscillator clock source divided by 8, real-time clock source divided by 8, Timer 0 overflow, or an external clock signal on the External Clock Input (ECI) pin.

Each capture/compare module may be configured to operate independently in one of six modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, 8-Bit PWM, or 16-Bit PWM. Additionally, PCA Module 5 may be used as a watchdog timer (WDT), and is enabled in this mode following a system reset. The PCA Capture/Compare Module I/O and the External Clock Input may be routed to Port I/O using the digital crossbar.

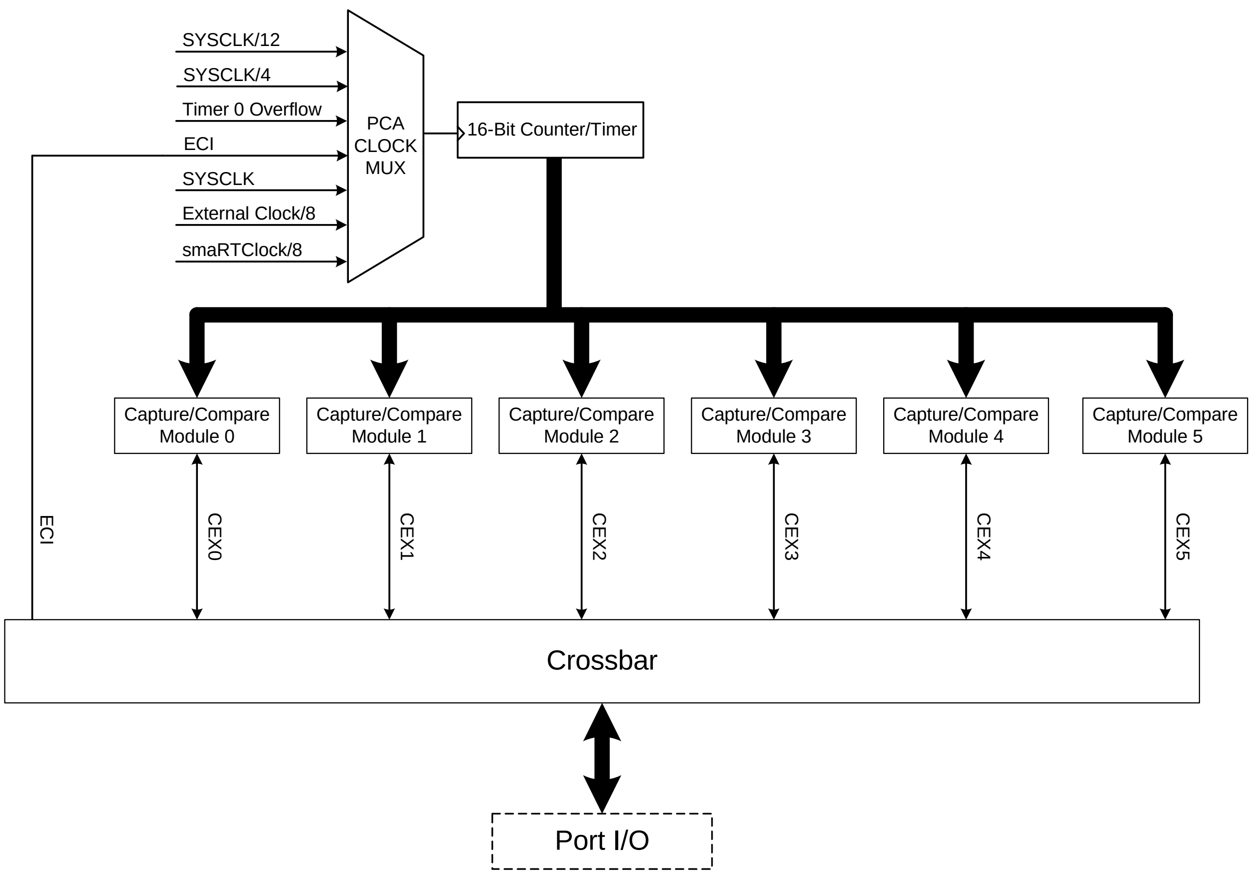


Figure 1.12. PCA Block Diagram

NOTES:

5.4.1. Window Detector In Single-Ended Mode

Figure 5.7 shows two example window comparisons for right-justified data with ADC0LTH:ADC0LTL = 0x0200 (512d) and ADC0GTH:ADC0GTL = 0x0100 (256d). The input voltage can range from ‘0’ to V_{REF} x (4095/4096) with respect to GND, and is represented by a 12-bit unsigned integer value. The repeat count is set to one. In the left example, an AD0WINT interrupt will be generated if the ADC0 conversion word (ADC0H:ADC0L) is within the range defined by ADC0GTH:ADC0GTL and ADC0LTH:ADC0LTL (if 0x0100 < ADC0H:ADC0L < 0x0200). In the right example, and AD0WINT interrupt will be generated if the ADC0 conversion word is outside of the range defined by the ADC0GT and ADC0LT registers (if ADC0H:ADC0L < 0x0100 or ADC0H:ADC0L > 0x0200). Figure 5.8 shows an example using left-justified data with the same comparison values.

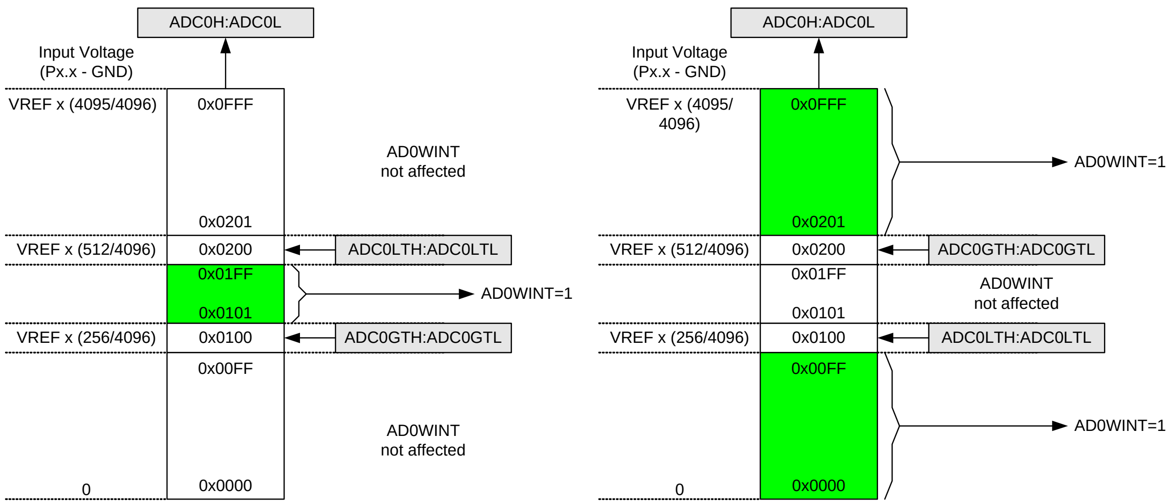


Figure 5.7. ADC Window Compare Example: Right-Justified Single-Ended Data

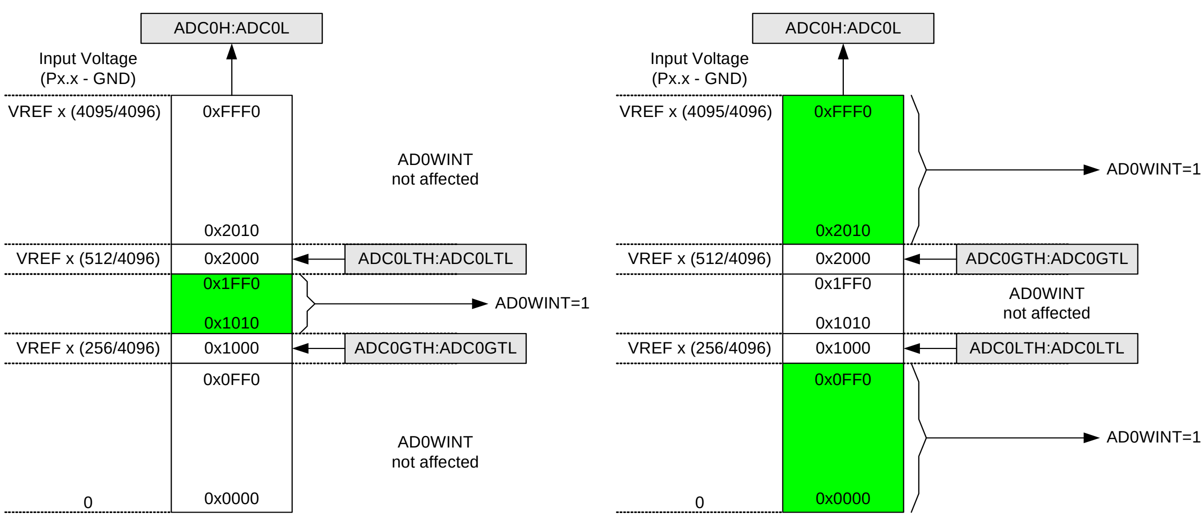


Figure 5.8. ADC Window Compare Example: Left-Justified Single-Ended Data

Table 5.4. ADC0 Electrical Characteristics (V_{DD} = 2.1 V, V_{REF} = 1.5 V)

V_{DD} = 2.1 V, V_{REF} = 1.5 V (REFSL = 0), –40 to +85 °C unless otherwise specified. Typical values are given at 25 ºC.

Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution			12		bits
Integral Nonlinearity		—	—	±1	LSB
Differential Nonlinearity	Guaranteed Monotonic	—	—	±1	LSB
Offset Error		—	±3	±10	LSB
Full Scale Error		—	±3	±10	LSB
Dynamic Performance (10 kHz sine-wave Single-ended input, 0 to 1 dB below Full Scale, 200 ksps)					
Signal-to-Noise Plus Distortion	Regular Mode (BURSTEN = '0') Burst Mode (BURSTEN = '0')	66 60	68 62	— —	dB
Total Harmonic Distortion	Up to the 5th harmonic	—	–75	—	dB
Spurious-Free Dynamic Range		—	–90	—	dB
Conversion Rate					
SAR Conversion Clock	Regular Mode (BURSTEN = '0')	—	—	3	MHz
Conversion Time in SAR Clocks[1]		—	13	—	clocks
Track/Hold Acquisition Time[2]		1	—	—	µs
Throughput Rate		—	—	200	ksps
Analog Inputs					
Input Voltage Range		0	—	V_{REF}	V
Input Capacitance		—	12	—	pF
Temperature Sensor					
Linearity[3,4]		—	±0.2	—	°C
Slope[4]		—	2.95	—	mV/°C
Slope Error[3]		—	±73	—	µV/°C
Offset	(Temp = 0 °C)	—	900	—	mV
Offset Error[3]		—	±17	—	mV
Power Specifications					
Power Supply Current (V_{DD} supplied to ADC0)	Operating Mode, 200 ksps	—	650	1000	µA
Burst Mode (Idle)		—	100	—	µA
Power Supply Rejection		—	1	—	mV/V

Notes:
1. An additional 2 FCLK cycles are required to start and complete a conversion.
2. Additional tracking time may be required depending on the output impedance connected to the ADC input. See Section "5.3.6. Settling Time Requirements" on page 58.
3. Represents one standard deviation from the mean.
4. Includes ADC offset, gain, and linearity variations.

SFR Definition 6.1. IDA0CN: IDA0 Control

R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	Reset Value
IDA0EN	IDA0CM			-	IDA0RJST	IDA0OMD		01110011
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xB9

Bit 7: IDA0EN: IDA0 Enable Bit.
0: IDA0 Disabled.
1: IDA0 Enabled.

Bits 6–4: IDA0CM[2:0]: IDA0 Update Source Select Bits.
000: DAC output updates on Timer 0 overflow.
001: DAC output updates on Timer 1 overflow.
010: DAC output updates on Timer 2 overflow.
011: DAC output updates on Timer 3 overflow.
100: DAC output updates on rising edge of CNVSTR.
101: DAC output updates on falling edge of CNVSTR.
110: DAC output updates on any edge of CNVSTR.
111: DAC output updates on write to IDA0H.

Bit 3: Reserved. Read = 0b, Write = 0b.

Bit 2: IDA0RJST: IDA0 Right Justify Select Bit.
0: IDA0 data in IDA0H:IDA0L is left justified.
1: IDA0 data in IDA0H:IDA0L is right justified.

Bits 1:0: IDA0OMD[1:0]: IDA0 Output Mode Select Bits.
00: 0.25 mA full-scale output current.
01: 0.5 mA full-scale output current.
10: 1.0 mA full-scale output current.
11: 2.0 mA full-scale output current.

SFR Definition 6.2. IDA0H: IDA0 Data High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x97

Bits 7–0: IDA0 Data Word High-Order Bits.
For IDA0RJST = 0:
Bits 7-0 hold the most significant 8-bits of the 12-bit IDA0 Data Word.
For IDA0RJST = 1:
Bits 3-0 hold the most significant 4-bits of the 12-bit IDA0 Data Word. Bits 7-4 are 0000b.

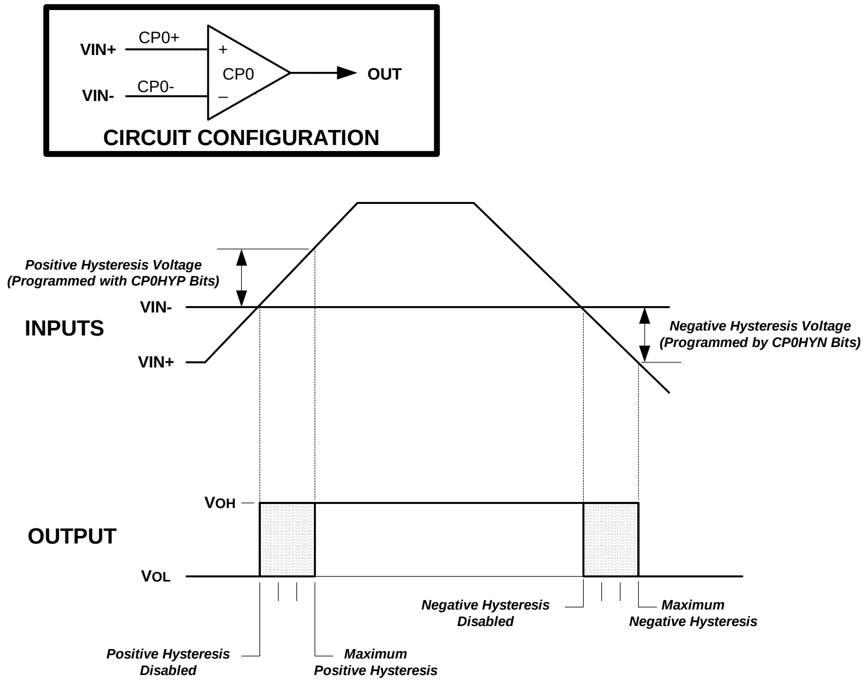


Figure 9.3. Comparator Hysteresis Plot

The Comparator hysteresis is software-programmable via its Comparator Control register CPTnCN (for n = 0 or 1). The user can program both the amount of hysteresis voltage (referred to the input voltage) and the positive and negative-going symmetry of this hysteresis around the threshold voltage.

The Comparator hysteresis is programmed using Bits3-0 in the Comparator Control Register CPTnCN (shown in SFR Definition 9.1 and SFR Definition 9.6). The amount of negative hysteresis voltage is determined by the settings of the CPnHYN bits. As shown in Table 9.1, settings of 20, 10 or 5 mV of negative hysteresis can be programmed, or negative hysteresis can be disabled. In a similar way, the amount of positive hysteresis is determined by setting the CPnHYP bits.

Comparator interrupts can be generated on both rising-edge and falling-edge output transitions. (For Interrupt enable and priority control, see **Section "12. Interrupt Handler" on page 110**). The CPnFIF flag is set to logic 1 upon a Comparator falling-edge detect, and the CPnRIF flag is set to logic 1 upon the Comparator rising-edge detect. Once set, these bits remain set until cleared by software. The output state of the Comparator can be obtained at any time by reading the CPnOUT bit. The Comparator is enabled by setting the CPnEN bit to logic 1, and is disabled by clearing this bit to logic 0.

The output state of the Comparator can be obtained at any time by reading the CPnOUT bit. The Comparator is enabled by setting the CPnEN bit to logic 1, and is disabled by clearing this bit to logic 0. When the Comparator is enabled, the internal oscillator is awakened from SUSPEND mode if the Comparator output is logic 0.

Note that false rising edges and falling edges can be detected when the comparator is first powered-on or if changes are made to the hysteresis or response time control bits. Therefore, it is recommended that the rising-edge and falling-edge flags be explicitly cleared to logic 0 a short time after the comparator is enabled or its mode bits have been changed. This Power Up Time is specified in Table 9.1 on page 92.

SFR Definition 9.1. CPT0CN: Comparator0 Control

R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CP0EN	CP0OUT	CP0RIF	CP0FIF	CP0HYP1	CP0HYP0	CP0HYN1	CP0HYN0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x9B

Bit7: CP0EN: Comparator0 Enable Bit.
0: Comparator0 Disabled.
1: Comparator0 Enabled.

Bit6: CP0OUT: Comparator0 Output State Flag.
0: Voltage on CP0+ < CP0–.
1: Voltage on CP0+ > CP0–.

Bit5: CP0RIF: Comparator0 Rising-Edge Flag.
0: No Comparator0 Rising Edge has occurred since this flag was last cleared.
1: Comparator0 Rising Edge has occurred.

Bit4: CP0FIF: Comparator0 Falling-Edge Flag.
0: No Comparator0 Falling-Edge has occurred since this flag was last cleared.
1: Comparator0 Falling-Edge has occurred.

Bits3–2: CP0HYP1–0: Comparator0 Positive Hysteresis Control Bits.
00: Positive Hysteresis Disabled.
01: Positive Hysteresis = 5 mV.
10: Positive Hysteresis = 10 mV.
11: Positive Hysteresis = 20 mV.

Bits1–0: CP0HYN1–0: Comparator0 Negative Hysteresis Control Bits.
00: Negative Hysteresis Disabled.
01: Negative Hysteresis = 5 mV.
10: Negative Hysteresis = 10 mV.
11: Negative Hysteresis = 20 mV.

10.3.1. Idle Mode

Setting the Idle Mode Select bit (PCON.0) causes the CIP-51 to halt the CPU and enter Idle mode as soon as the instruction that sets the bit completes execution. All internal registers and memory maintain their original data. All analog and digital peripherals can remain active during Idle mode.

Idle mode is terminated when an enabled interrupt is asserted or a reset occurs. The assertion of an enabled interrupt will cause the Idle Mode Selection bit (PCON.0) to be cleared and the CPU to resume operation. The pending interrupt will be serviced and the next instruction to be executed after the return from interrupt (RETI) will be the instruction immediately following the one that set the Idle Mode Select bit. If Idle mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

If enabled, the Watchdog Timer (WDT) will eventually cause an internal watchdog reset and thereby terminate the Idle mode. This feature protects the system from an unintended permanent shutdown in the event of an inadvertent write to the PCON register. If this behavior is not desired, the WDT may be disabled by software prior to entering the Idle mode if the WDT was initially configured to allow this operation. This provides the opportunity for additional power savings, allowing the system to remain in the Idle mode indefinitely, waiting for an external stimulus to wake up the system.

10.3.2. Stop Mode

Setting the Stop Mode Select bit (PCON.1) causes the CIP-51 to enter Stop mode as soon as the instruction that sets the bit completes execution. In Stop mode the internal oscillator, CPU, and all digital peripherals are stopped; the state of the external oscillator circuit is not affected. Each analog peripheral (including the external oscillator circuit) may be shut down individually prior to entering Stop Mode. Stop mode can only be terminated by an internal or external reset. On reset, the CIP-51 performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the Stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to in STOP mode for longer than the MCD timeout period of 100 µs.

10.3.3. Suspend Mode

The C8051F41x devices feature a low-power SUSPEND mode, which stops the internal oscillator until a wakening event occurs. See **Section “19.1.1. Internal Oscillator Suspend Mode” on page 166**.

SFR Definition 10.7. PCON: Power Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	STOP	IDLE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x87

Bits7–2: Reserved.
Bit1: STOP: STOP Mode Select.
Writing a ‘1’ to this bit will place the CIP-51 into STOP mode. This bit will always read ‘0’.
1: CIP-51 forced into power-down mode. (Turns off internal oscillator).
Bit0: IDLE: IDLE Mode Select.
Writing a ‘1’ to this bit will place the CIP-51 into IDLE mode. This bit will always read ‘0’.
1: CIP-51 forced into IDLE mode. (Shuts off clock to CPU, but clock to Timers, Interrupts, and all peripherals remain active.)

Table 11.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	Description	Page
IDA1L	0xF4	Current Mode DAC1 Low Byte	73
IDA1CN	0xB5	Current Mode DAC1 Control	72
IE	0xA8	Interrupt Enable	112
IP	0xB8	Interrupt Priority	113
IT01CF	0xE4	INT0/INT1 Configuration	118
ONESHOT	0xAF	Flash Oneshot Period	143
OSCICL	0xB3	Internal Oscillator Calibration	167
OSCICN	0xB2	Internal Oscillator Control	167
OSCXCN	0xB1	External Oscillator Control	171
P0	0x80	Port 0 Latch	155
P0MASK	0xC7	Port 0 Mask	157
P0MAT	0xD7	Port 0 Match	157
P0MDIN	0xF1	Port 0 Input Mode Configuration	155
P0MDOUT	0xA4	Port 0 Output Mode Configuration	156
P0ODEN	0xB0	Port 0 Overdrive	157
P0SKIP	0xD4	Port 0 Skip	156
P1	0x90	Port 1 Latch	158
P1MASK	0xBF	Port 1 Mask	160
P1MAT	0xCF	Port 1 Match	160
P1MDIN	0xF2	Port 1 Input Mode Configuration	158
P1MDOUT	0xA5	Port 1 Output Mode Configuration	159
P1SKIP	0xD5	Port 1 Skip	159
P2	0xA0	Port 2 Latch	161
P2MDIN	0xF3	Port 2 Input Mode Configuration	161
P2MDOUT	0xA6	Port 2 Output Mode Configuration	162
P2SKIP	0xD6	Port 2 Skip	162
PCA0CN	0xD8	PCA Control	261
PCA0CPH0	0xFC	PCA Capture 0 High	264
PCA0CPH1	0xEA	PCA Capture 1 High	264
PCA0CPH2	0xEC	PCA Capture 2 High	264
PCA0CPH3	0xEE	PCA Capture 3 High	264
PCA0CPH4	0xFE	PCA Capture 4 High	264
PCA0CPH5	0xD3	PCA Capture 5 High	264
PCA0CPL0	0xFB	PCA Capture 0 Low	264
PCA0CPL1	0xE9	PCA Capture 1 Low	264
PCA0CPL2	0xEB	PCA Capture 2 Low	264
PCA0CPL3	0xED	PCA Capture 3 Low	264
PCA0CPL4	0xFD	PCA Capture 4 Low	264

14. Cyclic Redundancy Check Unit (CRC0)

C8051F41x devices include a cyclic redundancy check unit (CRC0) that can perform a CRC using a 16-bit or 32-bit polynomial. CRC0 accepts a stream of 8-bit data written to the CRC0IN register. CRC0 posts the 16-bit or 32-bit result to an internal register. The internal result register may be accessed indirectly using the CRC0PNT bits and CRC0DAT register, as shown in Figure 14.1. CRC0 also has a bit reverse register for quick data manipulation.

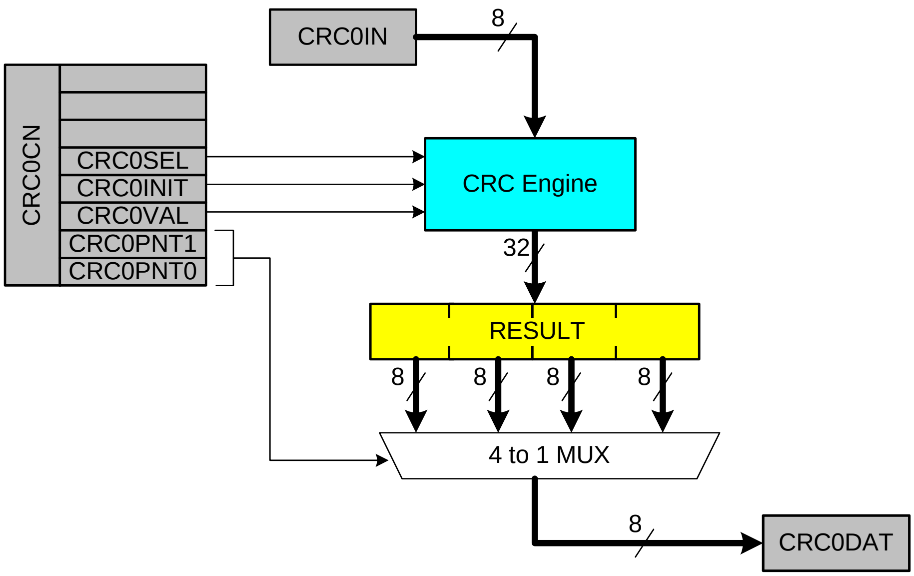


Figure 14.1. CRC0 Block Diagram

14.1. 16-bit CRC Algorithm

The C8051F41x CRC unit calculates the 16-bit CRC MSB-first, using a poly of 0x1021. The following describes the 16-bit CRC algorithm performed by the hardware:

Step 1. XOR the most-significant byte of the current CRC result with the input byte. If this is the first iteration of the CRC unit, the current CRC result will be the set initial value (0x0000 or 0xFFFF).
Step 2a. If the MSB of the CRC result is set, left-shift the CRC result, and then XOR the CRC result with the polynomial (0x1021).
Step 2b. If the MSB of the CRC result is not set, left-shift the CRC result.
Step 3. Repeat at Step 2a for the number of input bits (8).

Table 14.2. Example 32-bit CRC Outputs

Input	Output
0x63	0xF9462090
0xAA, 0xBB, 0xCC	0x41B207B3
0x00, 0x00, 0xAA, 0xBB, 0xCC	0x78D129BC

14.3. Preparing for a CRC Calculation

To prepare CRC0 for a CRC calculation, software should select the desired polynomial and set the initial value of the result. Two polynomials are available: 0x1021 (16-bit) and 0x04C11DB7 (32-bit). The CRC0 result may be initialized to one of two values: 0x00000000 or 0xFFFFFFFF. The following steps can be used to initialize CRC0.

Step 1. Select a polynomial (Set CRC0SEL to ‘0’ for 32-bit or ‘1’ for 16-bit).
Step 2. Select the initial result value (Set CRC0VAL to ‘0’ for 0x00000000 or ‘1’ for 0xFFFFFFFF).
Step 3. Set the result to its initial value (Write ‘1’ to CRC0INIT).

14.4. Performing a CRC Calculation

Once CRC0 is initialized, the input data stream is sequentially written to CRC0IN, one byte at a time. The CRC0 result is automatically updated after each byte is written.

14.5. Accessing the CRC0 Result

The internal CRC0 result is 32-bits (CRC0SEL = 0b) or 16-bits (CRC0SEL = 1b). The CRC0PNT bits select the byte that is targeted by read and write operations on CRC0DAT and increment after each read or write. The calculation result will remain in the internal CRC0 result register until it is set, overwritten, or additional data is written to CRC0IN.

14.6. CRC0 Bit Reverse Feature

CRC0 includes hardware to reverse the bit order of each bit in a byte as shown in Figure 14.2. Each byte of data written to CRC0FLIP is read back bit reversed. For example, if 0xC0 is written to CRC0FLIP, the data read back is 0x03.

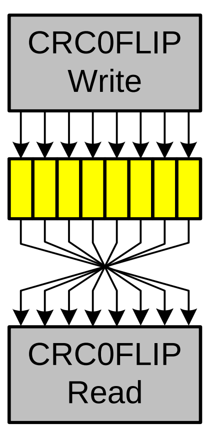


Figure 14.2. Bit Reverse Register

18. Port Input/Output

Digital and analog resources are available through up to 24 I/O pins. Port pins are organized as three byte-wide Ports. Each of the Port pins can be defined as general-purpose I/O (GPIO) or analog input/output; Port pins P0.0 - P2.7 can be assigned to one of the internal digital resources as shown in Figure 18.3. The designer has complete control over which functions are assigned, limited only by the number of physical I/O pins. This resource assignment flexibility is achieved through the use of a Priority Crossbar Decoder. Note that the state of a Port I/O pin can always be read in the corresponding Port latch, regardless of the Crossbar settings.

The Crossbar assigns the selected internal digital resources to the I/O pins based on the peripheral priority order of the Priority Decoder (Figure 18.3 and Figure 18.4). The registers XBR0 and XBR1, defined in SFR Definition 18.1 and SFR Definition 18.2, are used to select internal digital functions.

Port I/Os on P0 are 5 V tolerant over the operating range of V_{IO}. Port I/Os on P1 and P2 should not be driven above V_{IO} or they will sink current. Figure 18.2 shows the Port cell circuit. The Port I/O cells are configured as either push-pull or open-drain in the Port Output Mode registers (PnMDOUT, where n = 0,1,2). Complete Electrical Specifications for Port I/O are given in Table 18.1 on page 163.

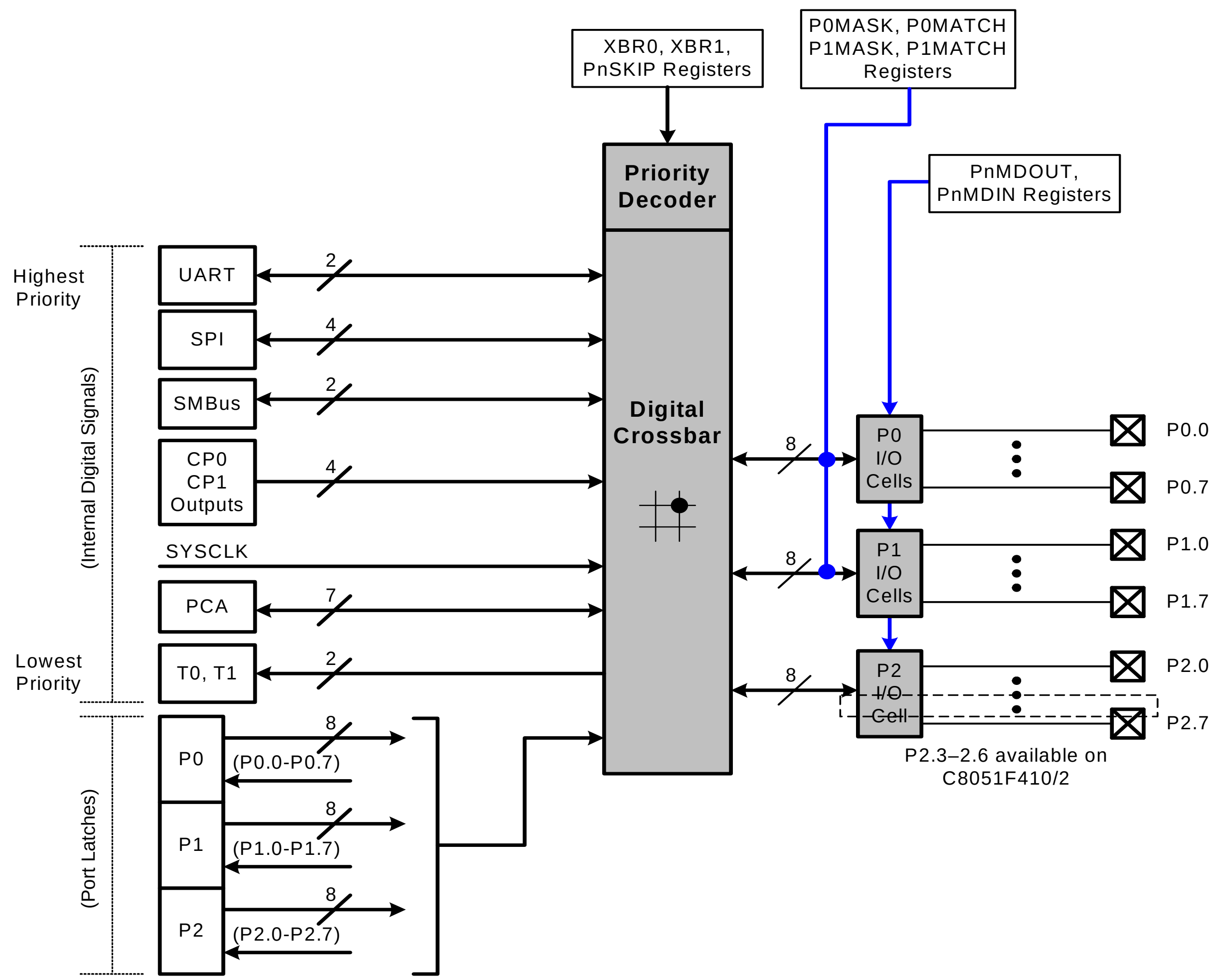


Figure 18.1. Port I/O Functional Block Diagram

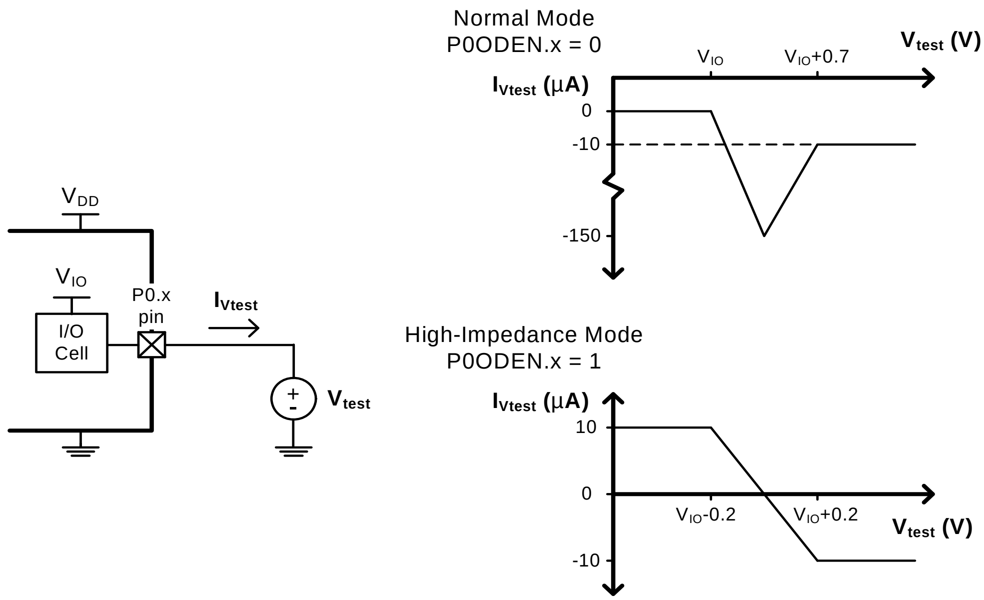


Figure 18.5. Port 0 Input Overdrive Current Range

The output driver characteristics of the I/O pins are defined using the Port Output Mode registers (PnMDOUT). Each Port Output driver can be configured as either open drain or push-pull. This selection is required even for the digital resources selected in the XBRn registers, and is not automatic. The only exception to this is the SMBus (SDA, SCL) pins, which are configured as open-drain regardless of the PnMDOUT settings. When the WEAKPUD bit in XBR1 is '0', a weak pullup is enabled for all Port I/O configured as open-drain. WEAKPUD does not affect the push-pull Port I/O. Furthermore, the weak pullup is turned off on an output that is driving a '0' and for pins configured for analog input mode to avoid unnecessary power dissipation.

Registers XBR0 and XBR1 must be loaded with the appropriate values to select the digital I/O functions required by the design. Setting the XBARE bit in XBR1 to '1' enables the Crossbar. Until the Crossbar is enabled, the external pins remain as standard Port I/O (in input mode), regardless of the XBRn Register settings. For given XBRn Register settings, one can determine the I/O pin-out using the Priority Decode Table.

The Crossbar must be enabled to use Port pins as standard Port I/O in output mode. **Port output drivers are disabled while the Crossbar is disabled.**

SFR Definition 18.14. P1MAT: Port1 Match

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xCF

Bits7–0: P1MAT[7:0]: Port1 Match Value.
These bits control the value that unmasked P0 Port pins are compared against. A Port Match event is generated if (P1 & P1MASK) does not equal (P1MAT & P1MASK).

SFR Definition 18.15. P1MASK: Port1 Mask

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xBF

Bits7–0: P1MASK[7:0]: Port1 Mask Value.
These bits select which Port pins will be compared to the value stored in P1MAT.
0: Corresponding P1.n pin is ignored and cannot cause a Port Match event.
1: Corresponding P1.n pin is compared to the corresponding bit in P1MAT.

SMBus configuration options include:

- Timeout detection (SCL Low Timeout and/or Bus Free Timeout)
- SDA setup and hold time extensions
- Slave event enable/disable
- Clock source selection

These options are selected in the SMB0CF register, as described in **Section “21.4.1. SMBus Configuration Register” on page 195**.

21.4.1. SMBus Configuration Register

The SMBus Configuration register (SMB0CF) is used to enable the SMBus Master and/or Slave modes, select the SMBus clock source, and select the SMBus timing and timeout options. When the ENSMB bit is set, the SMBus is enabled for all master and slave events. Slave events may be disabled by setting the INH bit. With slave events inhibited, the SMBus interface will still monitor the SCL and SDA pins; however, the interface will NACK all received addresses and will not generate any slave interrupts. When the INH bit is set, all slave events will be inhibited following the next START (interrupts will continue for the duration of the current transfer).

Table 21.1. SMBus Clock Source Selection

SMBCS1	SMBCS0	SMBus Clock Source
0	0	Timer 0 Overflow
0	1	Timer 1 Overflow
1	0	Timer 2 High Byte Overflow
1	1	Timer 2 Low Byte Overflow

The SMBCS1-0 bits select the SMBus clock source, which is used only when operating as a master or when the Bus Free Timeout detection is enabled. When operating as a master, overflows from the selected source determine the absolute minimum SCL low and high times as defined in Equation 21.1. Note that the selected clock source may be shared by other peripherals so long as the timer is left running at all times. For example, Timer 1 overflows may generate the SMBus and UART baud rates simultaneously. Timer configuration is covered in **Section “24. Timers” on page 231**.

$$T_{HighMin} = T_{LowMin} = \frac{1}{f_{ClockSourceOverflow}}$$

Equation 21.1. Minimum SCL High and Low Times

The selected clock source should be configured to establish the minimum SCL High and Low times as per Equation 21.1. When the interface is operating as a master (and SCL is not driven or extended by any other devices on the bus), the typical SMBus bit rate is approximated by Equation 21.2.

$$BitRate = \frac{f_{ClockSourceOverflow}}{3}$$

Equation 21.2. Typical SMBus Bit Rate

SFR Definition 22.1. SCON0: Serial Port 0 Control

R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
S0MODE	-	MCE0	REN0	TB80	RB80	TI0	RI0	01000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0x98

Bit7: S0MODE: Serial Port 0 Operation Mode.
This bit selects the UART0 Operation Mode.
0: 8-bit UART with Variable Baud Rate.
1: 9-bit UART with Variable Baud Rate.

Bit6: UNUSED. Read = 1b. Write = don't care.

Bit5: MCE0: Multiprocessor Communication Enable.
The function of this bit is dependent on the Serial Port 0 Operation Mode.
S0MODE = 0: Checks for valid stop bit.
0: Logic level of stop bit is ignored.
1: RI0 will only be activated if stop bit is logic level 1.
S0MODE = 1: Multiprocessor Communications Enable.
0: Logic level of ninth bit is ignored.
1: RI0 is set and an interrupt is generated only when the ninth bit is logic 1.

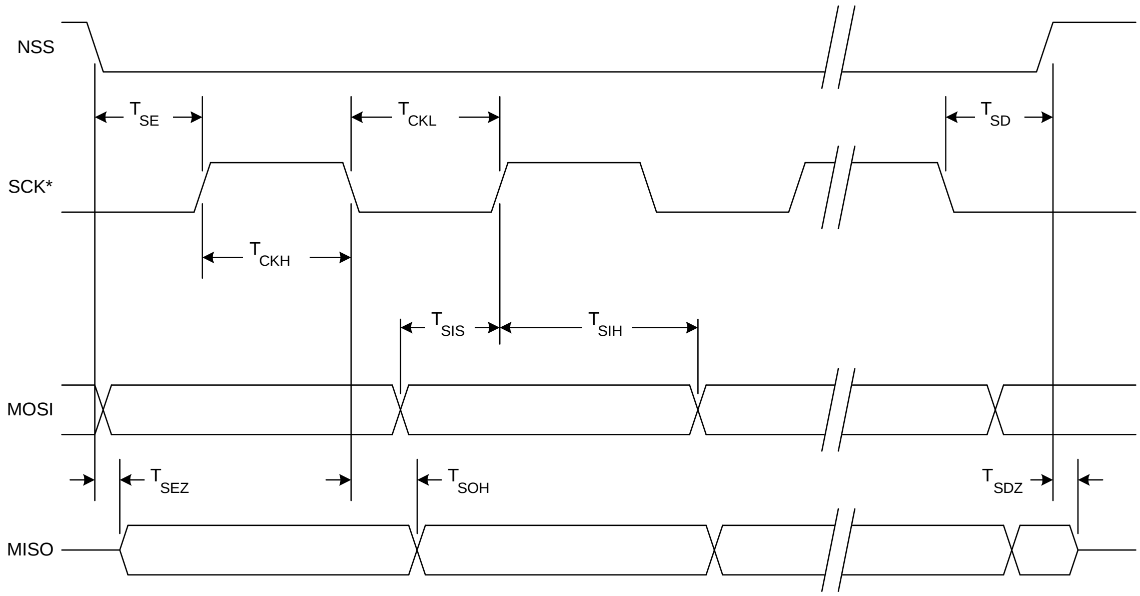
Bit4: REN0: Receive Enable.
This bit enables/disables the UART receiver.
0: UART0 reception disabled.
1: UART0 reception enabled.

Bit3: TB80: Ninth Transmission Bit.
The logic level of this bit will be assigned to the ninth transmission bit in 9-bit UART Mode. It is not used in 8-bit UART Mode. Set or cleared by software as required.

Bit2: RB80: Ninth Receive Bit.
RB80 is assigned the value of the STOP bit in Mode 0; it is assigned the value of the 9th data bit in Mode 1.

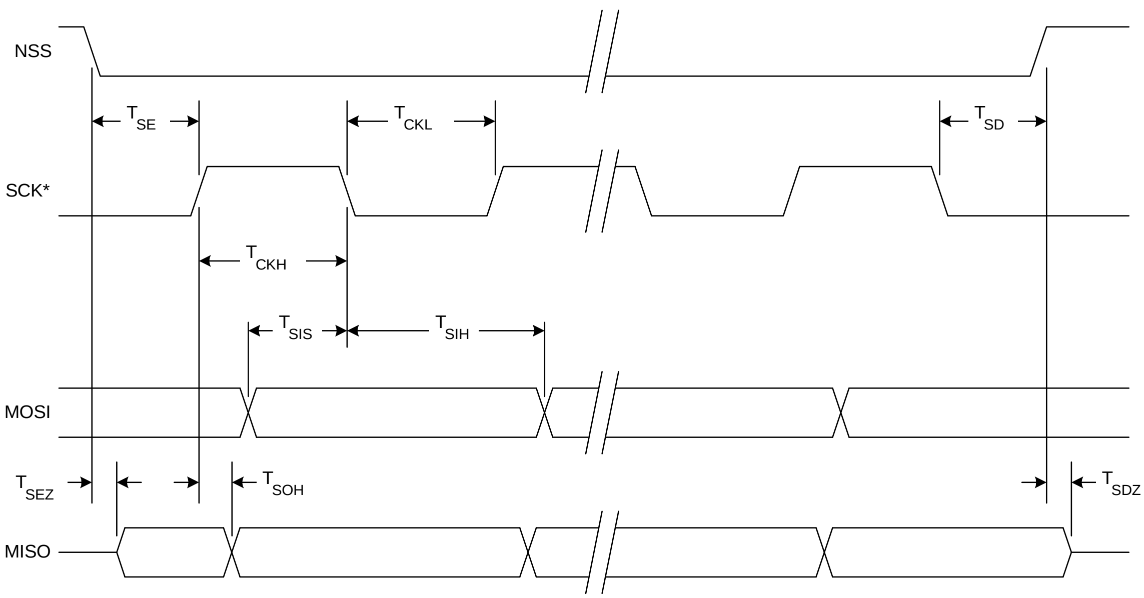
Bit1: TI0: Transmit Interrupt Flag.
Set by hardware when a byte of data has been transmitted by UART0 (after the 8th bit in 8-bit UART Mode, or at the beginning of the STOP bit in 9-bit UART Mode). When the UART0 interrupt is enabled, setting this bit causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.

Bit0: RI0: Receive Interrupt Flag.
Set to '1' by hardware when a byte of data has been received by UART0 (set at the STOP bit sampling time). When the UART0 interrupt is enabled, setting this bit to '1' causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 23.8. SPI Slave Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 23.9. SPI Slave Timing (CKPHA = 1)

25.3.1. Watchdog Timer Operation

While the WDT is enabled:

- PCA counter is forced on.
- Writes to PCA0L and PCA0H are not allowed.
- PCA clock source bits (CPS2-CPS0) are frozen.
- PCA Idle control bit (CIDL) is frozen.
- Module 5 is forced into software timer mode.
- Writes to the Module 5 mode register (PCA0CPM5) are disabled.

While the WDT is enabled, writes to the CR bit will not change the PCA counter state; the counter will run until the WDT is disabled. The PCA counter run control (CR) will read zero if the WDT is enabled but user software has not enabled the PCA counter. If a match occurs between PCA0CPH5 and PCA0H while the WDT is enabled, a reset will be generated. To prevent a WDT reset, the WDT may be updated with a write of any value to PCA0CPH5. Upon a PCA0CPH5 write, PCA0H plus the offset held in PCA0CPL5 is loaded into PCA0CPH5 (See Figure 25.10).

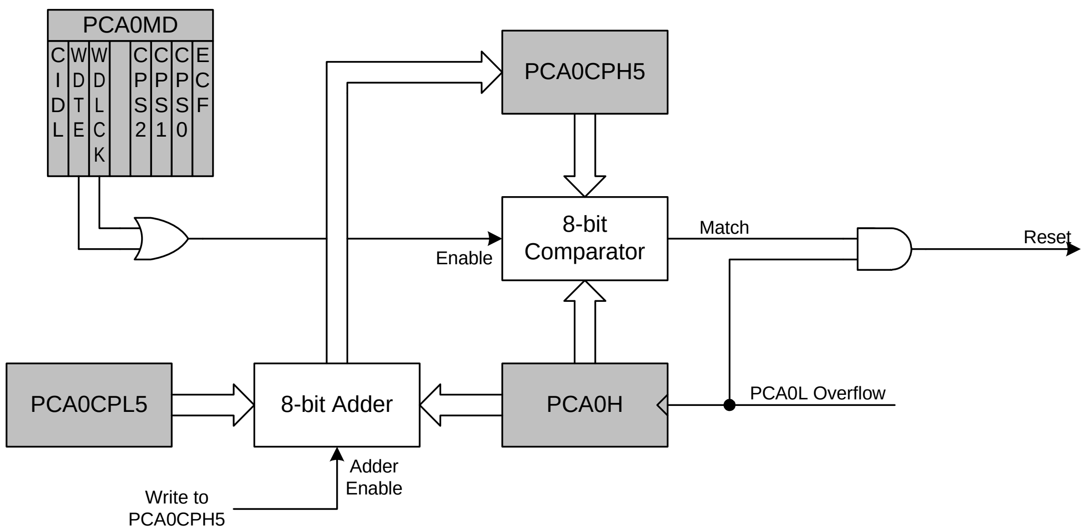


Figure 25.10. PCA Module 5 with Watchdog Timer Enabled

26. C2 Interface

C8051F41x devices include an on-chip Silicon Laboratories 2-Wire (C2) debug interface to allow Flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

26.1. C2 Interface Registers

The following describes the C2 registers necessary to perform Flash programming functions through the C2 interface. All C2 registers are accessed through the C2 interface as described in the C2 Interface Specification.

C2 Register Definition 26.1. C2ADD: C2 Address

								Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits7-0: The C2ADD register is accessed via the C2 interface to select the target Data register for C2 Data Read and Data Write commands.

Address	Description
0x00	Selects the Device ID register for Data Read instructions (DEVICEID)
0x01	Selects the Revision ID register for Data Read instructions (REVID)
0x02	Selects the C2 Flash Programming Control register for Data Read/Write instructions (FPCTL)
0xB4	Selects the C2 Flash Programming Data register for Data Read/Write instructions (FPDAT)

C2 Register Definition 26.2. DEVICEID: C2 Device ID

								Reset Value
								00001011
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

This read-only register returns the 8-bit device ID: 0x0C (C8051F41x).