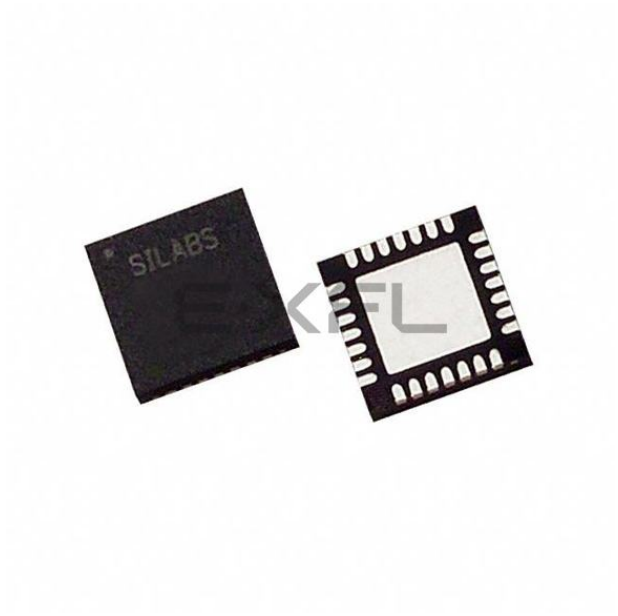

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	20
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.25V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VFQFN Exposed Pad
Supplier Device Package	28-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f413-gmr

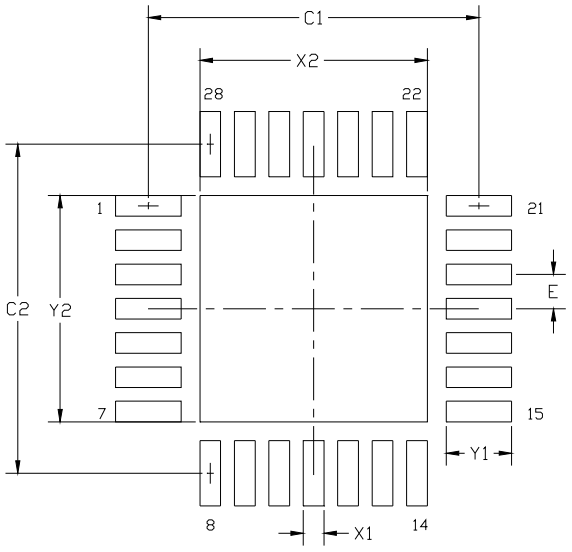


Figure 4.6. QFN-28 Recommended PCB Land Pattern

Table 4.5. QFN-28 PCB Land Pattern Dimensions

Dimension	Min	Max		Dimension	Min	Max
C1	4.80			X2	3.20	3.30
C2	4.80			Y1	0.85	0.95
E	0.50			Y2	3.20	3.30
X1	0.20	0.30				

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60µm minimum, all the way around the pad.

Stencil Design

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
8. A 3x3 array of 0.90mm openings on a 1.1mm pitch should be used for the center pad to assure the proper paste volume (67% Paste Coverage).

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

5.3.5. Output Conversion Code

The registers ADC0H and ADC0L contain the high and low bytes of the output conversion code. When the repeat count is set to 1, conversion codes are represented in 12-bit unsigned integer format and the output conversion code is updated after each conversion. Inputs are measured from '0' to V_{REF} x 4095/4096. Data can be right-justified or left-justified, depending on the setting of the AD0LJST bit (ADC0CN.2). Unused bits in the ADC0H and ADC0L registers are set to '0'. Example codes are shown in Table 5.1 for both right-justified and left-justified data.

Table 5.1. ADC0 Examples of Right- and Left-Justified Samples

Input Voltage	Right-Justified ADC0H:ADC0L (AD0LJST = 0)	Left-Justified ADC0H:ADC0L (AD0LJST = 1)
V_{REF} x 4095/4096	0x0FFF	0xFFF0
V_{REF} x 2048/4096	0x0800	0x8000
V_{REF} x 2047/4096	0x07FF	0x7FF0
0	0x0000	0x0000

When the ADC0 Repeat Count is greater than 1, the output conversion code represents the accumulated result of the conversions performed and is updated after the last conversion in the series is finished. Sets of 4, 8, or 16 consecutive samples can be accumulated and represented in unsigned integer format. The repeat count can be selected using the AD0RPT bits in the ADC0CF register. The value must be right-justified (AD0LJST = "0"), and unused bits in the ADC0H and ADC0L registers are set to '0'. The example in Table 5.2 shows the right-justified result for various input voltages and repeat counts. Notice that accumulating 2^n samples is equivalent to left-shifting by *n* bit positions when all samples returned from the ADC have the same value.

Table 5.2. ADC0 Repeat Count Examples at Various Input Voltages

Input Voltage	Repeat Count = 4	Repeat Count = 8	Repeat Count = 16
V_{REF} x 4095/4096	0x3FFC	0x7FF8	0xFFF0
V_{REF} x 2048/4096	0x2000	0x4000	0x8000
V_{REF} x 2047/4096	0x1FFC	0x3FF8	0x7FF0
0	0x0000	0x0000	0x0000

SFR Definition 5.1. ADC0MX: ADC0 Channel Select

R	R	R	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	AD0MX					00011111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xBB

Bits7–5: UNUSED. Read = 000b; Write = don't care.
Bits4–0: AD0MX4–0: AMUX0 Positive Input Selection

AD0MX4–0	ADC0 Input Channel
00000	P0.0
00001	P0.1
00010	P0.2
00011	P0.3
00100	P0.4
00101	P0.5
00110	P0.6
00111	P0.7
01000	P1.0
01001	P1.1
01010	P1.2
01011	P1.3
01100	P1.4
01101	P1.5
01110	P1.6
01111	P1.7
10000	P2.0
10001	P2.1
10010	P2.2
10011	P2.3*
10100	P2.4*
10101	P2.5*
10110	P2.6*
10111	P2.7
11000	Temp Sensor
11001	V_{DD}
11010 - 11111	GND

***Note:** Only applies to C8051F410/2; selection RESERVED on C8051F411/3 devices.

Important Note About the V_{REF} Pin: Port pin P1.2 is used as the external V_{REF} input and as an output for the internal V_{REF}. When using either an external voltage reference or the internal reference circuitry, P1.2 should be configured as an analog pin, and skipped by the Digital Crossbar. To configure P1.2 as an analog pin, clear Bit 2 in register P1MDIN to '0' and set Bit 2 in register P1 to '1'. To configure the Crossbar to skip P1.2, set Bit 2 in register P1SKIP to '1'. Refer to **Section "18. Port Input/Output" on page 147** for complete Port I/O configuration details. The TEMPE bit in register REF0CN enables/disables the temperature sensor. While disabled, the temperature sensor defaults to a high impedance state and any ADC0 measurements performed on the sensor result in meaningless data.

SFR Definition 7.1. REF0CN: Reference Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
IDAMRG	GF	ZTCEN	REFLV	REFSL	TEMPE	BIASE	REFBE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xD1

Bit7: IDAMRG: IDAC Output Merge Select.
0: IDA1 Output is P0.1.
1: IDA1 Output is P0.0 (Merged with IDA0 Output).

Bit6: GF. General Purpose Flag.
This bit is a general purpose flag for use under software control.

Bit5: ZTCEN: Zero-TempCo Bias Enable Bit.
0: ZeroTC Bias Generator automatically enabled when needed.
1: ZeroTC Bias Generator forced on.

Bit4: REFLV: Voltage Reference Output Level Select.
This bit selects the output voltage level for the internal voltage reference.
0: Internal voltage reference set to 1.5 V.
1: Internal voltage reference set to 2.2 V.

Bit3: REFSL: Voltage Reference Select.
This bit selects the source for the internal voltage reference.
0: V_{REF} pin used as voltage reference.
1: V_{DD} used as voltage reference.

Bit2: TEMPE: Temperature Sensor Enable Bit.
0: Internal Temperature Sensor off.
1: Internal Temperature Sensor on.

Bit1: BIASE: Internal Analog Bias Generator Enable Bit.
0: Internal Analog Bias Generator automatically enabled when needed.
1: Internal Analog Bias Generator on.

Bit0: REFBE: Internal Reference Buffer Enable Bit.
0: Internal Reference Buffer disabled.
1: Internal Reference Buffer enabled. Internal voltage reference driven on the V_{REF} pin.

9. Comparators

C8051F41x devices include two on-chip programmable voltage comparators: Comparator0 is shown in Figure 9.1; Comparator1 is shown in Figure 9.2. The two comparators operate identically, but only Comparator0 can be used as a reset source.

The Comparator offers programmable response time and hysteresis, an analog input multiplexer, and two outputs that are optionally available at the Port pins: a synchronous “latched” output (CP0, CP1), or an asynchronous “raw” output (CP0A, CP1A). The asynchronous CP0A signal is available even when the system clock is not active. This allows the Comparator to operate and generate an output with the device in STOP or SUSPEND mode. When assigned to a Port pin, the Comparator output may be configured as open drain or push-pull (see **Section “18.2. Port I/O Initialization” on page 151**). Comparator0 may also be used as a reset source (see **Section “15.5. Comparator0 Reset” on page 130**).

The Comparator0 inputs are selected in the CPT0MX register (SFR Definition 9.2). The CMX0P3-CMX0P0 bits select the Comparator0 positive input; the CMX0N3-CMX0N0 bits select the Comparator0 negative input. The Comparator1 inputs are selected in the CPT1MX register (SFR Definition 9.4). The CMX1P3-CMX1P0 bits select the Comparator1 positive input; the CMX1N3-CMX1N0 bits select the Comparator1 negative input.

Important Note About Comparator Inputs: The Port pins selected as Comparator inputs should be configured as analog inputs in their associated Port configuration register (with a ‘1’ written to the corresponding Port Latch register), and configured to be skipped by the Crossbar (for details on Port configuration, see **Section “18.3. General Purpose Port I/O” on page 154**)

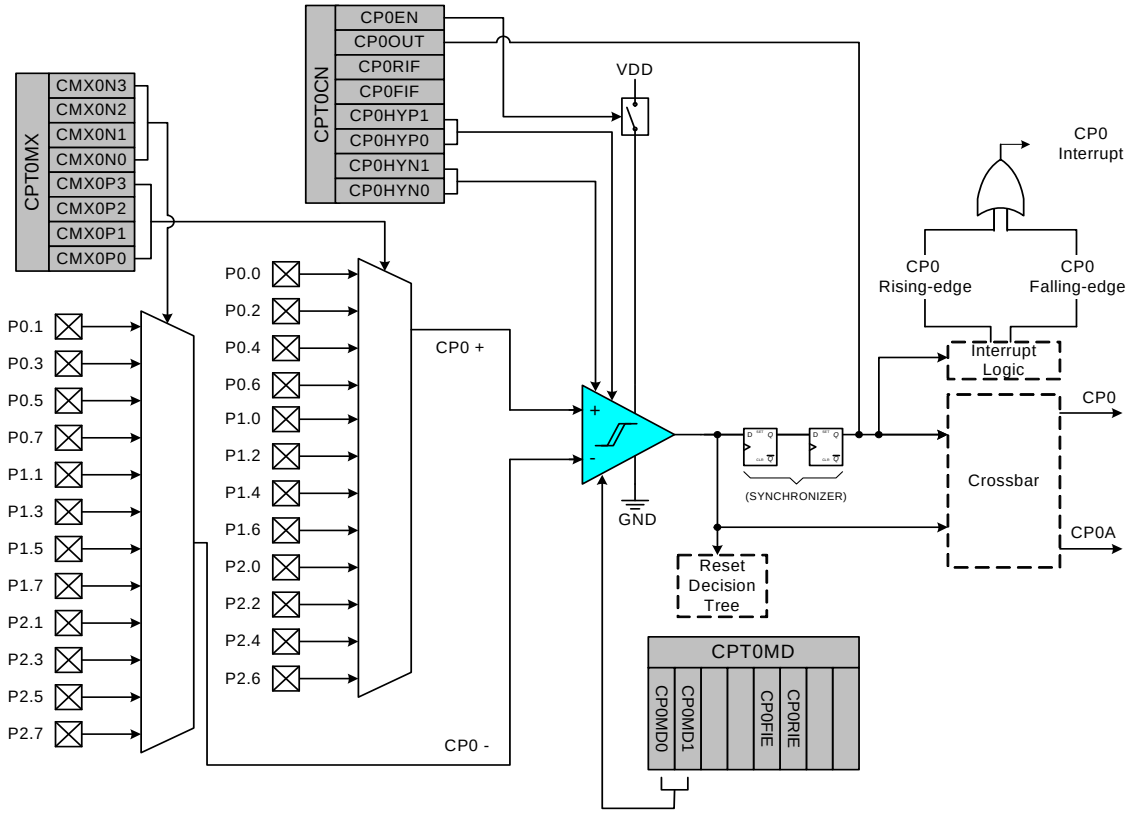


Figure 9.1. Comparator0 Functional Block Diagram

16. Flash Memory

On-chip, re-programmable Flash memory is included for program code and non-volatile data storage. The Flash memory can be programmed in-system through the C2 interface or by software using the MOVX write instruction. Once cleared to logic 0, a Flash bit must be erased to set it back to logic 1. Flash bytes would typically be erased (set to 0xFF) before being reprogrammed. The write and erase operations are automatically timed by hardware for proper execution; data polling to determine the end of the write/erase operations is not required. Code execution is stalled during Flash write/erase operations. Refer to Table 16.2 for complete Flash memory electrical characteristics.

16.1. Programming The Flash Memory

The simplest means of programming the Flash memory is through the C2 interface using programming tools provided by Silicon Laboratories or a third party vendor. This is the only means for programming a non-initialized device. For details on the C2 commands to program Flash memory, see **Section "26. C2 Interface" on page 265**. For detailed guidelines on writing or erasing Flash from firmware, please see **Section "16.4. Flash Write and Erase Guidelines" on page 139**.

To ensure the integrity of the Flash contents, the on-chip VDD Monitor must be enabled to the higher setting (VDMLVL = '1') in any system that includes code that writes and/or erases Flash memory from software. Furthermore, there should be no delay between enabling the V_{DD} Monitor and enabling the V_{DD} Monitor as a reset source. Any attempt to write or erase Flash memory while the V_{DD} Monitor disabled will cause a Flash Error device reset.

16.1.1. Flash Lock and Key Functions

Flash writes and erases by user software are protected with a lock and key function. The Flash Lock and Key Register (FLKEY) must be written with the correct key codes, in sequence, before Flash operations may be performed. The key codes are: 0xA5, 0xF1. The timing does not matter, but the codes must be written in order. If the key codes are written out of order, or the wrong codes are written, Flash writes and erases will be disabled until the next system reset. Flash writes and erases will also be disabled if a Flash write or erase is attempted before the key codes have been written properly. The Flash lock resets after each write or erase; the key codes must be written again before a following Flash operation can be performed. The FLKEY register is detailed in SFR Definition 16.2.

16.1.2. Flash Erase Procedure

The Flash memory can be programmed by software using the MOVX write instruction with the address and data byte to be programmed provided as normal operands. Before writing to Flash memory using MOVX, Flash write operations must be enabled by: (1) setting the PSWE Program Store Write Enable bit (PSCTL.0) to logic 1 (this directs the MOVX writes to target Flash memory); and (2) Writing the Flash key codes in sequence to the Flash Lock register (FLKEY). The PSWE bit remains set until cleared by software.

A write to Flash memory can clear bits to logic 0 but cannot set them; only an erase operation can set bits to logic 1 in Flash. **A byte location to be programmed should be erased before a new value is written.** The Flash memory is organized in 512-byte pages. The erase operation applies to an entire page (setting all bytes in the page to 0xFF). To erase an entire 512-byte page, perform the following steps:

Step 1. Disable interrupts (recommended).
Step 2. Write the first key code to FLKEY: 0xA5.
Step 3. Write the second key code to FLKEY: 0xF1.
Step 4. Set the PSEE bit (register PSCTL).
Step 5. Set the PSWE bit (register PSCTL).
Step 6. Using the MOVX instruction, write a data byte to any location within the 512-byte page to be erased.
Step 7. Clear the PSWE and PSEE bits.
Step 8. Re-enable interrupts.

NOTES:

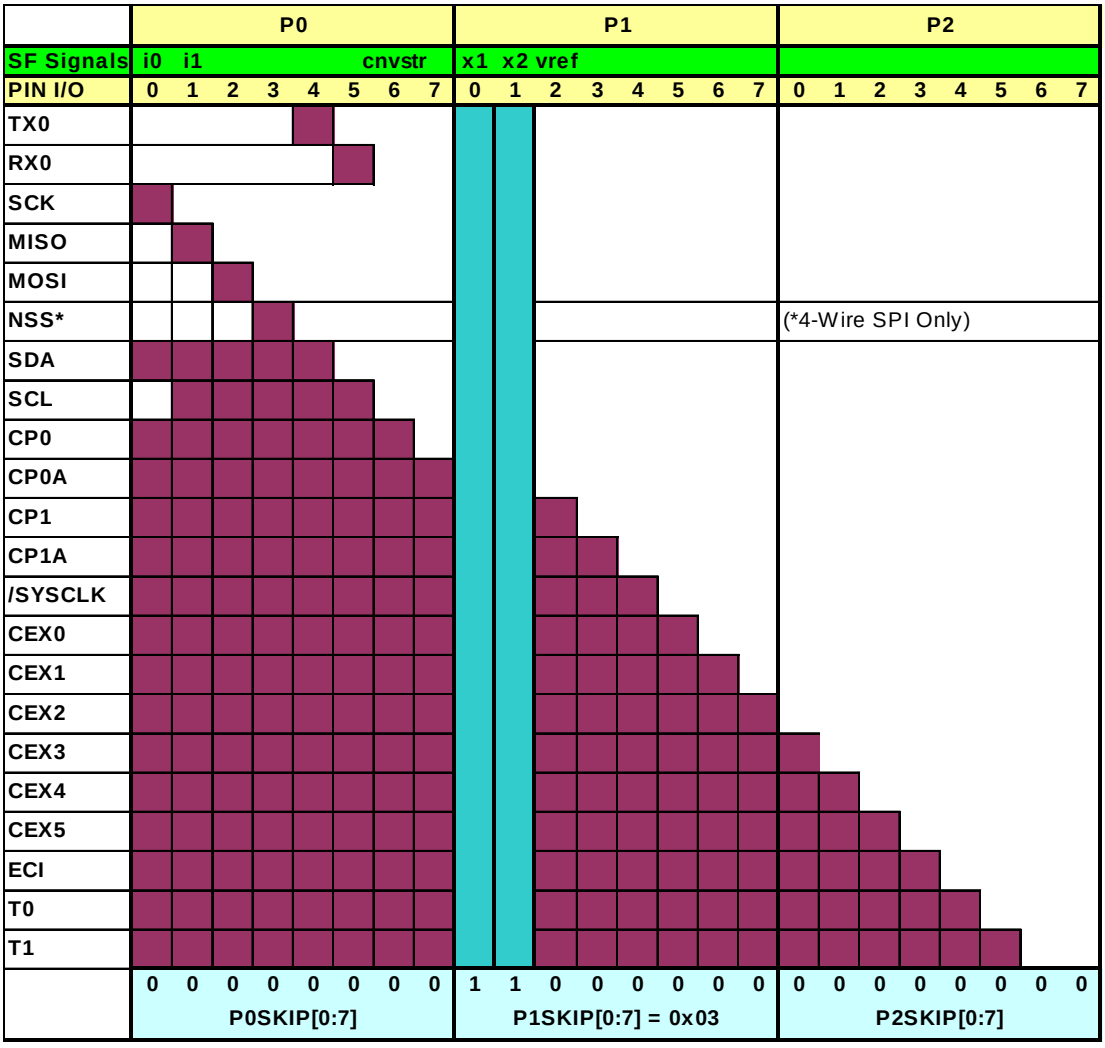


Figure 18.4. Crossbar Priority Decoder with Crystal Pins Skipped

Registers XBR0 and XBR1 are used to assign the digital I/O resources to the physical I/O Port pins. Note that when the SMBus is selected, the Crossbar assigns both pins associated with the SMBus (SDA and SCL); when the UART is selected, the Crossbar assigns both pins associated with the UART (TX and RX). UART0 pin assignments are fixed for bootloading purposes: UART TX0 is always assigned to P0.4; UART RX0 is always assigned to P0.5. Standard Port I/Os appear contiguously starting at P0.0 after prioritized functions and skipped pins are assigned.

Important Note: The SPI can be operated in either 3-wire or 4-wire modes, depending on the state of the NSSMD1-NSSMD0 bits in register SPI0CN. According to the SPI mode, the NSS signal may or may not be routed to a Port pin.

SFR Definition 18.5. P0MDOUT: Port0 Output Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA4

Bits7–0: Output Configuration Bits for P0.7–P0.0 (respectively): ignored if corresponding bit in register P0MDIN is logic 0.
0: Corresponding P0.n Output is open-drain.
1: Corresponding P0.n Output is push-pull.

(Note: When SDA and SCL appear on any of the Port I/O, each are open-drain regardless of the value of P0MDOUT).

SFR Definition 18.6. P0SKIP: Port0 Skip

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD4

Bits7–0: P0SKIP[7:0]: Port0 Crossbar Skip Enable Bits.
These bits select Port pins to be skipped by the Crossbar Decoder. Port pins used as analog inputs (for ADC or Comparator) or used as special functions (V_{REF} input, external oscillator circuit, CNVSTR input) should be skipped by the Crossbar.
0: Corresponding P0.n pin is not skipped by the Crossbar.
1: Corresponding P0.n pin is skipped by the Crossbar.

SFR Definition 18.10. P1: Port1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0x90

Bits7–0: P1.[7:0]
Write - Output appears on I/O pins per Crossbar Registers.
0: Logic Low Output.
1: Logic High Output (high impedance if corresponding P1MDOUT.n bit = 0).
Read - Always reads '0' if selected as analog input in register P1MDIN. Directly reads Port pin when configured as digital input.
0: P1.n pin is logic low.
1: P1.n pin is logic high.

SFR Definition 18.11. P1MDIN: Port1 Input Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xF2

Bits7–0: Analog Input Configuration Bits for P1.7–P1.0 (respectively).
Port pins configured as analog inputs have their weak pullup, digital driver, and digital receiver disabled.
0: Corresponding P1.n pin is configured as an analog input. **In order for the P1.n pin to be in analog input mode, there MUST be a '1' in the Port Latch register corresponding to that pin.**
1: Corresponding P1.n pin is not configured as an analog input.

NOTES:

ning of each series of consecutive reads. Software must check if the smaRTClock Interface is busy prior to reading RTC0DAT. Autoread is enabled by setting AUTORD (RTC0ADR.6) to logic 1.

20.1.4. RTC0ADR Autoincrement Feature

For ease of reading and writing the 48-bit CAPTURE and ALARM values, RTC0ADR automatically increments after each read or write to a CAPTUREn or ALARMn register. This speeds up the process of setting an alarm or reading the current smaRTClock timer value.

Table 20.1. smaRTClock Internal Registers

smaRTClock Address	smaRTClock Register	Register Name	Description
0x00 - 0x05	CAPTUREn	smaRTClock Capture Registers	Six Registers used for setting the 47-bit smaRTClock timer or reading its current value. The LSB of CAPTURE0 is not used.
0x06	RTC0CN	smaRTClock Control Register	Controls the operation of the smaRTClock State Machine.
0x07	RTC0XCN	smaRTClock Oscillator Control Register	Controls the operation of the smaRTClock Oscillator.
0x08–0x0D	ALARMn	smaRTClock Alarm Registers	Six registers used to set or read the 47-bit smaRTClock alarm value. The LSB of ALARM0 is not used.
0x0E	RAMADDR	smaRTClock Backup RAM Indirect Address Register	Used as an index to the 64 byte smaRTClock backup RAM.
0x0F	RAMDATA	smaRTClock Backup RAM Indirect Data Register	Used to read or write the byte pointed to by RAMADDR.

```
   ; Enable the smaRTClock
   mov RTC0ADR, #06h ; address the RTC0CN register
   mov RTC0DAT, #080h ; enable the smaRTClock
L0:mov A, RTC0ADR   ; poll on the BUSY bit
   jb ACC.7, L0

   ; Write to the smaRTClock RAM
   mov RTC0ADR, #0Eh; address the RAMADDR register
   mov RTC0DAT, #20h; write the address of 0x20 to RAMADDR
L1:mov A, RTC0ADR     ; poll on the BUSY bit
   jb ACC.7, L1

   mov RTC0ADR, #0Fh; address the RAMDATA register
   mov RTC0DAT, #0A5h; write 0xA5 to RAM address 0x20
L2: mov A, RTC0ADR     ; poll on the BUSY bit
   jb ACC.7, L2


   ; Read from the smaRTClock RAM
   mov RTC0ADR, #0Eh; address the RAMADDR register
   mov RTC0DAT, #20h; write the address of 0x20 to RAMADDR
L3:mov A, RTC0ADR   ; poll on the BUSY bit
   jb ACC.7, L3

   mov RTC0ADR, #0Fh   ; address the RAMDATA register
   orl RTC0ADR, #80h   ; initiate a read of the RAMDATA register
L4: mov A, RTC0ADR   ; poll on the BUSY bit
   jb ACC.7, L4
   movR0, #80h
   mov@R0, RTC0DAT    ; read the value of RAM address 0x20 into
             ; the 128-byte internal RAM
```

To reduce the number of instructions necessary to read and write sections of the 64-byte RAM, the RAMADDR register automatically increments after each write or read. The following C example initializes the entire 64-byte RAM to 0xA5 and copies this value from the RAM to an array using the auto-increment feature:

```
// in 'C':
unsigned char RAM_data[64] = 0x00;
unsigned char addr;

// Unlock smaRTClock, enable smaRTClock

// Write to the entire smaRTClock RAM
RTC0ADR = 0x0E;// address the RAMADDR register
RTC0DAT = 0x00;// write the address of 0x00 to RAMADDR
while ((RTC0ADR & 0x80) == 0x80);   // poll on the BUSY bit
RTC0ADR = 0x0F;// address the RAMDATA register
for (addr = 0; addr < 64; addr++)
{
   RTC0DAT = 0xA5; // write 0xA5 to every RAM address
   while ((RTC0ADR & 0x80) == 0x80);// poll on the BUSY bit
}

// Read from the entire smaRTClock RAM
RTC0ADR = 0x0E;// address the RAMADDR register
```

SFR Definition 22.2. SBUF0: Serial (UART0) Port Data Buffer

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x99

Bits7–0: SBUF0[7:0]: Serial Data Buffer Bits 7-0 (MSB-LSB)
This SFR accesses two registers; a transmit shift register and a receive latch register. When data is written to SBUF0, it goes to the transmit shift register and is held for serial transmission. Writing a byte to SBUF0 initiates the transmission. A read of SBUF0 returns the contents of the receive latch.

SFR Definition 24.2. TMOD: Timer Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x89

Bit7: GATE1: Timer 1 Gate Control.
0: Timer 1 enabled when TR1 = 1 irrespective of /INT1 logic level.
1: Timer 1 enabled only when TR1 = 1 AND /INT1 is active as defined by bit IN1PL in register IT01CF (see SFR Definition 12.7. “IT01CF: INT0/INT1 Configuration” on page 118).

Bit6: C/T1: Counter/Timer 1 Select.
0: Timer Function: Timer 1 incremented by clock defined by T1M bit (CKCON.4).
1: Counter Function: Timer 1 incremented by high-to-low transitions on external input pin (T1).

Bits5–4: T1M1–T1M0: Timer 1 Mode Select.
These bits select the Timer 1 operation mode.

T1M1	T1M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Timer 1 inactive

Bit3: GATE0: Timer 0 Gate Control.
0: Timer 0 enabled when TR0 = 1 irrespective of /INT0 logic level.
1: Timer 0 enabled only when TR0 = 1 AND /INT0 is active as defined by bit IN0PL in register IT01CF (see SFR Definition 12.7. “IT01CF: INT0/INT1 Configuration” on page 118).

Bit2: C/T0: Counter/Timer Select.
0: Timer Function: Timer 0 incremented by clock defined by T0M bit (CKCON.3).
1: Counter Function: Timer 0 incremented by high-to-low transitions on external input pin (T0).

Bits1–0: T0M1–T0M0: Timer 0 Mode Select.
These bits select the Timer 0 operation mode.

T0M1	T0M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Two 8-bit counter/timers

25. Programmable Counter Array (PCA0)

The Programmable Counter Array (PCA0) provides enhanced timer functionality while requiring less CPU intervention than the standard 8051 counter/timers. The PCA consists of a dedicated 16-bit counter/timer and six 16-bit capture/compare modules. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the Crossbar to Port I/O when enabled (See **Section "18.1. Priority Crossbar Decoder" on page 149** for details on configuring the Crossbar). The counter/timer is driven by a programmable timebase that can select between seven sources: system clock, system clock divided by four, system clock divided by twelve, the external oscillator clock source divided by 8, smaRTClock Clock divided by 8, Timer 0 overflow, or an external clock signal on the ECI input pin. Each capture/compare module may be configured to operate independently in one of six modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, 8-Bit PWM, or 16-Bit PWM (each mode is described in **Section "25.2. Capture/Compare Modules" on page 251**). The PCA is configured and controlled through the system controller's Special Function Registers. The PCA block diagram is shown in Figure 25.1

Important Note: The PCA Module 5 may be used as a watchdog timer (WDT), and is enabled in this mode following a system reset. **Access to certain PCA registers is restricted while WDT mode is enabled**. See **Section 25.3** for details.

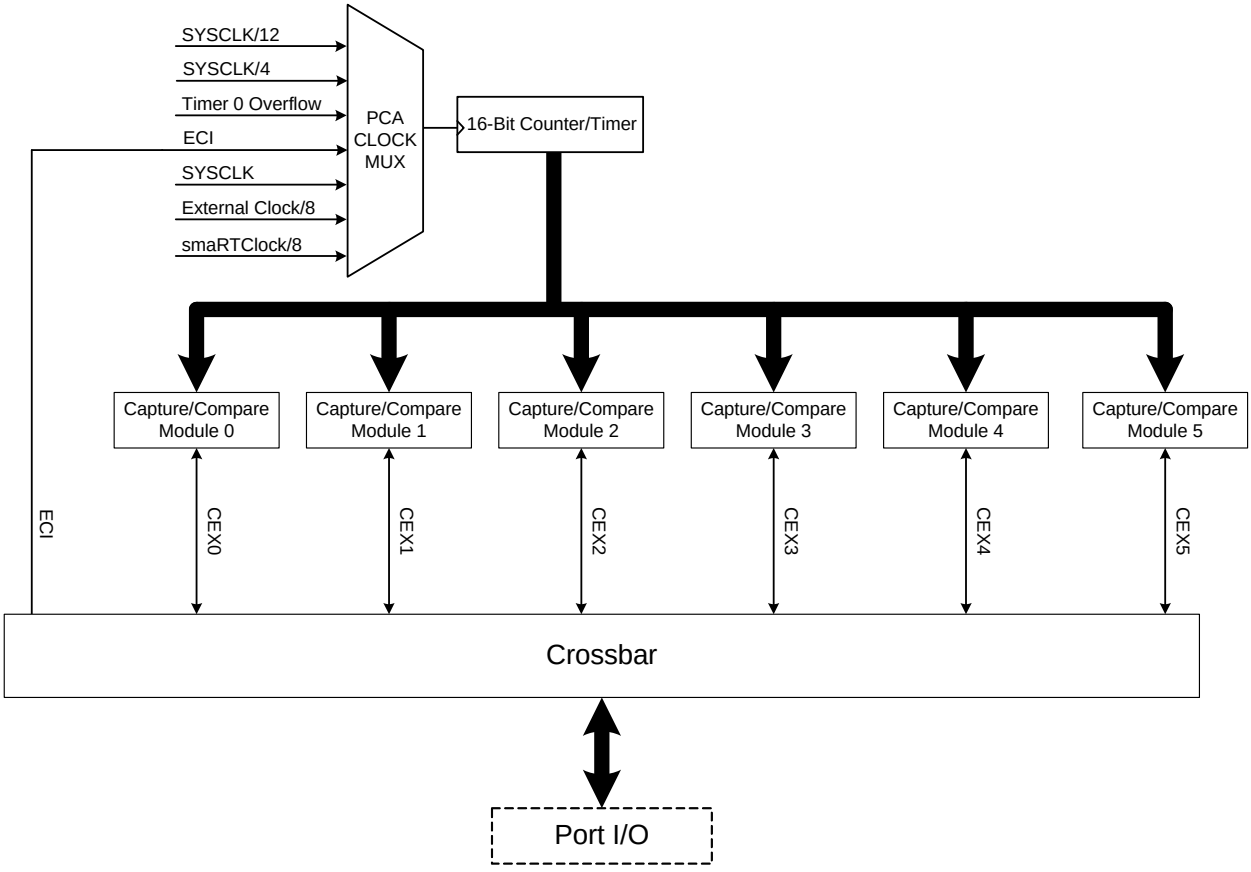


Figure 25.1. PCA Block Diagram

25.4. Register Descriptions for PCA

Following are detailed descriptions of the special function registers related to the operation of the PCA.

SFR Definition 25.1. PCA0CN: PCA Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CF	CR	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xD8

Bit7: CF: PCA Counter/Timer Overflow Flag.
Set by hardware when the PCA Counter/Timer overflows from 0xFFFF to 0x0000. When the Counter/Timer Overflow (CF) interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit6: CR: PCA Counter/Timer Run Control.
This bit enables/disables the PCA Counter/Timer.
0: PCA Counter/Timer disabled.
1: PCA Counter/Timer enabled.

Bit0: CCF5: PCA Module 5 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF5 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit4: CCF4: PCA Module 4 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF4 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit3: CCF3: PCA Module 3 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF3 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit2: CCF2: PCA Module 2 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF2 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit1: CCF1: PCA Module 1 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF1 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit0: CCF0: PCA Module 0 Capture/Compare Flag.
This bit is set by hardware when a match or capture occurs. When the CCF0 interrupt is enabled, setting this bit causes the CPU to vector to the PCA interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

SFR Definition 25.3. PCA0CPMn: PCA Capture/Compare Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PWM16n	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: PCA0CPM0: 0xDA, PCA0CPM1: 0xDB, PCA0CPM2: 0xDC, PCA0CPM3: 0xDD, PCA0CPM4: 0xDE, PCA0CPM5: 0xCE

Bit7: PWM16n: 16-bit Pulse Width Modulation Enable.
This bit selects 16-bit mode when Pulse Width Modulation mode is enabled (PWMn = 1).
0: 8-bit PWM selected.
1: 16-bit PWM selected.

Bit6: ECOMn: Comparator Function Enable.
This bit enables/disables the comparator function for PCA module n.
0: Disabled.
1: Enabled.

Bit5: CAPPn: Capture Positive Function Enable.
This bit enables/disables the positive edge capture for PCA module n.
0: Disabled.
1: Enabled.

Bit4: CAPNn: Capture Negative Function Enable.
This bit enables/disables the negative edge capture for PCA module n.
0: Disabled.
1: Enabled.

Bit3: MATn: Match Function Enable.
This bit enables/disables the match function for PCA module n. When enabled, matches of the PCA counter with a module's capture/compare register cause the CCFn bit in PCA0MD register to be set to logic 1.
0: Disabled.
1: Enabled.

Bit2: TOGn: Toggle Function Enable.
This bit enables/disables the toggle function for PCA module n. When enabled, matches of the PCA counter with a module's capture/compare register cause the logic level on the CEXn pin to toggle. If the PWMn bit is also set to logic 1, the module operates in Frequency Output Mode.
0: Disabled.
1: Enabled.

Bit1: PWMn: Pulse Width Modulation Mode Enable.
This bit enables/disables the PWM function for PCA module n. When enabled, a pulse width modulated signal is output on the CEXn pin. 8-bit PWM is used if PWM16n is cleared; 16-bit mode is used if PWM16n is set to logic 1. If the TOGn bit is also set, the module operates in Frequency Output Mode.
0: Disabled.
1: Enabled.

Bit0: ECCFn: Capture/Compare Flag Interrupt Enable.
This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt.
0: Disable CCFn interrupts.
1: Enable a Capture/Compare Flag interrupt request when CCFn is set.

26. C2 Interface

C8051F41x devices include an on-chip Silicon Laboratories 2-Wire (C2) debug interface to allow Flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

26.1. C2 Interface Registers

The following describes the C2 registers necessary to perform Flash programming functions through the C2 interface. All C2 registers are accessed through the C2 interface as described in the C2 Interface Specification.

C2 Register Definition 26.1. C2ADD: C2 Address

								Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

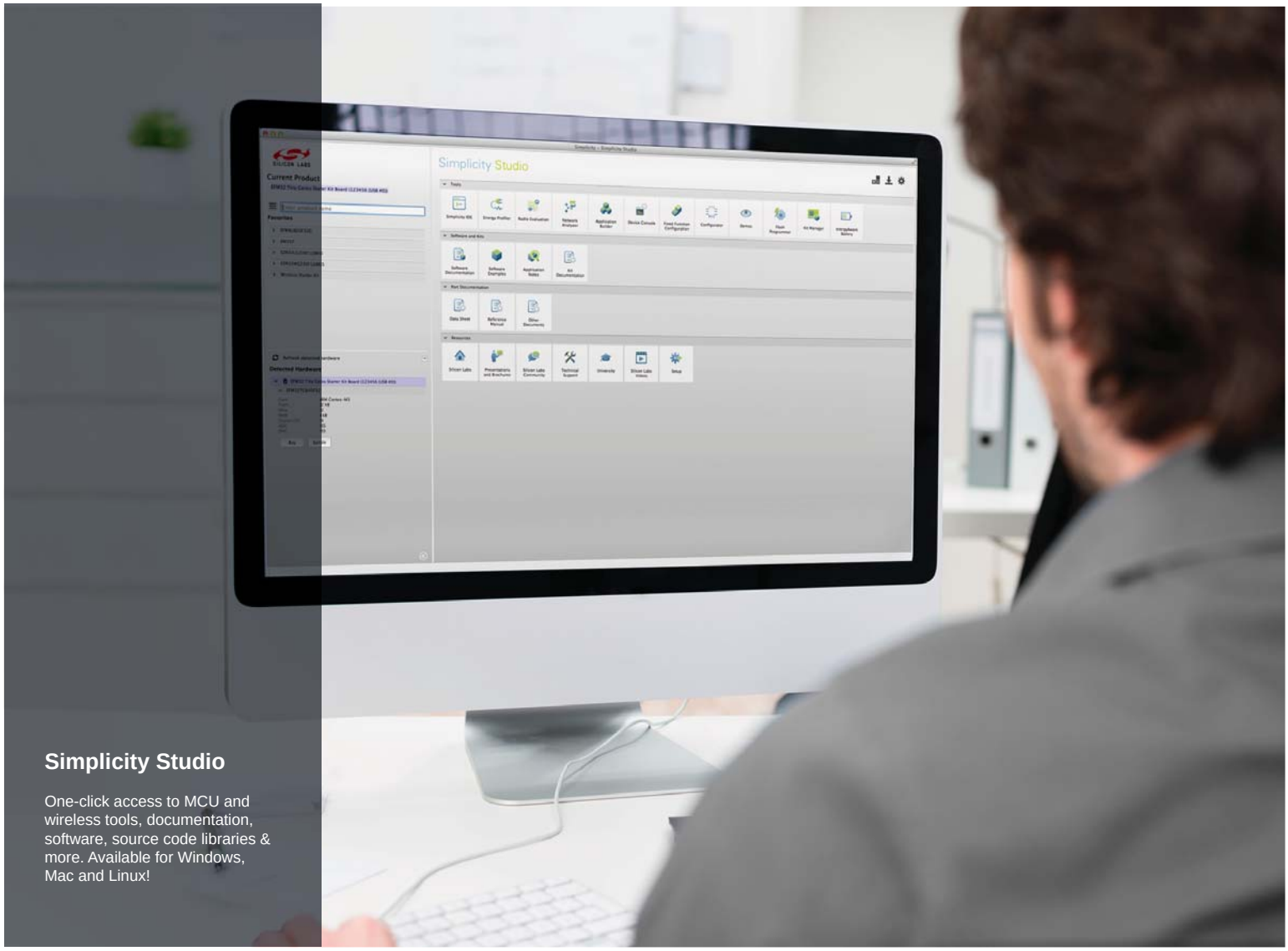
Bits7-0: The C2ADD register is accessed via the C2 interface to select the target Data register for C2 Data Read and Data Write commands.

Address	Description
0x00	Selects the Device ID register for Data Read instructions (DEVICEID)
0x01	Selects the Revision ID register for Data Read instructions (REVID)
0x02	Selects the C2 Flash Programming Control register for Data Read/Write instructions (FPCTL)
0xB4	Selects the C2 Flash Programming Data register for Data Read/Write instructions (FPDAT)

C2 Register Definition 26.2. DEVICEID: C2 Device ID

								Reset Value
								00001011
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

This read-only register returns the 8-bit device ID: 0x0C (C8051F41x).



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