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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SIO
Peripherals	POR, WDT
Number of I/O	21
Program Memory Size	4.5KB (4.5K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	176 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705p6acdw

Chapter 4
Resets

Chapter 5
Interrupts

Chapter 6
Input/Output Ports

Chapter 7
Serial Input/Output Port (SIOP)

Chapter 8
Capture/Compare Timer

Chapter 9
Analog Subsystem

Chapter 10
EPROM

1.3.8 TCMP

This pin is the output from the 16-bit timer's output compare function. It is low after reset. Refer to Chapter 8 Capture/Compare Timer.

1.3.9 $\overline{IRQ}/V_{PP}$ (Maskable Interrupt Request)

This input pin drives the asynchronous interrupt function of the MCU in user mode and provides the V_{PP} programming voltage in bootloader mode. The MCU will complete the current instruction being executed before it responds to the $\overline{IRQ}$ interrupt request. When the $\overline{IRQ}/V_{PP}$ pin is driven low, the event is latched internally to signify an interrupt has been requested. When the MCU completes its current instruction, the interrupt latch is tested. If the interrupt latch is set and the interrupt mask bit (I bit) in the condition code register is clear, the MCU will begin the interrupt sequence.

Depending on the MOR LEVEL bit, the $\overline{IRQ}/V_{PP}$ pin will trigger an interrupt on either a negative edge at the $\overline{IRQ}/V_{PP}$ pin and/or while the $\overline{IRQ}/V_{PP}$ pin is held in the low state. In either case, the $\overline{IRQ}/V_{PP}$ pin must be held low for at least one t_{ILIH} time period. If the edge- and level-sensitive mode is selected (LEVEL bit set), the $\overline{IRQ}/V_{PP}$ input pin requires an external resistor connected to V_{DD} for wired-OR operation. If the $\overline{IRQ}/V_{PP}$ pin is not used, it must be tied to the V_{DD} supply. The $\overline{IRQ}/V_{PP}$ pin input circuitry contains an internal Schmitt trigger to improve noise immunity. Refer to Chapter 5 Interrupts.

NOTE

If the voltage level applied to the $\overline{IRQ}/V_{PP}$ pin exceeds V_{DD}, it may affect the MCU's mode of operation. See Chapter 3 Operating Modes.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PORTA) See page 37.	Read:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Write:								
		Reset:	Unaffected by reset							
$0001	Port B Data Register (PORTB) See page 38.	Read:	PB7	PB6	PB5	0	0	0	0	0
		Write:								
		Reset:	Unaffected by reset							
$0002	Port C Data Register (PORTC) See page 38.	Read:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Write:								
		Reset:	Unaffected by reset							
$0003	Port D Data Register (PORTD) See page 39.	Read:	PD7	0	PD5	1	0	0	0	0
		Write:								
		Reset:	Unaffected by reset							
$0004	Port A Data Direction Register (DDRA) See page 37.	Read:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0005	Port B Data Direction Register (DDRB) See page 38.	Read:	DDRB7	DDRB6	DDRB5	1	1	1	1	1
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0006	Port C Data Direction Register (DDRC) See page 38.	Read:	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0007	Port D Data Direction Register (DDRD) See page 39.	Read:	0	0	DDRD5	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0008	Unimplemented									
$0009	Unimplemented									
$000A	SIOP Control Register (SCR) See page 43.	Read:	0	SPE	0	MSTR	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000B	SIOP Status Register (SSR) See page 44.	Read:	SPIF	DCOL	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000C	SIOP Data Register (SDR) See page 44.	Read:	SDR7	SDR6	SDR5	SDR4	SDR3	SSDR2	SDR1	SDR0
		Write:								
		Reset:	Unaffected by reset							

= Unimplemented R = Reserved U = Undetermined

Figure 2-3. I/O and Control Register Summary (Sheet 1 of 3)

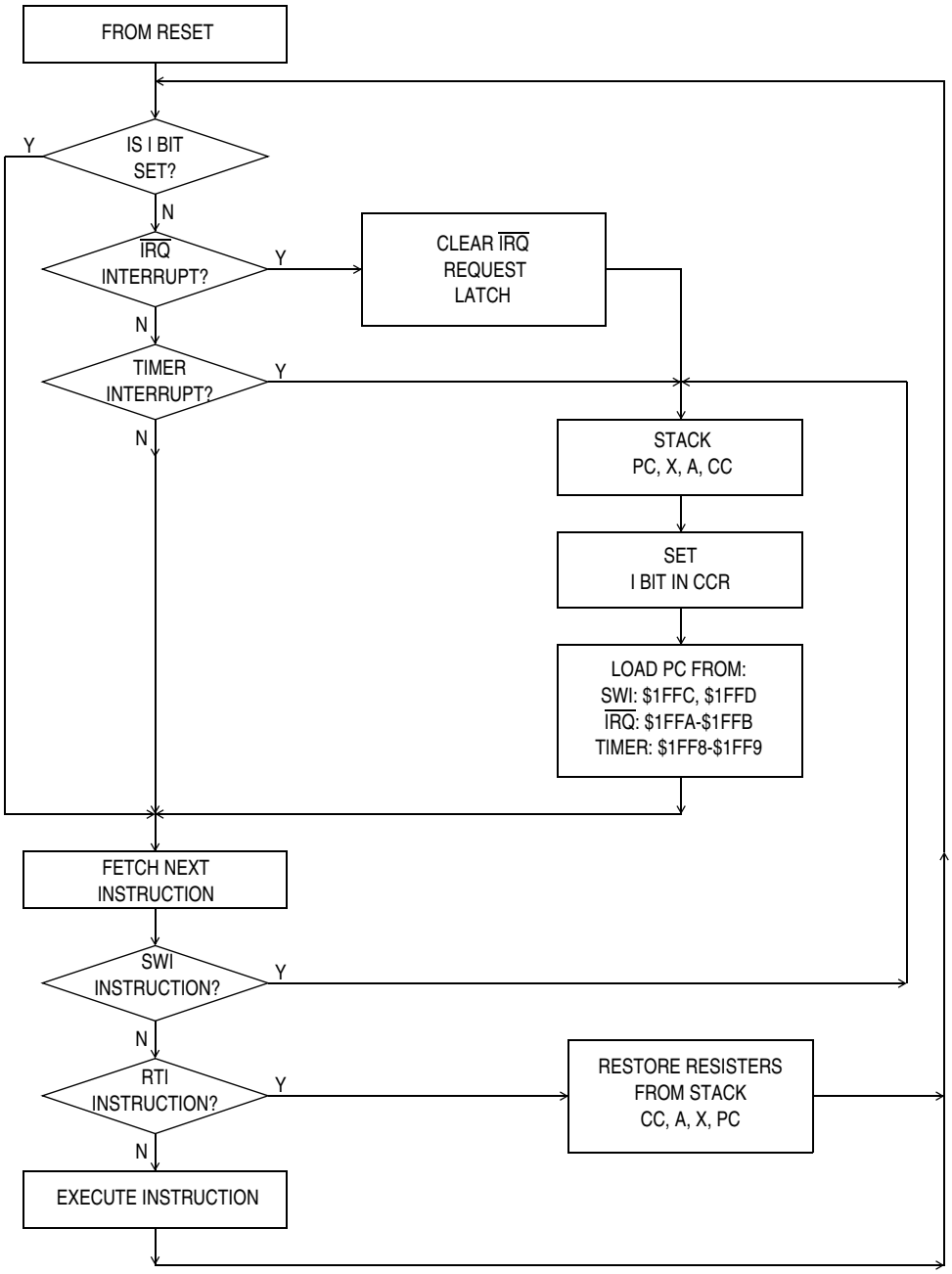


Figure 5-1. Interrupt Processing Flowchart

5.2 Interrupt Types

The interrupts fall into three categories: reset, software, and hardware.

5.2.1 Reset Interrupt Sequence

The reset function is not in the strictest sense an interrupt; however, it is acted upon in a similar manner as shown in Figure 5-1. A low-level input on the $\overline{\text{RESET}}$ pin or internally generated RST signal causes the program to vector to its starting address which is specified by the contents of memory locations $1FFE and $1FFF. The I bit in the condition code register is also set. The MCU is configured to a known state during this type of reset as previously described in Chapter 4 Resets.

5.2.2 Software Interrupt (SWI)

The SWI is an executable instruction. It is also a non-maskable interrupt since it is executed regardless of the state of the I bit in the CCR. As with any instruction, interrupts pending during the previous instruction will be serviced before the SWI opcode is fetched. The interrupt service routine address for the SWI instruction is specified by the contents of memory locations $1FFC and $1FFD.

5.2.3 Hardware Interrupts

All hardware interrupts are maskable by the I bit in the CCR. If the I bit is set, all hardware interrupts (internal and external) are disabled. Clearing the I bit enables the hardware interrupts. Four hardware interrupts are explained in the following subsections.

5.2.3.1 External Interrupt ($\overline{IRQ}$)

The $\overline{\text{IRQ}}/V_{PP}$ pin drives an asynchronous interrupt to the CPU. An edge detector flip-flop is latched on the falling edge of $\overline{\text{IRQ}}/V_{PP}$. If either the output from the internal edge detector flip-flop or the level on the $\overline{\text{IRQ}}/V_{PP}$ pin is low, a request is synchronized to the CPU to generate the IRQ interrupt. If the LEVEL bit in the mask option register is clear (edge-sensitive only), the output of the internal edge detector flip-flop is sampled and the input level on the $\overline{\text{IRQ}}/V_{PP}$ pin is ignored. The interrupt service routine address is specified by the contents of memory locations $1FFA and $1FFB. If the port A interrupts are enabled by the MOR, they generate external interrupts identically to the $\overline{\text{IRQ}}/V_{PP}$ pin.

NOTE

The internal interrupt latch is cleared nine internal clock cycles after the interrupt is recognized (immediately after location $1FFA is read). Therefore, another external interrupt pulse could be latched during the $\overline{IRQ}$ service routine.

Another interrupt will be serviced if the $\overline{IRQ}$ pin is still in a low state when the RTI in the service routine is executed.

5.2.3.2 Input Capture Interrupt

The input capture interrupt is generated by the 16-bit timer as described in Chapter 8 Capture/Compare Timer. The input capture interrupt flag is located in register TSR and its corresponding enable bit can be found in register TCR. The I bit in the CCR must be clear for the input capture interrupt to be enabled. The interrupt service routine address is specified by the contents of memory locations $1FF8 and $1FF9.

5.2.3.3 Output Compare Interrupt

The output compare interrupt is generated by a 16-bit timer as described in Chapter 8 Capture/Compare Timer**.** The output compare interrupt flag is located in register TSR and its corresponding enable bit can be found in register TCR. The I bit in the CCR must be clear for the output compare interrupt to be enabled. The interrupt service routine address is specified by the contents of memory locations $1FF8 and $1FF9.

5.2.3.4 Timer Overflow Interrupt

The timer overflow interrupt is generated by the 16-bit timer as described in Chapter 8 Capture/Compare Timer. The timer overflow interrupt flag is located in register TSR and its corresponding enable bit can be found in register TCR. The I bit in the CCR must be clear for the timer overflow interrupt to be enabled. This internal interrupt will vector to the interrupt service routine located at the address specified by the contents of memory locations $1FF8 and $1FF9.

Chapter 8
Capture/Compare Timer

8.1 Introduction

This section describes the operation of the 16-bit capture/compare timer. Figure 8-1 shows the structure of the capture/compare subsystem.

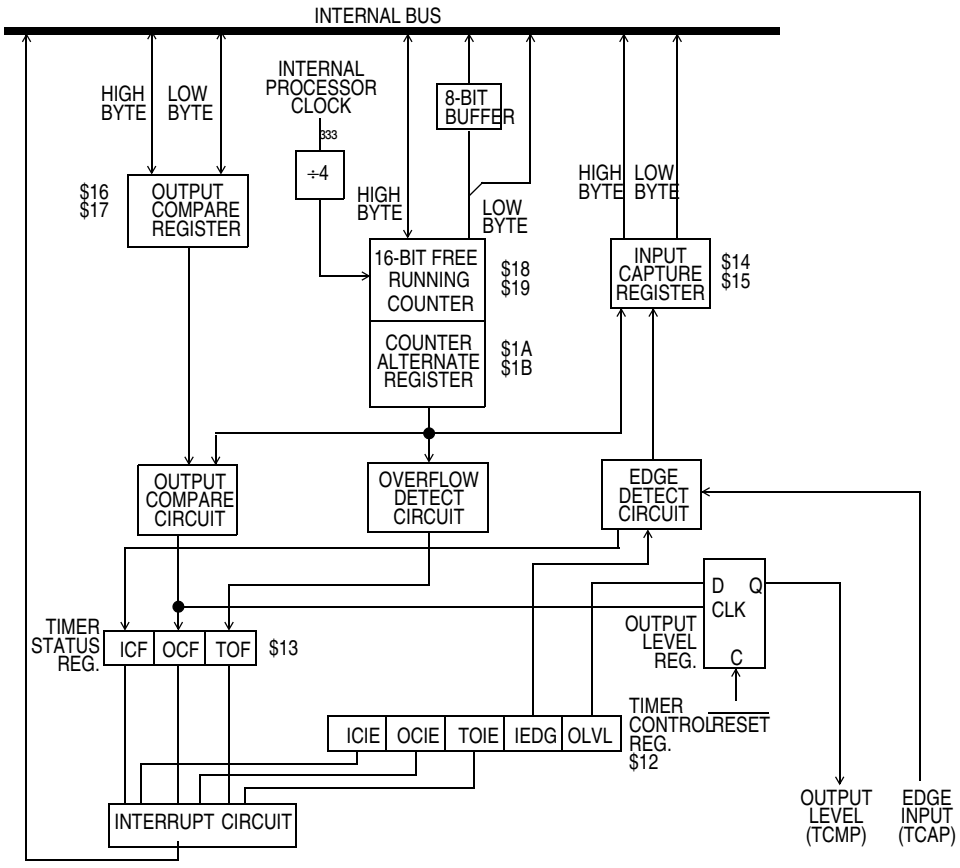


Figure 8-1. Capture/Compare Timer Block Diagram

Chapter 10
EPROM

10.1 Introduction

The user EPROM consists of 48 bytes of user page zero EPROM from $0020 to $004F, 4608 bytes of user EPROM from $0100 to $12FF, the two MOR reset values located at $1EFF and $1F00, and 16 bytes of user vectors EPROM from $1FF0 to $1FFF. The bootloader ROM and vectors are located from $1F01 to $1FEF.

10.2 EPROM Erasing

NOTE

Only parts packaged in a windowed package may be erased. Others are one-time programmable and may not be erased by UV exposure.

The MC68HC705P6A can be erased by exposure to a high-intensity ultraviolet (UV) light with a wavelength of 2537 angstroms. The recommended dose (UV intensity multiplied by exposure time) is 15 Ws/cm^2. UV lamps without shortwave filters should be used, and the EPROM device should be positioned about one inch from the UV lamp. An erased EPROM byte will read as $00.

10.3 EPROM Programming Sequence

The bootloader software goes through a complete write cycle of the EPROM including the MOR. This is followed by a verify cycle which continually branches in a loop if an error is found. A sample routine to program a byte of EPROM is shown in Table 10-1.

NOTE

To avoid damage to the MCU, V_{DD} must be applied to the MCU before V_{PP}.

10.4 EPROM Registers

Three registers are associated with the EPROM: the EPROM programming register (EPROG) and the two mask option registers (MOR). The EPROG register controls the actual programming of the EPROM bytes and the MOR. The MOR registers control the six mask options found on the ROM version of this MCU (MC68HC05P6), the EPROM security feature, and eight additional port A interrupt options.

10.5 EPROM Programming Register (EPROG)

This register is used to program the EPROM array. Only the ELAT and EPGM bits are available. Table 10-1 shows the location of each bit in the EPROG register and the state of these bits coming out of reset. All the bits in the EPROG register are cleared by reset.

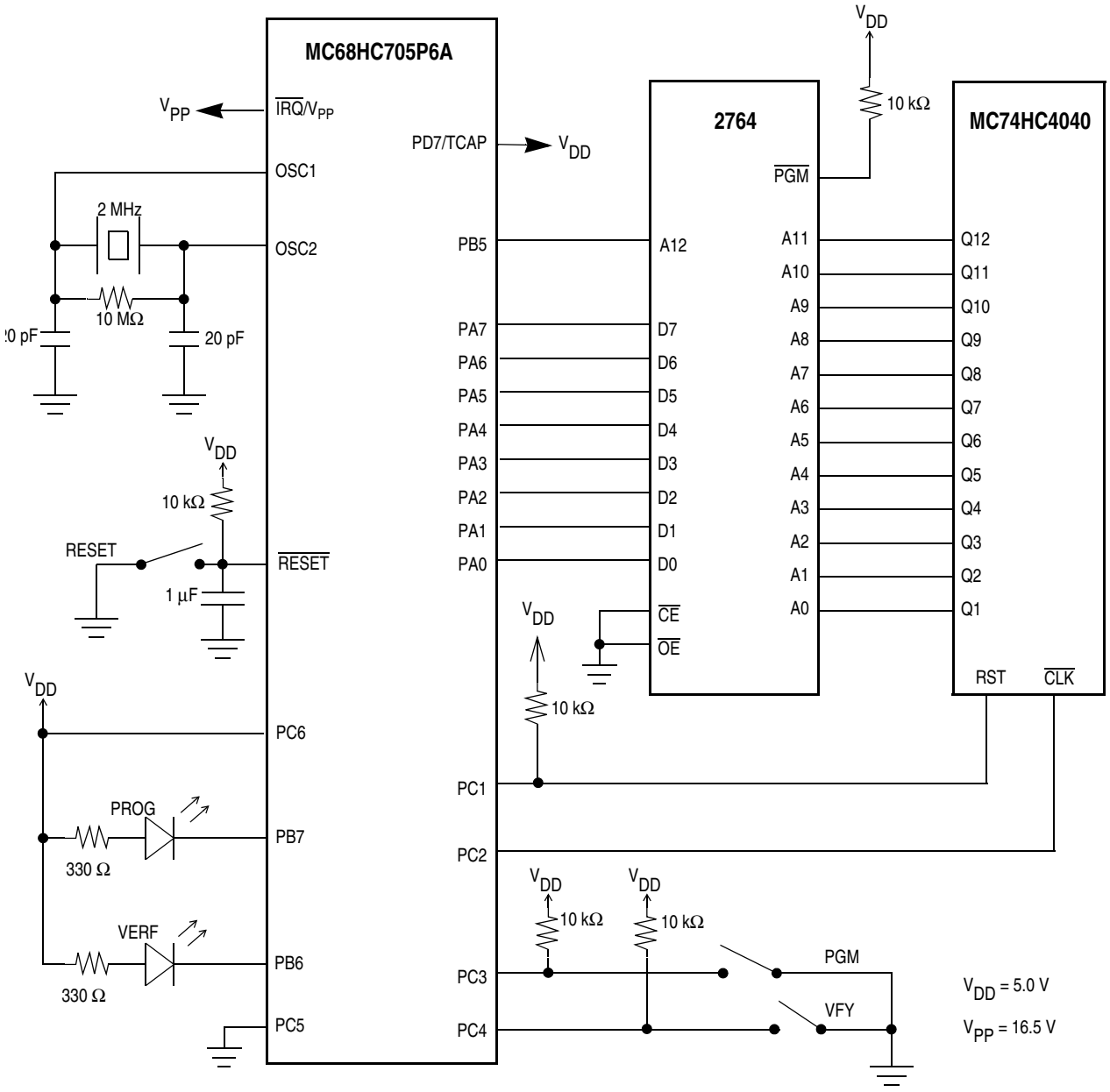


Figure 10-3. MC68HC705P6A EPROM Programming Schematic Diagram

Chapter 12
Central Processor Unit (CPU) Core

12.1 Introduction

The MC68HC705P6A has an 8-K memory map. Therefore, it uses only the lower 13 bits of the address bus. In the following discussion, the upper three bits of the address bus can be ignored. Also, the STOP instruction can be modified to place the MCU in either the normal stop mode or the halt mode by means of a MOR bit. All other instructions and registers behave as described in this section.

12.2 Registers

The MCU contains five registers which are hard-wired within the CPU and are not part of the memory map. These five registers are shown in Figure 12-1 and are described in the following paragraphs.

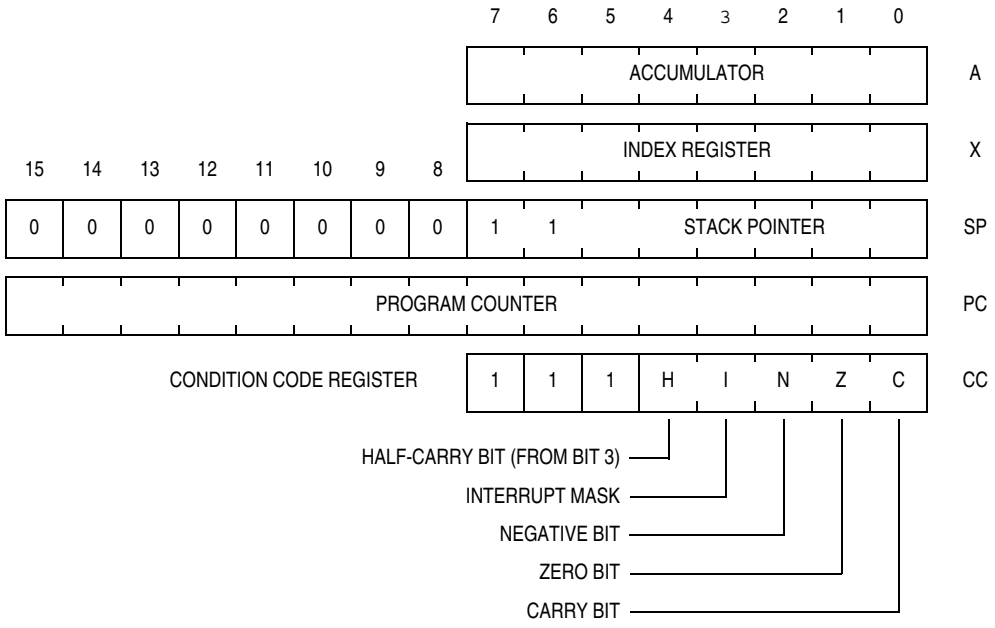


Figure 12-1. MC68HC05 Programming Model

12.2.1 Accumulator

The accumulator is a general-purpose 8-bit register as shown in Figure 12-1. The CPU uses the accumulator to hold operands and results of arithmetic calculations or non-arithmetic operations. The accumulator is unaffected by a reset of the device.

I — Interrupt Mask Bit

When the interrupt mask is set, the internal and external interrupts are disabled. Interrupts are enabled when the interrupt mask is cleared. When an interrupt occurs, the interrupt mask is automatically set after the CPU registers are saved on the stack, but before the interrupt vector is fetched. If an interrupt request occurs while the interrupt mask is set, the interrupt request is latched. Normally, the interrupt is processed as soon as the interrupt mask is cleared.

A return from interrupt (RTI) instruction pulls the CPU registers from the stack, restoring the interrupt mask to its state before the interrupt was encountered. After any reset, the interrupt mask is set and can only be cleared by the clear I bit (CLI), STOP, or WAIT instructions.

N — Negative Bit

The negative bit is set when the result of the last arithmetic operation, logical operation, or data manipulation was negative. (Bit 7 of the result was a logic one.)

The negative bit can also be used to check an often-tested flag by assigning the flag to bit 7 of a register or memory location. Loading the accumulator with the contents of that register or location then sets or clears the negative bit according to the state of the flag.

Z — Zero Bit

The zero bit is set when the result of the last arithmetic operation, logical operation, data manipulation, or data load operation was zero.

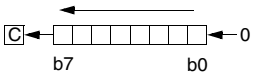
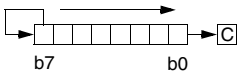
C — Carry/Borrow Bit

The carry/borrow bit is set when a carry out of bit 7 of the accumulator occurred during the last arithmetic operation, logical operation, or data manipulation. The carry/borrow bit is also set or cleared during bit test and branch instructions and during shifts and rotates. This bit is not set by an INC or DEC instruction.

13.4 Instruction Set Summary

Table 13-6 is an alphabetical list of all M68HC05 instructions and shows the effect of each instruction on the condition code register.

Table 13-6. Instruction Set Summary (Sheet 1 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ADC #*opr* ADC *opr* ADC *opr* ADC *opr*,X ADC *opr*,X ADC ,X	Add with Carry	A ← (A) + (M) + (C)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A9 B9 C9 D9 E9 F9	ii dd hh ll ee ff ff	2 3 4 5 4 3
ADD #*opr* ADD *opr* ADD *opr* ADD *opr*,X ADD *opr*,X ADD ,X	Add without Carry	A ← (A) + (M)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	AB BB CB DB EB FB	ii dd hh ll ee ff ff	2 3 4 5 4 3
AND #*opr* AND *opr* AN*D opr* AND *opr*,X AND *opr*,X AND ,X	Logical AND	A ← (A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A4 B4 C4 D4 E4 F4	ii dd hh ll ee ff ff	2 3 4 5 4 3
ASL *opr* ASLA ASLX ASL *opr*,X ASL ,X	Arithmetic Shift Left (Same as LSL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
ASR *opr* ASRA ASRX ASR *opr*,X ASR ,X	Arithmetic Shift Right		—	—	↕	↕	↕	DIR INH INH IX1 IX	37 47 57 67 77	dd ff 	5 3 3 6 5
BCC *rel*	Branch if Carry Bit Clear	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BCLR *n opr*	Clear Bit n	Mn ← 0	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BCS *rel*	Branch if Carry Bit Set (Same as BLO)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BEQ *rel*	Branch if Equal	PC ← (PC) + 2 + *rel* ? Z = 1	—	—	—	—	—	REL	27	rr	3
BHCC *rel*	Branch if Half-Carry Bit Clear	PC ← (PC) + 2 + *rel* ? H = 0	—	—	—	—	—	REL	28	rr	3
BHCS *rel*	Branch if Half-Carry Bit Set	PC ← (PC) + 2 + *rel* ? H = 1	—	—	—	—	—	REL	29	rr	3
BHI *rel*	Branch if Higher	PC ← (PC) + 2 + *rel* ? C ∨ Z = 0	—	—	—	—	—	REL	22	rr	3
BHS *rel*	Branch if Higher or Same	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3

14.10 Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Frequency of operation Crystal option External clock option	f_{OSC}	— DC	4.2 4.2	MHz
Internal operating frequency Crystal ($f_{OSC} \div 2$) External clock ($f_{OSC} \div 2$)	f_{OP}	— DC	2.1 2.1	MHz
Cycle time	t_{CYC}	476	—	ns
Crystal oscillator startup time	t_{OXOV}	—	100	ms
Stop mode recovery startup time (crystal oscillator)	t_{ILCH}	—	100	ms
$\overline{\text{RESET}}$ pulse width	t_{RL}	1.5	—	t_{CYC}
Interrupt pulse width low (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period[2]	t_{ILIL}	Note 2	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	200	—	ns
A/D On current stabilization time	t_{ADON}	Q	100	µs

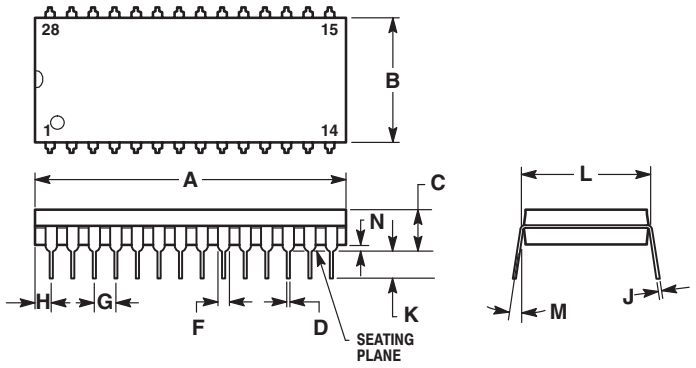
1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +125°C, unless otherwise noted
2. The minimum period, t_{ILIL}, should not be less than the number of cycle times it takes to execute the interrupt service routine plus 19 t_{CYC}.

Chapter 15
Mechanical Specifications

15.1 Introduction

The MC68HC705P6A is available in either a 28-pin plastic dual in-line (PDIP) or a 28-pin small outline integrated circuit (SOIC) package.

15.2 Plastic Dual In-Line Package (Case 710)



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

Chapter 16
Ordering Information

16.1 Introduction

This section contains ordering information for the available package types.

16.2 MC Order Numbers

The following table shows the MC order numbers for the available package types.

MC Order Number	Operating Temperature Range
MC68HC705P6ACP[1] (extended)	–40°C to 85°C
MC68HC705P6ACDW[2] (extended)	–40°C to 85°C

1. P = Plastic dual in-line package
2. DW = Small outline integrated circuit (SOIC) package