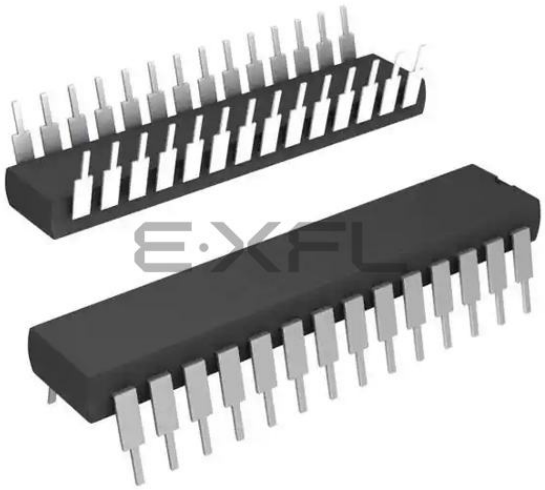


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SIO
Peripherals	POR, WDT
Number of I/O	21
Program Memory Size	4.5KB (4.5K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	176 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705p6acp

Chapter 15
Mechanical Specifications

Chapter 16
Ordering Information

Chapter 1
General Description

1.1 Introduction

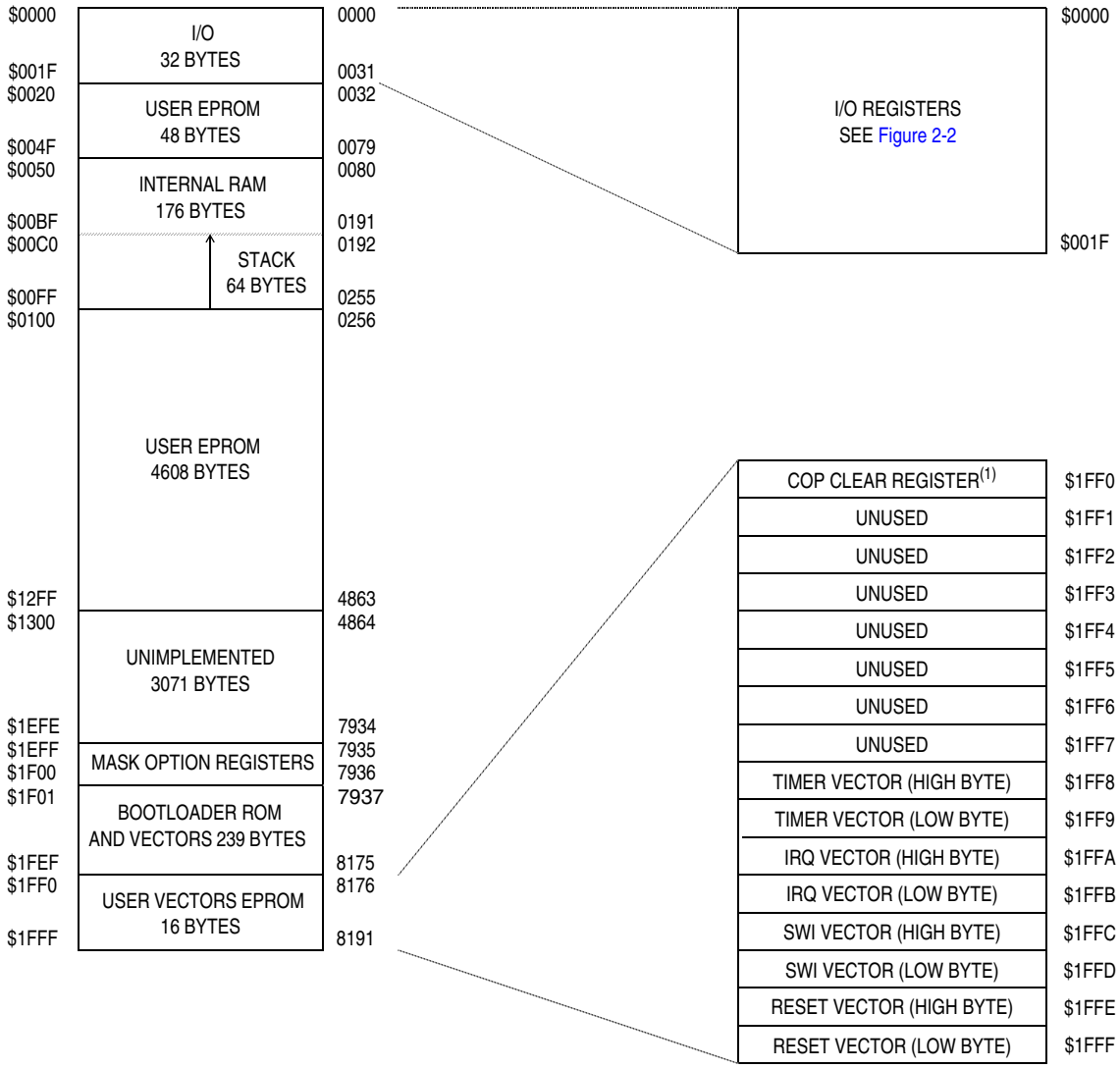
The MC68HC705P6A is an EPROM version of the MC68HC05P6 microcontroller. It is a low-cost combination of an M68HC05 Family microprocessor with a 4-channel, 8-bit analog-to-digital (A/D) converter, a 16-bit timer with output compare and input capture, a serial communications port (SIOP), and a computer operating properly (COP) watchdog timer. The M68HC05 CPU core contains 176 bytes of RAM, 4672 bytes of user EPROM, 239 bytes of bootloader ROM, and 21 input/output (I/O) pins (20 bidirectional, 1 input-only). This device is available in either a 28-pin plastic dual in-line (PDIP) or a 28-pin small outline integrated circuit (SOIC) package.

A functional block diagram of the MC68HC705P6A is shown in Figure 1-1.

1.2 Features

Features of the MC68HC705P6A include:

- Low cost
- M68HC05 core
- 28-pin SOIC, PDIP, or windowed DIP package
- 4672 bytes of user EPROM (including 48 bytes of page zero EPROM and 16 bytes of user vectors)
- 239 bytes of bootloader ROM
- 176 bytes of on-chip RAM
- 4-channel 8-bit A/D converter
- SIOP serial communications port
- 16-bit timer with output compare and input capture
- 20 bidirectional I/O lines and 1 input-only line
- PC0 and PC1 high-current outputs
- Single-chip, bootloader, and test modes
- Power-saving stop, halt, and wait modes
- Static EPROM mask option register (MOR) selectable options:
  - COP watchdog timer enable or disable
  - Edge-sensitive or edge- and level-sensitive external interrupt
  - SIOP most significant bit (MSB) or least significant bit (LSB) first
  - SIOP clock rates: OSC divided by 8, 16, 32, or 64
  - Stop instruction mode, STOP or HALT
  - EPROM security external lockout
  - Programmable keyscan (pullups/interrupts) on PA0–PA7



Note 1. Writing zero to bit 0 of $1FF0 clears the COP watchdog timer. Reading $1FF0 returns user EPROM data.

Figure 2-1. MC68HC705P6A User Mode Memory Map

6.3 Port B

Port B is a 3-bit bidirectional port which can share pins PB5–PB7 with the SIOP communications subsystem. The port B data register is located at address $0001 and its data direction register (DDR) is located at address $0005. The contents of the port B data register are indeterminate at initial powerup and must be initialized by user software. Reset does not affect the data registers, but clears the DDRs, thereby setting all of the port pins to input mode. Writing a 1 to a DDR bit sets the corresponding port pin to output mode (see Figure 6-2).

Port B may be used for general I/O applications when the SIOP subsystem is disabled. The SPE bit in register SPCR is used to enable/disable the SIOP subsystem. When the SIOP subsystem is enabled, port B registers are still accessible to software. Writing to either of the port B registers while a data transfer is under way could corrupt the data. See Chapter 7 Serial Input/Output Port (SIOP) for a discussion of the SIOP subsystem.

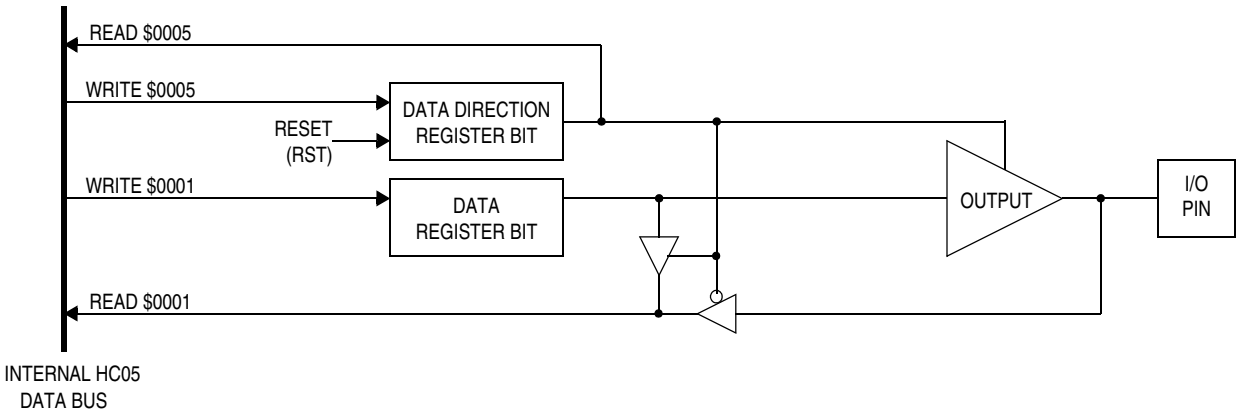


Figure 6-2. Port B I/O Circuitry

6.4 Port C

Port C is an 8-bit bidirectional port which can share pins PC3–PC7 with the A/D subsystem. The port C data register is located at address $0002 and its data direction register (DDR) is located at address $0006. The contents of the port C data register are indeterminate at initial powerup and must be initialized by user software. Reset does not affect the data registers, but clears the DDRs, thereby setting all of the port pins to input mode. Writing a 1 to a DDR bit sets the corresponding port pin to output mode (see Figure 6-3).

Port C may be used for general I/O applications when the A/D subsystem is disabled. The ADON bit in register ADSC is used to enable/disable the A/D subsystem. Care must be exercised when using pins PC0–PC2 while the A/D subsystem is enabled. Accidental changes to bits that affect pins PC3–PC7 in the data or DDR registers will produce unpredictable results in the A/D subsystem. See Chapter 9 Analog Subsystem.

7.2 SIOP Signal Format

The SIOP subsystem is software configurable for master or slave operation. No external mode selection inputs are available (for instance, slave select pin).

7.2.1 Serial Clock (SCK)

The state of the SCK output normally remains a logic 1 during idle periods between data transfers. The first falling edge of SCK signals the beginning of a data transfer. At this time, the first bit of received data may be presented at the SDI pin and the first bit of transmitted data is presented at the SDO pin (see Figure 7-2). Data is captured at the SDI pin on the rising edge of SCK. The transfer is terminated upon the eighth rising edge of SCK.

The master and slave modes of operation differ only by the sourcing of SCK. In master mode, SCK is driven from an internal source within the MCU. In slave mode, SCK is driven from a source external to the MCU. The SCK frequency is dependent upon the SPR0 and SPR1 bits located in the mask option register. Refer to 11.2 Mask Option Register for a description of available SCK frequencies.

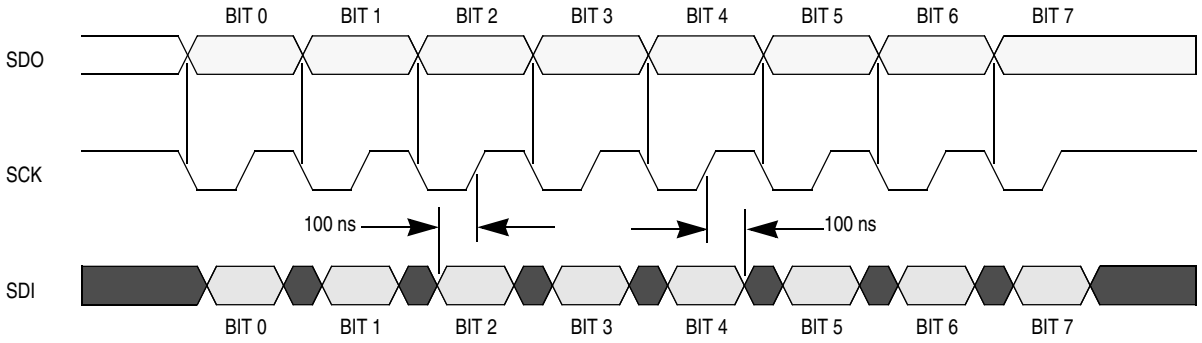


Figure 7-2. SIOP Timing Diagram

7.2.2 Serial Data Input (SDI)

The SDI pin becomes an input as soon as the SIOP subsystem is enabled. New data may be presented to the SDI pin on the falling edge of SCK.However, valid data must be present at least 100 nanoseconds before the rising edge of SCK and remain valid for 100 nanoseconds after the rising edge of SCK. See Figure 7-2.

7.2.3 Serial Data Output (SDO)

The SDO pin becomes an output as soon as the SIOP subsystem is enabled. Prior to enabling the SIOP, PB5 can be initialized to determine the beginning state. While the SIOP is enabled, PB5 cannot be used as a standard output since that pin is connected to the last stage of the SIOP serial shift register. Mask option register bit LSBF permits data to be transmitted in either the MSB first format or the LSB first format. Refer to 11.2 Mask Option Register for MOR LSBF programming information.

On the first falling edge of SCK, the first data bit will be shifted out to the SDO pin. The remaining data bits will be shifted out to the SDO pin on subsequent falling edges of SCK. The SDO pin will present valid data at least 100 nanoseconds before the rising edge of the SCK and remain valid for 100 nanoseconds after the rising edge of SCK. See Figure 7-2.

8.3.1 Timer Control Register

The timer control register (TCR), shown in Figure 8-2, performs these functions:

- Enables input capture interrupts
- Enables output compare interrupts
- Enables timer overflow interrupts
- Controls the active edge polarity of the TCAP signal
- Controls the active level of the TCMP output

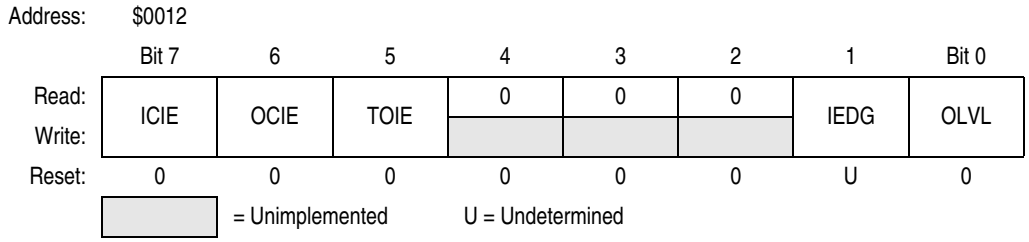


Figure 8-2. Timer Control Register (TCR)

ICIE — Input Capture Interrupt Enable

This read/write bit enables interrupts caused by an active signal on the TCAP pin. Resets clear the ICIE bit.

1 = Input capture interrupts enabled
0 = Input capture interrupts disabled

OCIE — Output Compare Interrupt Enable

This read/write bit enables interrupts caused by an active signal on the TCMP pin. Resets clear the OCIE bit.

1 = Output compare interrupts enabled
0 = Output compare interrupts disabled

TOIE — Timer Overflow Interrupt Enable

This read/write bit enables interrupts caused by a timer overflow. Reset clear the TOIE bit.

1 = Timer overflow interrupts enabled
0 = Timer overflow interrupts disabled

IEDG — Input Edge

The state of this read/write bit determines whether a positive or negative transition on the TCAP pin triggers a transfer of the contents of the timer register to the input capture register. Resets have no effect on the IEDG bit.

1 = Positive edge (low to high transition) triggers input capture
0 = Negative edge (high to low transition) triggers input capture

OLVL — Output Level

The state of this read/write bit determines whether a logic 1 or logic 0 appears on the TCMP pin when a successful output compare occurs. Resets clear the OLVL bit.

1 = TCMP goes high on output compare
0 = TCMP goes low on output compare

8.3.3 Timer Registers

The timer registers (TRH and TRL), shown in Figure 8-4, contains the current high and low bytes of the 16-bit counter. Reading TRH before reading TRL causes TRL to be latched until TRL is read. Reading TRL after reading the timer status register clears the timer overflow flag (TOF). Writing to the timer registers has no effect.

Address: TRH — $0018

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TRH7	TRH6	TRH5	TRH4	TRH3	TRH2	TRH1	TRH0
Write								
Reset:	1	1	1	1	1	1	1	1

Address: TRL — $0019

	Bit 7	6	5	4	3	2	1	Bit 0
Write:								
Reset:	1	1	1	1	1	1	0	0

= Unimplemented

Figure 8-4. Timer Registers (TRH and TRL)

8.3.4 Alternate Timer Registers

The alternate timer registers (ATRH and ATRL), shown in Figure 8-5, contain the current high and low bytes of the 16-bit counter. Reading ATRH before reading ATRL causes ATRL to be latched until ATRL is read. Reading ATRL has no effect on the timer overflow flag (TOF). Writing to the alternate timer registers has no effect.

Address: ATRH — $001A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	ACRH7	ACRH6	ACRH5	ACRH4	ACRH3	ACRH2	ACRH1	ACRH0
Write:								
Reset:	1	1	1	1	1	1	1	1

Address: ATRL — $001B

	Bit 7	6	5	4	3	2	1	Bit 0
Write:								
Reset:	1	1	1	1	1	1	0	0

= Unimplemented

Figure 8-5. Alternate Timer Registers (ATRH and ATRL)

NOTE

To prevent interrupts from occurring between readings of ATRH and ATRL, set the interrupt flag in the condition code register before reading ATRH, and clear the flag after reading ATRL.

To prevent OCF from being set between the time it is read and the time the output compare registers are updated, use this procedure:

1. Disable interrupts by setting the I bit in the condition code register.
2. Write to OCRH. Compares are now inhibited until OCRL is written.
3. Clear bit OCF by reading timer status register (TSR).
4. Enable the output compare function by writing to OCRL.
5. Enable interrupts by clearing the I bit in the condition code register.

8.4 Timer During Wait/Halt Mode

The CPU clock halts during the wait (or halt) mode, but the timer remains active. If interrupts are enabled, a timer interrupt will cause the processor to exit the wait mode.

8.5 Timer During Stop Mode

In the stop mode, the timer stops counting and holds the last count value if STOP is exited by an interrupt. If STOP is exited by RESET, the counters are forced to $FFFC. During STOP, if at least one valid input capture edge occurs at the TCAP pins, the input capture detect circuit is armed. This does not set any timer flags or wake up the MCU, but if an interrupt is used to exit stop mode, there is an active input capture flag and data from the first valid edge that occurred during the stop mode. If reset is used to exit stop mode, then no input capture flag or data remains, even if a valid input capture edge occurred.

Chapter 10
EPROM

10.1 Introduction

The user EPROM consists of 48 bytes of user page zero EPROM from $0020 to $004F, 4608 bytes of user EPROM from $0100 to $12FF, the two MOR reset values located at $1EFF and $1F00, and 16 bytes of user vectors EPROM from $1FF0 to $1FFF. The bootloader ROM and vectors are located from $1F01 to $1FEF.

10.2 EPROM Erasing

NOTE

Only parts packaged in a windowed package may be erased. Others are one-time programmable and may not be erased by UV exposure.

The MC68HC705P6A can be erased by exposure to a high-intensity ultraviolet (UV) light with a wavelength of 2537 angstroms. The recommended dose (UV intensity multiplied by exposure time) is 15 Ws/cm^2. UV lamps without shortwave filters should be used, and the EPROM device should be positioned about one inch from the UV lamp. An erased EPROM byte will read as $00.

10.3 EPROM Programming Sequence

The bootloader software goes through a complete write cycle of the EPROM including the MOR. This is followed by a verify cycle which continually branches in a loop if an error is found. A sample routine to program a byte of EPROM is shown in Table 10-1.

NOTE

To avoid damage to the MCU, V_{DD} must be applied to the MCU before V_{PP}.

10.4 EPROM Registers

Three registers are associated with the EPROM: the EPROM programming register (EPROG) and the two mask option registers (MOR). The EPROG register controls the actual programming of the EPROM bytes and the MOR. The MOR registers control the six mask options found on the ROM version of this MCU (MC68HC05P6), the EPROM security feature, and eight additional port A interrupt options.

10.5 EPROM Programming Register (EPROG)

This register is used to program the EPROM array. Only the ELAT and EPGM bits are available. Table 10-1 shows the location of each bit in the EPROG register and the state of these bits coming out of reset. All the bits in the EPROG register are cleared by reset.

LEVEL — $\overline{IRQ}$ Edge Sensitivity

If the LEVEL bit is clear, the $\overline{IRQ}/V_{PP}$ pin will only be sensitive to the falling edge of the signal applied to the $\overline{IRQ}/V_{PP}$ pin. If the LEVEL bit is set, the $\overline{IRQ}/V_{PP}$ pin will be sensitive to both the falling edge of the input signal and the logic low level of the input signal on the $\overline{IRQ}/V_{PP}$ pin.

LSBF — SIOP Least Significant Bit First

If the LSBF bit is set, the serial data to and from the SIOP will be transferred least significant bit first. If the LSBF bit is clear, the serial data to and from the SIOP will be transferred most significant bit first.

SPR0 and SPR1 — SIOP Clock Rate

The SPR0 and SPR1 bits determine the clock rate used to transfer the serial data to and from the SIOP. The various clock rates available are given in Table 11-1.

Table 11-1. SIOP Clock Rate

SPR1	SPR0	SIOP Master Clock
0	0	$f_{osc} \div 64$
0	1	$f_{osc} \div 32$
1	0	$f_{osc} \div 16$
1	1	$f_{osc} \div 8$

SWAIT — STOP Instruction Mode

Setting the SWAIT bit will prevent the STOP instruction from stopping the on-board oscillator. Clearing the SWAIT bit will permit the STOP instruction to stop the on-board oscillator and place the MCU in stop mode. Executing the STOP instruction when SWAIT is set will place the MCU in halt mode. See 3.4.1 STOP Instruction for additional information.

SECURE — Security State[1]

If SECURE bit is set, the EPROM is locked.

PA(0:7)PU — Port A Pullups/Interrupt Enable/Disable

If any PA(0:7)PU is selected, that pullup/interrupt is enabled. The interrupt sensitivity will be selected via the LEVEL bit in the same way as the $\overline{IRQ}$ pin.

NOTE

*The port A pullup/interrupt function is **NOT** available on the ROM device, MC68HC05P6.*

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the EPROM/OTPROM difficult for unauthorized users.

Chapter 12
Central Processor Unit (CPU) Core

12.1 Introduction

The MC68HC705P6A has an 8-K memory map. Therefore, it uses only the lower 13 bits of the address bus. In the following discussion, the upper three bits of the address bus can be ignored. Also, the STOP instruction can be modified to place the MCU in either the normal stop mode or the halt mode by means of a MOR bit. All other instructions and registers behave as described in this section.

12.2 Registers

The MCU contains five registers which are hard-wired within the CPU and are not part of the memory map. These five registers are shown in Figure 12-1 and are described in the following paragraphs.

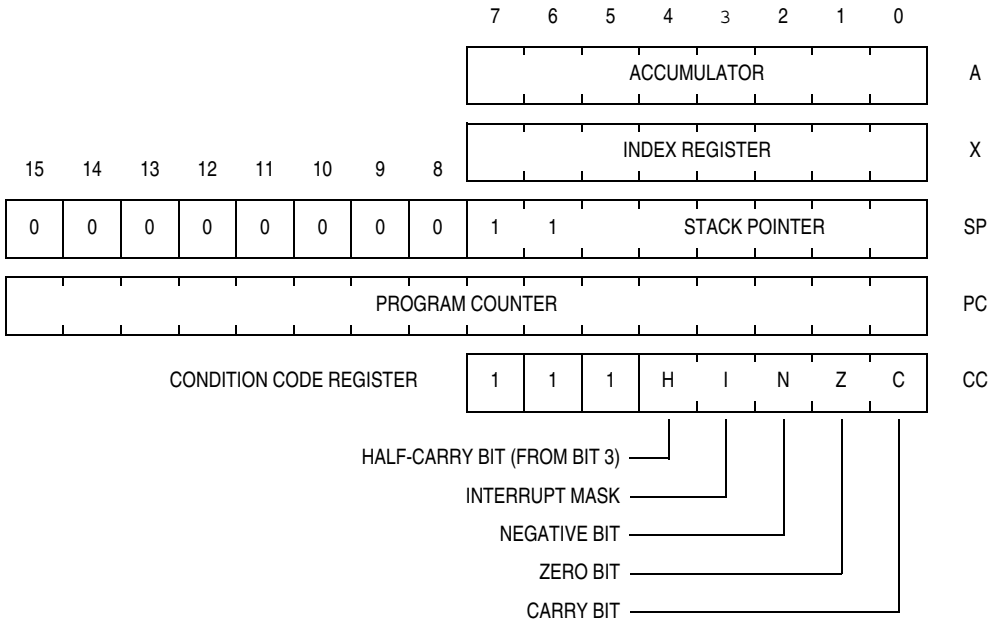


Figure 12-1. MC68HC05 Programming Model

12.2.1 Accumulator

The accumulator is a general-purpose 8-bit register as shown in Figure 12-1. The CPU uses the accumulator to hold operands and results of arithmetic calculations or non-arithmetic operations. The accumulator is unaffected by a reset of the device.

12.2.2 Index Register

The index register shown in Figure 12-1 is an 8-bit register that can perform two functions:

- Indexed addressing
- Temporary storage

In indexed addressing with no offset, the index register contains the low byte of the operand address, and the high byte is assumed to be $00. In indexed addressing with an 8-bit offset, the CPU finds the operand address by adding the index register contents to an 8-bit immediate value. In indexed addressing with a 16-bit offset, the CPU finds the operand address by adding the index register contents to a 16-bit immediate value.

The index register can also serve as an auxiliary accumulator for temporary storage. The index register is unaffected by a reset of the device.

12.2.3 Stack Pointer

The stack pointer shown in Figure 12-1 is a 16-bit register internally. In devices with memory maps less than 64 Kbytes, the unimplemented upper address lines are ignored. The stack pointer contains the address of the next free location on the stack. During a reset or the reset stack pointer (RSP) instruction, the stack pointer is set to $00FF. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

When accessing memory, the 10 most significant bits are permanently set to 0000000011. The six least significant register bits are appended to these 10 fixed bits to produce an address within the range of $00FF to $00C0. Subroutines and interrupts may use up to 64 ($40) locations. If 64 locations are exceeded, the stack pointer wraps around and writes over the previously stored information. A subroutine call occupies two locations on the stack and an interrupt uses five locations.

12.2.4 Program Counter

The program counter shown in Figure 12-1 is a 16-bit register internally. In devices with memory maps less than 64 Kbytes, the unimplemented upper address lines are ignored. The program counter contains the address of the next instruction or operand to be fetched.

Normally, the address in the program counter increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, and interrupt operations load the program counter with an address other than that of the next sequential location.

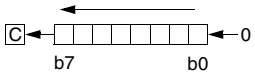
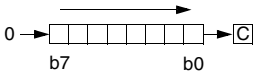
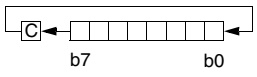
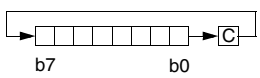
12.2.5 Condition Code Register

The CCR shown in Figure 12-1 is a 5-bit register in which four bits are used to indicate the results of the instruction just executed. The fifth bit is the interrupt mask. These bits can be individually tested by a program, and specific actions can be taken as a result of their state. The condition code register should be thought of as having three additional upper bits that are always ones. Only the interrupt mask is affected by a reset of the device. The following paragraphs explain the functions of the lower five bits of the condition code register.

H — Half Carry Bit

When the half-carry bit is set, it means that a carry occurred between bits 3 and 4 of the accumulator during the last ADD or ADC (add with carry) operation. The half-carry bit is required for binary-coded decimal (BCD) arithmetic operations.

Table 13-6. Instruction Set Summary (Sheet 4 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
LDA #*opr* LDA *opr* LDA *opr* LDA *opr*,X LDA *opr*,X LDA ,X	Load Accumulator with Memory Byte	A ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A6 B6 C6 D6 E6 F6	ii dd hh ll ee ff ff	2 3 4 5 4 3
LDX #*opr* LDX *opr* LDX *opr* LDX *opr*,X LDX *opr*,X LDX ,X	Load Index Register with Memory Byte	X ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AE BE CE DE EE FE	ii dd hh ll ee ff ff	2 3 4 5 4 3
LSL *opr* LSLA LSLX LSL *opr*,X LSL ,X	Logical Shift Left (Same as ASL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
LSR *opr* LSRA LSRX LSR *opr*,X LSR ,X	Logical Shift Right		—	—	0	↕	↕	DIR INH INH IX1 IX	34 44 54 64 74	dd ff 	5 3 3 6 5
MUL	Unsigned Multiply	X : A ← (X) × (A)	0	—	—	—	0	INH	42		1 1
NEG *opr* NEGA NEGX NEG *opr*,X NEG ,X	Negate Byte (Two's Complement)	M ← –(M) = $00 – (M) A ← –(A) = $00 – (A) X ← –(X) = $00 – (X) M ← –(M) = $00 – (M) M ← –(M) = $00 – (M)	—	—	↕	↕	↕	DIR INH INH IX1 IX	30 40 50 60 70	dd ff 	5 3 3 6 5
NOP	No Operation		—	—	—	—	—	INH	9D		2
ORA #*opr* ORA *opr* ORA *opr* ORA *opr*,X ORA *opr*,X ORA ,X	Logical OR Accumulator with Memory	A ← (A) ∨ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AA BA CA DA EA FA	ii dd hh ll ee ff ff	2 3 4 5 4 3
ROL *opr* ROLA ROLX ROL *opr*,X ROL ,X	Rotate Byte Left through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	39 49 59 69 79	dd ff 	5 3 3 6 5
ROR *opr* RORA RORX ROR *opr*,X ROR ,X	Rotate Byte Right through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	36 46 56 66 76	dd ff 	5 3 3 6 5
RSP	Reset Stack Pointer	SP ← $00FF	—	—	—	—	—	INH	9C		2

14.5 5.0-Volt DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	 V_{OL} V_{OH}	 — V_{DD} –0.1	 — —	 0.1 —	 V
Output high voltage (I_{Load} = –0.8 mA) PA0:7, PB5:7, PC2:7, PD5, TCMP (I_{Load} = –5.0 mA) PC0:1	V_{OH}	V_{DD} –0.8 V_{DD} –0.8	— —	— —	V
Output low voltage (I_{Load} = 1.6 mA) PA0:7, PB5:7, PC2:7, PD5, TCMP (I_{Load} = 10 mA) PC0:1	V_{OL}	— —	— —	0.4 0.4	V
Input high voltage PA0:7, PB5:7, PC0:7, PD5, TCAP/PD7, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IH}	0.7 x V_{DD}	—	V_{DD}	V
Input low voltage PA0:7, PB5:7, PC0:7, PD5, TCAP/PD7, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 x V_{DD}	V
Supply current[3], [4] Run Wait[5] (A/D converter on) Wait[5] (A/D converter off) Stop[6] 25°C 0°C to +70°C (standard) –40°C to +85°C (extended)	 I_{DD}	 — — — — — —	 4.0 2.0 1.3 2 — —	 7.0 4.0 2.0 30 50 100	 mA mA mA µA µA µA
I/O ports high-z leakage current PA0:7, PB5:7, PC0:7, PD5, TCAP/PD7	I_{IL}	—	—	±10.0	µA
A/D ports hi-z leakage current PC3:7	I_{OZ}	—	—	±1.0	µA
Input current $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1, PD7/TCAP	I_{In}	—	—	±1.0	µA
Input pullup current PA0:7 (with pullup enabled)	I_{In}	175	385	750	µA
Capaitance Ports (as input or output) $\overline{RESET}$, $\overline{IRQ}$/V_{PP}	 C_{Out} C_{In}	 — —	 — —	 12 8	 pF

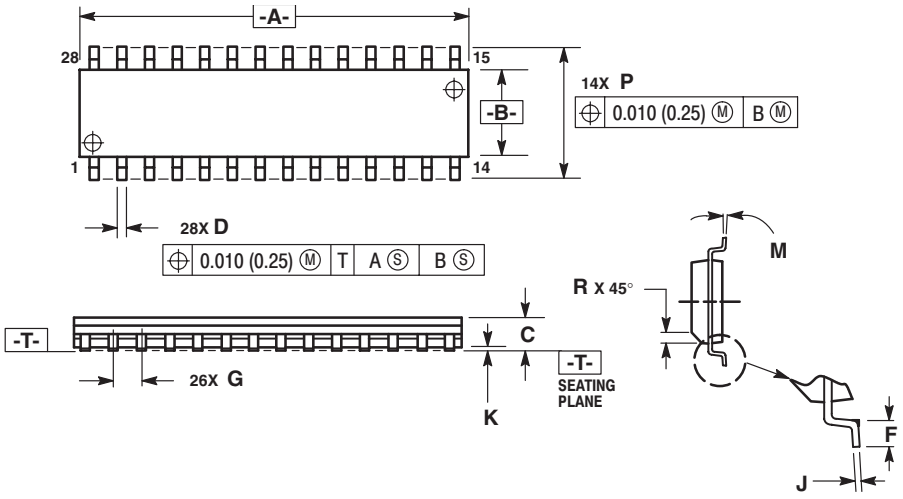
1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted. All values shown refelect pre-silicon estimates.
2. Typical values at midpoint of voltage range, 25°C only.
3. Run (Operating) I_{DD}, Wait I_{DD}: To be measured using external square wave clock source (f_{osc} = 4.2 MHz), all inputs 0.2 V from rail; no dc loads, less than 50 pF on all outputs, C_L = 20 pF on OSC2.
4. Wait, Stop I_{DD}: All ports configured as inputs, V_{IL} = 0.2 V, V_{IH} = V_{DD} –0.2 V.
5. Wait I_{DD} will be affected linearly by the OSC2 capacitance.
6. Stop I_{DD} to be measured with OSC1 = V_{SS}.

14.10 Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Frequency of operation Crystal option External clock option	f_{OSC}	— DC	4.2 4.2	MHz
Internal operating frequency Crystal ($f_{OSC} \div 2$) External clock ($f_{OSC} \div 2$)	f_{OP}	— DC	2.1 2.1	MHz
Cycle time	t_{CYC}	476	—	ns
Crystal oscillator startup time	t_{OXOV}	—	100	ms
Stop mode recovery startup time (crystal oscillator)	t_{ILCH}	—	100	ms
$\overline{\text{RESET}}$ pulse width	t_{RL}	1.5	—	t_{CYC}
Interrupt pulse width low (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period[2]	t_{ILIL}	Note 2	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	200	—	ns
A/D On current stabilization time	t_{ADON}	Q	100	µs

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +125°C, unless otherwise noted
2. The minimum period, t_{ILIL}, should not be less than the number of cycle times it takes to execute the interrupt service routine plus 19 t_{CYC}.

15.3 Small Outline Integrated Circuit Package (Case 751F)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029