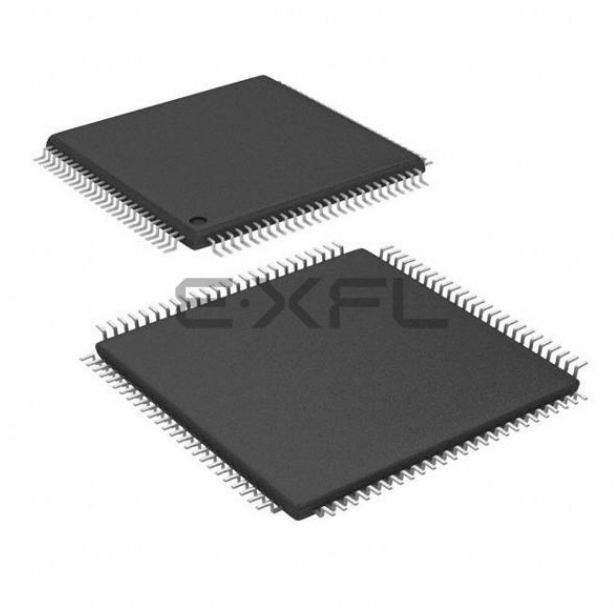

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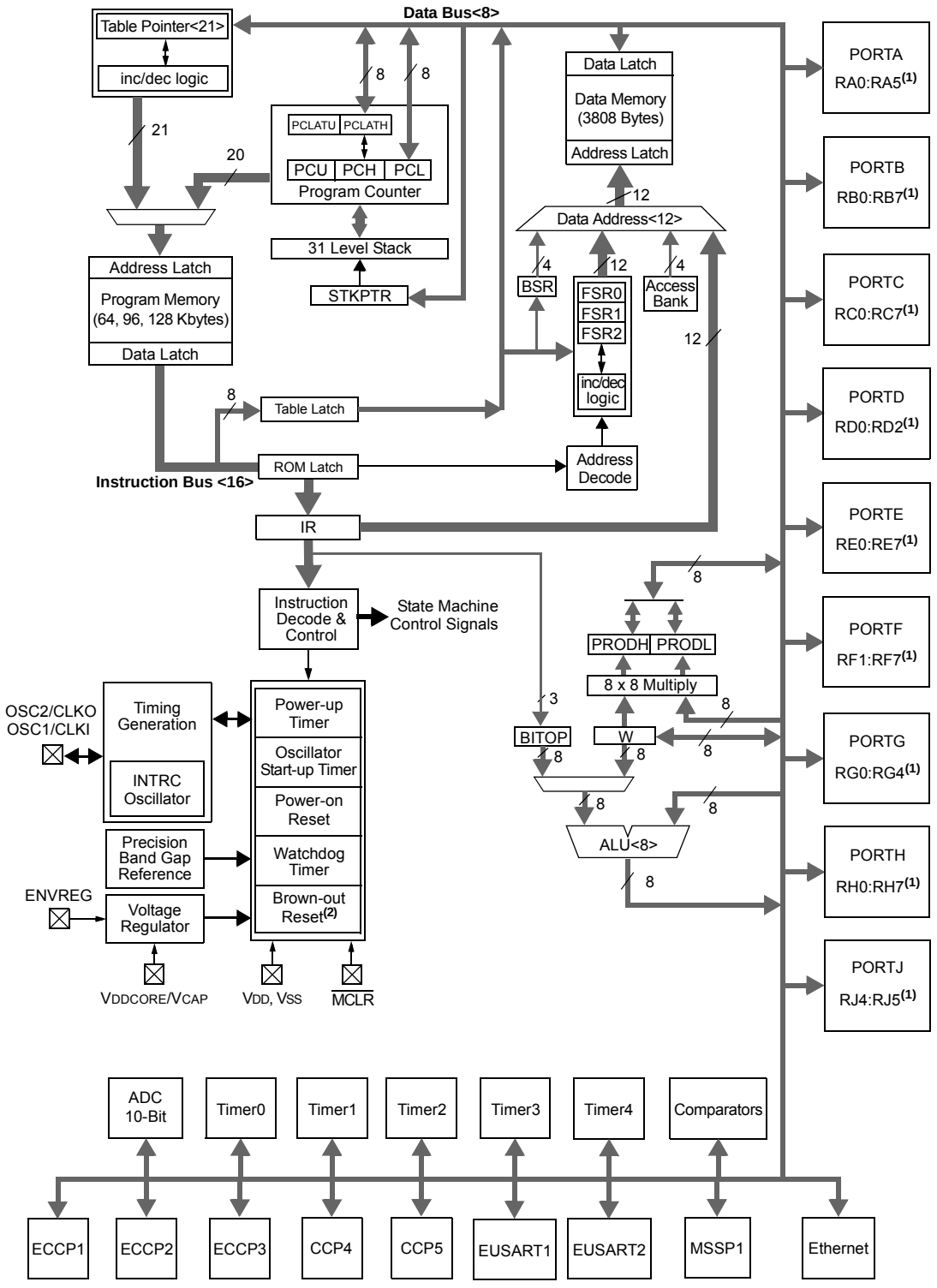
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	41.667MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	70
Program Memory Size	96KB (48K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3808 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f96j65t-i-pf

FIGURE 1-2: PIC18F86J60/86J65/87J60 (80-PIN) BLOCK DIAGRAM



Note 1: See Table 1-5 for I/O port pin descriptions.

2: BOR functionality is provided when the on-board voltage regulator is enabled.

TABLE 1-6: PIC18F96J60/96J65/97J60 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTJ is a bidirectional I/O port.
RJ0/ALE	49			
RJ0		I/O	ST	Digital I/O.
ALE		O	—	External memory address latch enable.
RJ1/$\overline{OE}$	50			
RJ1		I/O	ST	Digital I/O.
$\overline{OE}$		O	—	External memory output enable.
RJ2/$\overline{WRL}$	66			
RJ2		I/O	ST	Digital I/O.
$\overline{WRL}$		O	—	External memory write low control.
RJ3/$\overline{WRH}$	61			
RJ3		I/O	ST	Digital I/O.
$\overline{WRH}$		O	—	External memory write high control.
RJ4/BA0	47			
RJ4		I/O	ST	Digital I/O.
BA0		O	—	External Memory Byte Address 0 control.
RJ5/$\overline{CE}$	48			
RJ5		I/O	ST	Digital I/O
$\overline{CE}$		O	—	External memory chip enable control.
RJ6/$\overline{LB}$	58			
RJ6		I/O	ST	Digital I/O.
$\overline{LB}$		O	—	External memory low byte control.
RJ7/$\overline{UB}$	39			
RJ7		I/O	ST	Digital I/O.
$\overline{UB}$		O	—	External memory high byte control.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD})

Note 1: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared (Extended Microcontroller mode).

2: Default assignment for ECCP2/P2A for all devices in all operating modes (CCP2MX Configuration bit is set).

3: Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

4: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared (Microcontroller mode).

5: Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

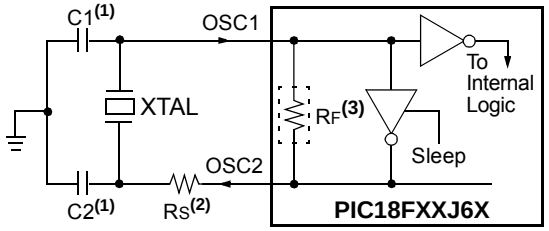
3.3 Crystal Oscillator/Ceramic Resonators (HS Modes)

In HS or HSPLL Oscillator modes, a crystal is connected to the OSC1 and OSC2 pins to establish oscillation. Figure 3-2 shows the pin connections.

The oscillator design requires the use of a crystal that is rated for parallel resonant operation.

Note:	Use of a crystal rated for series resonant operation may give a frequency out of the crystal manufacturer's specifications.

FIGURE 3-2: CRYSTAL OSCILLATOR OPERATION (HS OR HSPLL CONFIGURATION)



Note 1: See Table 3-1 for initial values of C1 and C2.

2: A series resistor (RS) may be required for crystals with a low drive specification.

3: RF varies with the oscillator mode chosen.

TABLE 3-1: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Crystal Freq.	Typical Capacitor Values Tested:	
		C1	C2
HS	25 MHz	33 pF	33 pF

Capacitor values are for design guidance only.

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application. Refer to the following application notes for oscillator specific information:

- *AN588, "PIC® Microcontroller Oscillator Design Guide"*
- *AN826, "Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices"*
- *AN849, "Basic PIC® Oscillator Design"*
- *AN943, "Practical PIC® Oscillator Analysis and Design"*
- *AN949, "Making Your Oscillator Work"*

See the notes following this table for additional information.

Note 1: Higher capacitance increases the stability of the oscillator but also increases the start-up time.

2: Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

3: Rs may be required to avoid overdriving crystals with low drive level specifications.

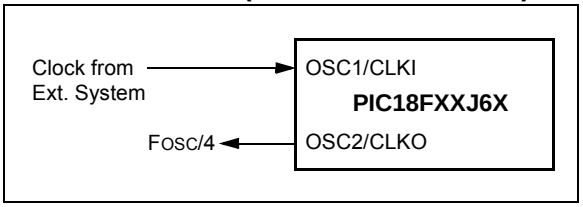
4: Always verify oscillator performance over the VDD and temperature range that is expected for the application.

3.4 External Clock Input (EC Modes)

The EC and ECPLL Oscillator modes require an external clock source to be connected to the OSC1 pin. There is no oscillator start-up time required after a Power-on Reset or after an exit from Sleep mode.

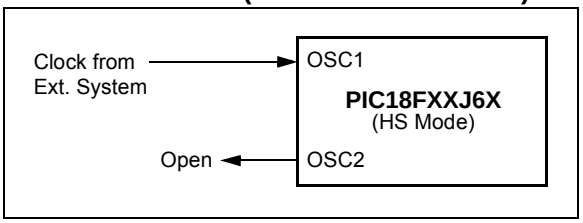
In the EC Oscillator mode, the oscillator frequency, divided by 4, is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic. Figure 3-3 shows the pin connections for the EC Oscillator mode.

FIGURE 3-3: EXTERNAL CLOCK INPUT OPERATION (EC CONFIGURATION)



An external clock source may also be connected to the OSC1 pin in the HS mode, as shown in Figure 3-4. In this configuration, the OSC2 pin is left open. Current consumption in this configuration will be somewhat higher than EC mode, as the internal oscillator's feedback circuitry will be enabled (in EC mode, the feedback circuit is disabled).

FIGURE 3-4: EXTERNAL CLOCK INPUT OPERATION (HS CONFIGURATION)



5.0 RESET

The PIC18F97J60 family of devices differentiates between various kinds of Reset:

a) MCLR Reset during normal operation
b) MCLR Reset during power-managed modes
c) Power-on Reset (POR)
d) Brown-out Reset (BOR)
e) Configuration Mismatch (CM)
f) RESET Instruction
g) Stack Full Reset
h) Stack Underflow Reset
i) Watchdog Timer (WDT) Reset during execution

This section discusses Resets generated by hard events (MCLR), power events (POR and BOR) and Configuration Mismatches (CM). It also covers the operation of the various start-up timers. Stack Reset events are covered in **Section 6.1.6.4 "Stack Full and Underflow Resets"**. WDT Resets are covered in **Section 25.2 "Watchdog Timer (WDT)"**.

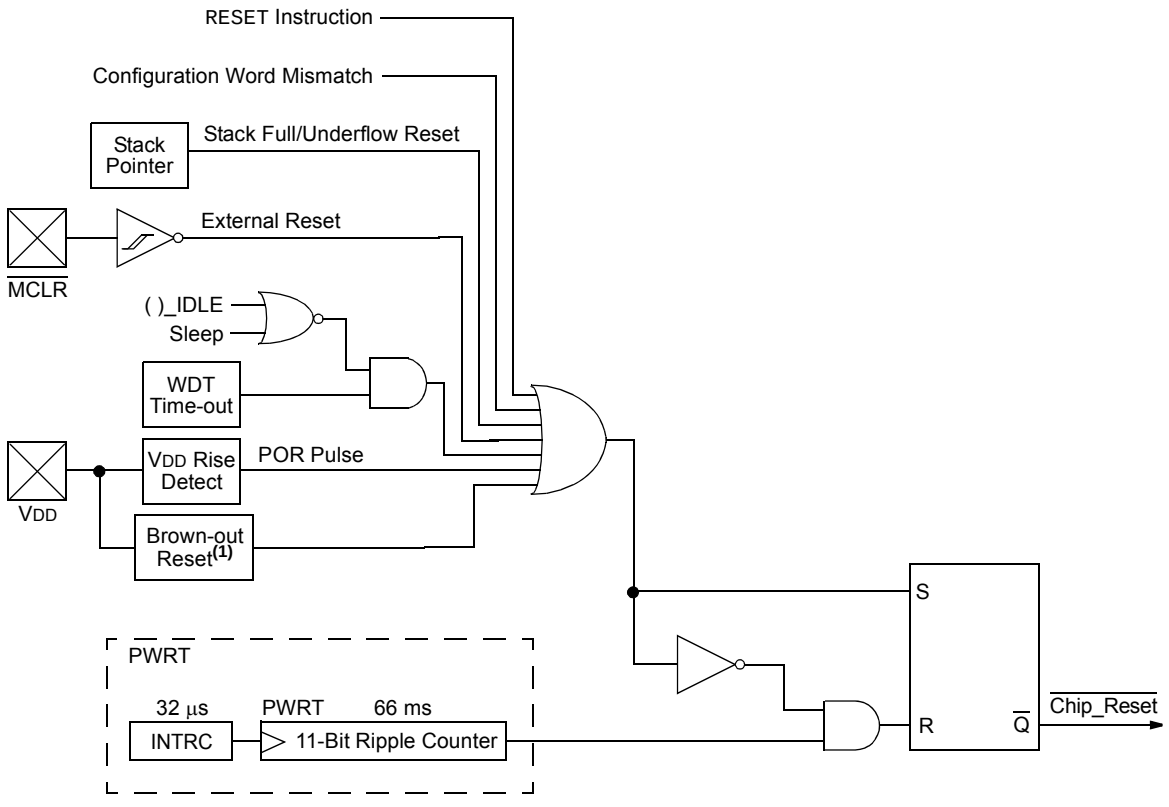
A simplified block diagram of the on-chip Reset circuit is shown in Figure 5-1.

5.1 RCON Register

Device Reset events are tracked through the RCON register (Register 5-1). The lower six bits of the register indicate that a specific Reset event has occurred. In most cases, these bits can only be set by the event and must be cleared by the application after the event. The state of these flag bits, taken together, can be read to indicate the type of Reset that just occurred. This is described in more detail in **Section 5.7 "Reset State of Registers"**.

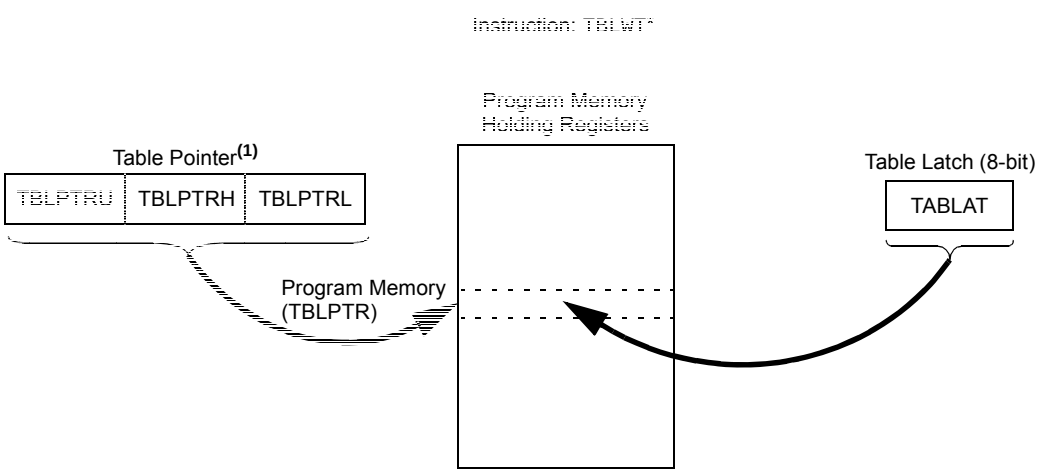
The RCON register also has a control bit for setting interrupt priority (IPEN). Interrupt priority is discussed in **Section 10.0 "Interrupts"**.

FIGURE 5-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: The ENVREG pin must be tied high to enable Brown-out Reset. The Brown-out Reset is provided by the on-chip voltage regulator when there is insufficient source voltage to maintain regulation.

FIGURE 7-2: TABLE WRITE OPERATION



Note 1: The Table Pointer actually points to one of 64 holding registers, the address of which is determined by TBLPTRL <5:0>. The process for physically writing data to the program memory array is discussed in Section 7.5 "Writing to Flash Program Memory".

7.2 Control Registers

Several control registers are used in conjunction with the TBLRD and TBLWT instructions. These include the:

- EECON1 register
- EECON2 register
- TABLAT register
- TBLPTR registers

7.2.1 EECON1 AND EECON2 REGISTERS

The EECON1 register (Register 7-1) is the control register for memory accesses. The EECON2 register is not a physical register; it is used exclusively in the memory write and erase sequences. Reading EECON2 will read all '0's.

The FREE bit, when set, will allow a program memory erase operation. When FREE is set, the erase operation is initiated on the next WR command. When FREE is clear, only writes are enabled.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set in hardware when the WR bit is set, and cleared when the internal programming timer expires and the write operation is complete.

Note:	During normal operation, the WRERR is read as '1'. This can indicate that a write operation was prematurely terminated by a Reset, or a write operation was attempted improperly.

The WR control bit initiates write operations. The bit cannot be cleared, only set, in software; it is cleared in hardware at the completion of the write operation.

EXAMPLE 7-3: WRITING TO FLASH PROGRAM MEMORY

```
                    MOVLW   CODE_ADDR_UPPER    ; Load TBLPTR with the base
                    MOVWF   TBLPTRU            ; address of the memory block
                    MOVLW   CODE_ADDR_HIGH
                    MOVWF   TBLPTRH
                    MOVLW   CODE_ADDR_LOW
                    MOVWF   TBLPTRL
ERASE_BLOCK
                    BSF     EECON1, WREN       ; enable write to memory
                    BSF     EECON1, FREE       ; enable Row Erase operation
                    BCF     INTCON, GIE        ; disable interrupts
                    MOVLW   55h
                    MOVWF   EECON2             ; write 55h
                    MOVLW   0AAh
                    MOVWF   EECON2             ; write 0AAh
                    BSF     EECON1, WR         ; start erase (CPU stall)
                    BSF     INTCON, GIE        ; re-enable interrupts
                    MOVLW   D'16'
                    MOVWF   WRITE_COUNTER      ; Need to write 16 blocks of 64 to write
                                               ; one erase block of 1024
RESTART_BUFFER
                    MOVLW   D'64'
                    MOVWF   COUNTER
                    MOVLW   BUFFER_ADDR_HIGH   ; point to buffer
                    MOVWF   FSR0H
                    MOVLW   BUFFER_ADDR_LOW
                    MOVWF   FSR0L
FILL_BUFFER
                    ...                        ; read the new data from I2C, SPI,
                                               ; PSP, USART, etc.
WRITE_BUFFER
                    MOVLW   D’64               ; number of bytes in holding register
                    MOVWF   COUNTER
WRITE_BYTE_TO_HREGS
                    MOVFF   POSTINC0, WREG     ; get low byte of buffer data
                    MOVWF   TABLAT             ; present data to table latch
                    TBLWT+*                    ; write data, perform a short write
                                               ; to internal TBLWT holding register.
                    DECFSZ  COUNTER            ; loop until buffers are full
                    BRA     WRITE_BYTE_TO_HREGS
PROGRAM_MEMORY
                    BSF     EECON1, WREN       ; enable write to memory
                    BCF     INTCON, GIE        ; disable interrupts
                    MOVLW   55h
   Required         MOVWF   EECON2             ; write 55h
   Sequence         MOVLW   0AAh
                    MOVWF   EECON2             ; write 0AAh
                    BSF     EECON1, WR         ; start program (CPU stall)
                    BSF     INTCON, GIE        ; re-enable interrupts
                    BCF     EECON1, WREN       ; disable write to memory

                    DECFSZ  WRITE_COUNTER      ; done with one write cycle
                    BRA     RESTART_BUFFER     ; if not done replacing the erase block
```

10.5 RCON Register

The RCON register contains bits used to determine the cause of the last Reset or wake-up from Idle or Sleep modes. RCON also contains the bit that enables interrupt priorities (IPEN).

REGISTER 10-13: RCON: RESET CONTROL REGISTER

R/W-0	U-0	R/W-1	R/W-1	R-1	R-1	R/W-0	R/W-0
IPEN	—	$\overline{CM}$	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **IPEN:** Interrupt Priority Enable bit
1 = Enable priority levels on interrupts
0 = Disable priority levels on interrupts (PIC16CXXX Compatibility mode)

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **$\overline{CM}$:** Configuration Mismatch Flag bit
For details of bit operation, see Register 5-1.

bit 4 **$\overline{RI}$:** RESET Instruction Flag bit
For details of bit operation, see Register 5-1.

bit 3 **$\overline{TO}$:** Watchdog Timer Time-out Flag bit
For details of bit operation, see Register 5-1.

bit 2 **$\overline{PD}$:** Power-Down Detection Flag bit
For details of bit operation, see Register 5-1.

bit 1 **$\overline{POR}$:** Power-on Reset Status bit(2)
For details of bit operation, see Register 5-1.

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit
For details of bit operation, see Register 5-1.

TABLE 11-9: PORTD FUNCTIONS (CONTINUED)

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RD5/AD5/ PSP5/SDI2/ SDA2(1)	RD5(1)	0	O	DIG	LATD<5> data output.
		1	I	ST	PORTD<5> data input; weak pull-up when RDPU bit is set.
	AD5(1)	x	O	DIG	External memory interface, Address/Data Bit 5 output.(2)
		x	I	TTL	External memory interface, Data Bit 5 input.(2)
	PSP5(1)	x	O	DIG	PSP read output data (LATD<5>); takes priority over port data.
		x	I	TTL	PSP write data input.
	SDI2(1)	1	I	ST	SPI data input (MSSP2 module).
	SDA2(1)	1	O	DIG	I^2C™ data output (MSSP2 module); takes priority over port data.
		1	I	ST	I^2C data input (MSSP2 module); input type depends on module setting.
RD6/AD6/ PSP6/SCK2/ SCL2(1)	RD6(1)	0	O	DIG	LATD<6> data output.
		1	I	ST	PORTD<6> data input; weak pull-up when RDPU bit is set.
	AD6(1)	x	O	DIG-3	External memory interface, Address/Data Bit 6 output.(2)
		x	I	TTL	External memory interface, Data Bit 6 input.(2)
	PSP6(1)	x	O	DIG	PSP read output data (LATD<6>); takes priority over port data.
		x	I	TTL	PSP write data input.
	SCK2(1)	0	O	DIG	SPI clock output (MSSP2 module); takes priority over port data.
		1	I	ST	SPI clock input (MSSP2 module).
	SCL2(1)	0	O	DIG	I^2C clock output (MSSP2 module); takes priority over port data.
		1	I	ST	I^2C clock input (MSSP2 module); input type depends on module setting.
RD7/AD7/ PSP7/$\overline{SS2}$(1)	RD7(1)	0	O	DIG	LATD<7> data output.
		1	I	ST	PORTD<7> data input; weak pull-up when RDPU bit is set.
	AD7(1)	x	O	DIG	External memory interface, Address/Data Bit 7 output.(2)
		x	I	TTL	External memory interface, Data Bit 7 input.(2)
	PSP7(1)	x	O	DIG	PSP read output data (LATD<7>); takes priority over port data.
		x	I	TTL	PSP write data input.
	$\overline{SS2}$(1)	x	I	TTL	Slave select input for MSSP2 module.

Legend: O = Output, I = Input, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

Note 1: These features or port pins are implemented only on 100-pin devices.

2: External memory interface I/O takes priority over all other digital and PSP I/O.

3: These features are implemented on this pin only on 64-pin devices; for all other devices, they are multiplexed with RE6/RH7 (P1B), RG0 (ECCP3/P3A) or RG3 (CCP4/P3D).

TABLE 11-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
PORTD	RD7(1)	RD6(1)	RD5(1)	RD4(1)	RD3(1)	RD2	RD1	RD0	72
LATD	LATD7(1)	LATD6(1)	LATD5(1)	LATD4(1)	LATD3(1)	LATD2	LATD1	LATD0	72
TRISD	TRISD7(1)	TRISD6(1)	TRISD5(1)	TRISD4(1)	TRISD3(1)	TRISD2	TRISD1	TRISD0	71
LATA	RDPU	REPU	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	72

Legend: Shaded cells are not used by PORTD.

Note 1: Unimplemented on 64-pin and 80-pin devices; read as '0'.

13.0 TIMER1 MODULE

The Timer1 timer/counter module incorporates these features:

- Software selectable operation as a 16-bit timer or counter
- Readable and writable 8-bit registers (TMR1H and TMR1L)
- Selectable clock source (internal or external) with device clock or Timer1 oscillator internal options
- Interrupt on overflow
- Reset on ECCP Special Event Trigger
- Device clock status flag (T1RUN)

A simplified block diagram of the Timer1 module is shown in Figure 13-1. A block diagram of the module's operation in Read/Write mode is shown in Figure 13-2.

The module incorporates its own low-power oscillator to provide an additional clocking option. The Timer1 oscillator can also be used as a low-power clock source for the microcontroller in power-managed operation.

Timer1 can also be used to provide Real-Time Clock (RTC) functionality to applications with only a minimal addition of external components and code overhead.

Timer1 is controlled through the T1CON Control register (Register 13-1). It also contains the Timer1 Oscillator Enable bit (T1OSCEN). Timer1 can be enabled or disabled by setting or clearing control bit, TMR1ON (T1CON<0>).

REGISTER 13-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **RD16:** 16-Bit Read/Write Mode Enable bit
1 = Enables register read/write of Timer1 in one 16-bit operation
0 = Enables register read/write of Timer1 in two 8-bit operations

bit 6 **T1RUN:** Timer1 System Clock Status bit
1 = Device clock is derived from Timer1 oscillator
0 = Device clock is derived from another source

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 **T1OSCEN:** Timer1 Oscillator Enable bit
1 = Timer1 oscillator is enabled
0 = Timer1 oscillator is shut off
The oscillator inverter and feedback resistor are turned off to eliminate power drain.

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Select bit
When TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
When TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from RC0/T1OSO/T13CKI pin (on the rising edge)
0 = Internal clock (FOSC/4)

bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

18.4 Enhanced PWM Mode

The Enhanced PWM mode provides additional PWM output options for a broader range of control applications. The module is a backward compatible version of the standard CCPx modules and offers up to four outputs, designated PxA through PxD. Users are also able to select the polarity of the signal (either active-high or active-low). The module's output mode and polarity are configured by setting the PxM<1:0> and CCPxM<3:0> bits of the CCPxCON register (CCPxCON<7:6> and <3:0>, respectively).

For the sake of clarity, Enhanced PWM mode operation is described generically throughout this section with respect to ECCP1 and TMR2 modules. Control register names are presented in terms of ECCP1. All three Enhanced modules, as well as the two timer resources, can be used interchangeably and function identically. TMR2 or TMR4 can be selected for PWM operation by selecting the proper bits in T3CON.

Figure 18-1 shows a simplified block diagram of PWM operation. All control registers are double-buffered and are loaded at the beginning of a new PWM cycle (the period boundary when Timer2 resets) in order to prevent glitches on any of the outputs. The exception is the ECCP1 Dead-Band Delay register, ECCP1DEL, which is loaded at either the duty cycle boundary or the boundary period (whichever comes first). Because of the buffering, the module waits until the assigned timer resets instead of starting immediately. This means that Enhanced PWM waveforms do not exactly match the standard PWM waveforms, but are instead, offset by one full instruction cycle (4 TOSC).

As before, the user must manually configure the appropriate TRIS bits for output.

18.4.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following equation:

EQUATION 18-1:

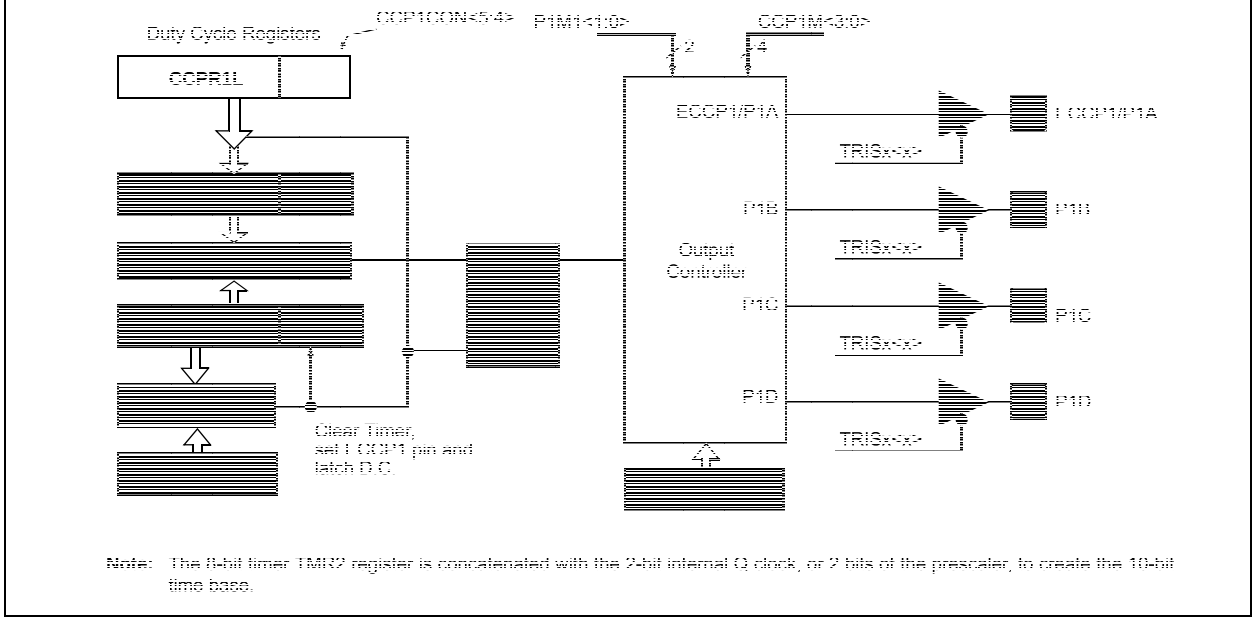
$$\text{PWM Period} = [(PR2) + 1] \cdot 4 \cdot T_{OSC} \cdot (\text{TMR2 Prescale Value})$$

PWM frequency is defined as 1/[PWM period]. When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The ECCP1 pin is set (if PWM duty cycle = 0%, the ECCP1 pin will not be set)
- The PWM duty cycle is copied from CCPR1L into CCPR1H

Note:	The Timer2 postscaler (see **Section 14.0 "Timer2 Module"**) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

FIGURE 18-1: SIMPLIFIED BLOCK DIAGRAM OF THE ENHANCED PWM MODULE



Note: The 8-bit timer TMR2 register is concatenated with the 2-bit internal Q clock, or 2 bits of the prescaler, to create the 10-bit time base.

19.1 Physical Interfaces and External Connections

19.1.1 SIGNAL AND POWER INTERFACES

PIC18F97J60 family devices all provide a dedicated 4-pin signal interface for the Ethernet module. No other microcontroller or peripheral functions are multiplexed with these pins, so potential device configuration conflicts do not need to be considered. The pins are:

- TPIN+: Differential plus twisted-pair input
- TPIN-: Differential minus twisted-pair input
- TPOUT+: Differential plus twisted-pair output
- TPOUT-: Differential minus twisted-pair output

No provisions are made for providing or receiving digital Ethernet data from an external Ethernet PHY.

In addition to the signal connections, the Ethernet module has its own independent voltage source and ground connections for the PHY module. Separate connections are provided for the receiver (V_{DDRX} and V_{SSRX}), the transmitter (V_{DDTX} and V_{SSTX}) and the transmitter's internal PLL (V_{DDPLL} and V_{SSPLL}). Although the voltage requirements are the same as V_{DD} and V_{SS} for the microcontroller, the pins are not internally connected. For the Ethernet module to operate properly, supply voltage and ground must be connected to these pins. All of the microcontroller's power and ground supply pins should be externally connected to the same power source or ground node, with no inductors or other filter components between the microcontroller and Ethernet module's V_{DD} pins.

Besides the independent voltage connections, the PHY module has a separate bias current input pin, RBIAS. A bias current, derived from an external resistor, must be applied to RBIAS for proper transceiver operation.

19.1.2 LED CONFIGURATION

The PHY module provides separate outputs to drive the standard Ethernet indicators, LEDA and LEDB. The LED outputs are multiplexed with PORTA pins, RA0 and RA1. Their use as LED outputs is enabled by setting the Configuration bit, ETHLED (Register 25-6, CONFIG3H<2>). When configured as LED outputs, RA0/LEDA and RA1/LEDB have sufficient drive capacity (up to 25 mA) to directly power the LEDs. The pins must always be configured to supply (source) current to the LEDs. Users must also configure the pins as outputs by clearing TRISA<1:0>.

The LEDs can be individually configured to automatically display link status, RX/TX activity, etc. A configurable stretch capability prolongs the LED blink duration for short events, such as a single packet transmit, allowing human perception. The options are controlled by the PHLCON register (Register 19-13). Typical values for blink stretch are listed in Table 19-1.

TABLE 19-1: LED BLINK STRETCH LENGTH

Stretch Length	Typical Stretch (ms)
T_{NSTRCH} (normal)	40
T_{MSTRCH} (medium)	70
T_{LSTRCH} (long)	140

19.1.3 OSCILLATOR REQUIREMENTS

The Ethernet module is designed to operate at 25 MHz. This is provided by the primary microcontroller clock, either with a 25 MHz crystal connected to the OSC1 and OSC2 pins or an external clock source connected to the OSC1 pin. No provision is made to clock the module from a different source.

To maintain the required clock frequency, the microcontroller can operate only from the primary oscillator source (PRI_RUN or PRI_IDLE modes) while the Ethernet module is enabled. Using any other power-managed mode will require that the Ethernet module be disabled.

19.1.3.1 Start-up Timer

The Ethernet module contains a start-up timer, independent of the microcontroller's OST, to ensure that the PHY module's PLL has stabilized before operation. Clearing the module enable bit, ETHEN (ECON2<5>), clears the PHYRDY status bit (ESTAT<0>). Setting the ETHEN bit causes this start-up timer to start counting. When the timer expires, after 1 ms, the PHYRDY bit will be automatically set.

After enabling the module by setting the ETHEN bit, the application software should always poll PHYRDY to determine when normal Ethernet operation can begin.

19.5 Transmitting and Receiving Data

The Ethernet protocol (IEEE Standard 802.3) provides an extremely detailed description of the 10 Mbps, frame-based serial communications system. Before discussing the actual use of the Ethernet module, a brief review of the structure of a typical Ethernet data frame may be appropriate. It is assumed that users already have some familiarity with IEEE 802.3. Those requiring more information should refer to the official standard, or other Ethernet reference texts, for a more comprehensive explanation.

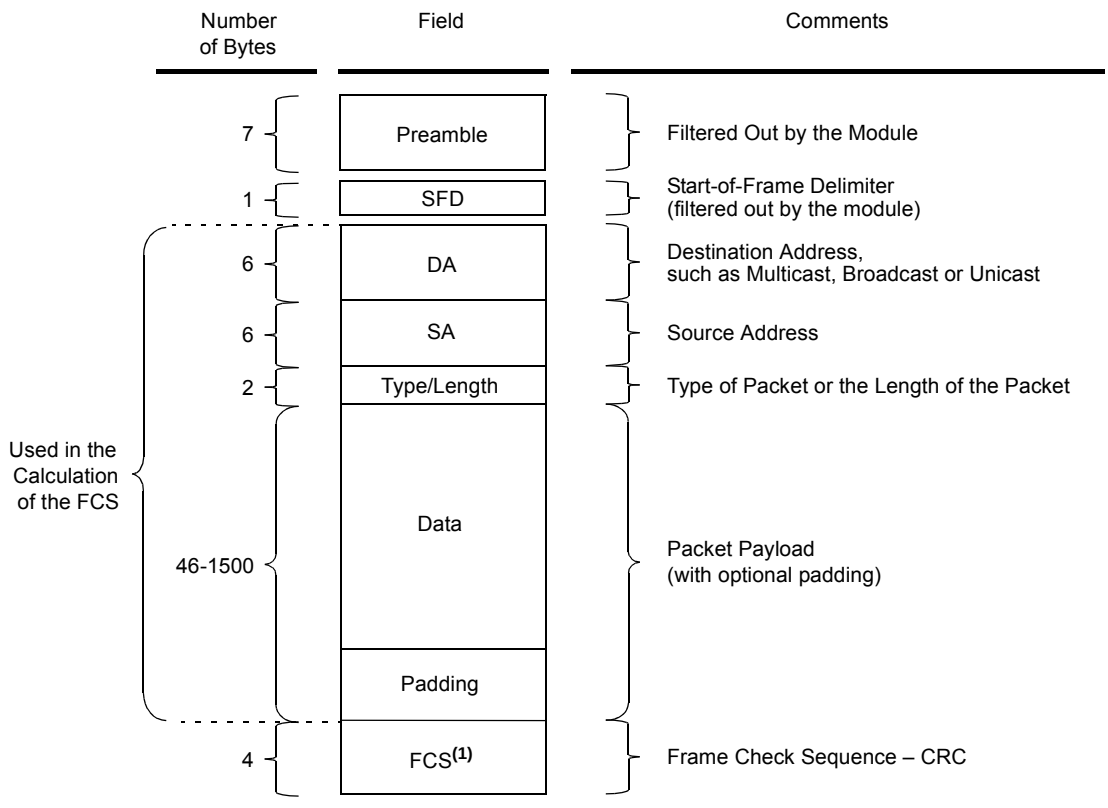
19.5.1 PACKET FORMAT

Normal IEEE 802.3 compliant Ethernet frames are between 64 and 1518 bytes long. They are made up of five or six different fields: a destination MAC address, a source MAC address, a type/length field, data payload, an optional padding field and a Cyclic Redundancy Check (CRC). Additionally, when transmitted on the Ethernet medium, a 7-byte preamble field and Start-of-Frame (SOF) delimiter byte are appended to the beginning of the Ethernet packet. Thus, traffic seen on the twisted-pair cabling will appear as shown in Figure 19-8.

19.5.1.1 Preamble/Start-of-Frame Delimiter

When transmitting and receiving data with the Ethernet module, the preamble and Start-of-Frame delimiter bytes are automatically generated, or stripped from the packets, when they are transmitted or received. It can also automatically generate CRC fields and padding as needed on transmission, and verify CRC data on reception. The user application does not need to create or process these fields, or manually verify CRC data. However, the padding and CRC fields are written into the receive buffer when packets arrive, so they may be evaluated by the user application as needed.

FIGURE 19-8: ETHERNET PACKET FORMAT



Note 1: The FCS is transmitted starting with bit 31 and ending with bit 0.

19.8.5 PATTERN MATCH FILTER

The Pattern Match filter selects up to 64 bytes from the incoming packet and calculates an IP checksum of the bytes. The checksum is then compared to the EPMCS registers. The packet meets the Pattern Match filter criteria if the calculated checksum matches the EPMCS registers. The Pattern Match filter may be useful for filtering packets which have expected data inside them.

To use the Pattern Match filter, the application must program the Pattern Match offset (EPMOH:EPMOL), all of the Pattern Match mask bytes (EPMM0:EPMM7) and the Pattern Match Checksum register pair (EPMCSH:EPMCSL). The Pattern Match offset should be loaded with the offset from the beginning of the destination address field to the 64-byte window which will be used for the checksum computation. Within the 64-byte window, each individual byte can be selectively included or excluded from the checksum computation by setting or clearing the respective bit in the Pattern Match mask. If a packet is received which would cause the 64-byte window to extend past the end of the CRC, the filter criteria will immediately not be met, even if the corresponding mask bits are all '0'.

Note:	In all cases, the value of the Pattern Match offset must be even for proper operation. Programming the EMPO register pair with an odd value will cause unpredictable results.

The Pattern Match Checksum registers should be programmed to the checksum which is expected for the selected bytes. The checksum is calculated in the same manner that the DMA module calculates checksums (see **Section 19.9.2 "Checksum Calculations"**). Data bytes which have corresponding mask bits programmed to '0' are completely removed for purposes of calculating the checksum, as opposed to treating the data bytes as zero.

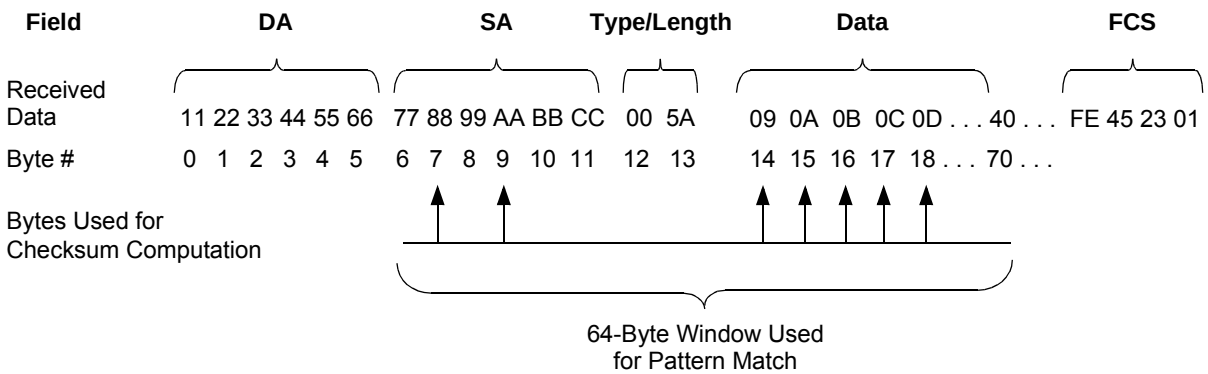
As an example, if the application wished to filter all packets having a particular source MAC address of 00-04-A3-FF-FF-FF, it could program the Pattern Match offset to 0000h and then set bits 6 and 7 of EPMM0 and bits 0, 1, 2 and 3 of EPMM1 (assuming all other mask bits are '0'). The proper checksum to program into the EPMCS registers would be 5BFCh. As an alternative configuration, it could program the offset to 0006h and set bits 0, 1, 2, 3, 4 and 5 of EPMM0. The checksum would still be 5BFCh. However, the second case would be less desirable as packets less than 70 bytes long could never meet the Pattern Match criteria, even if they would generate the proper checksum given the mask configuration.

Another example of a Pattern Match filter is illustrated in Figure 19-15.

FIGURE 19-15: SAMPLE PATTERN MATCH FORMAT

Input Configuration:

EMPOH:EPMOL = 0006h
EPMM7:EPMM0 = 0000000000001F0Ah
EPMCSH:EPMCSL = 563Fh



Values Used for Checksum Computation = {88h, AAh, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 00h}
(00h padding byte added by hardware)

Note: Received data is shown in hexadecimal. Byte numbers are shown in decimal format.

20.4.10 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address or the other half of a 10-bit address is accomplished by simply writing a value to the SSPxBUF register. This action will set the Buffer Full flag bit, BF, and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDAx pin after the falling edge of SCLx is asserted (see data hold time specification Parameter 106). SCLx is held low for one Baud Rate Generator rollover count (TBRG). Data should be valid before SCLx is released high (see data setup time specification Parameter 107). When the SCLx pin is released high, it is held that way for TBRG. The data on the SDAx pin must remain stable for that duration and some hold time after the next falling edge of SCLx. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDAx. This allows the slave device being addressed to respond with an $\overline{ACK}$ bit during the ninth bit time if an address match occurred, or if data was received properly. The status of $\overline{ACK}$ is written into the ACKDT bit on the falling edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge Status bit, ACKSTAT, is cleared; if not, the bit is set. After the ninth clock, the SSPxIF bit is set and the master clock (Baud Rate Generator) is suspended until the next data byte is loaded into the SSPxBUF, leaving SCLx low and SDAx unchanged (Figure 20-23).

After the write to the SSPxBUF, each bit of the address will be shifted out on the falling edge of SCLx until all seven address bits and the R/$\overline{W}$ bit are completed. On the falling edge of the eighth clock, the master will deassert the SDAx pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDAx pin to see if the address was recognized by a slave. The status of the $\overline{ACK}$ bit is loaded into the ACKSTAT status bit (SSPxCON2<6>). Following the falling edge of the ninth clock transmission of the address, the SSPxIF is set, the BF flag is cleared and the Baud Rate Generator is turned off until another write to the SSPxBUF takes place, holding SCLx low and allowing SDAx to float.

20.4.10.1 BF Status Flag

In Transmit mode, the BF bit (SSPxSTAT<0>) is set when the CPU writes to SSPxBUF, and is cleared when all 8 bits are shifted out.

20.4.10.2 WCOL Status Flag

If the user writes to the SSPxBUF when a transmit is already in progress (i.e., SSPxSR is still shifting out a data byte), the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur) after 2 TCY after the SSPxBUF write. If SSPxBUF is rewritten within 2 TCY, the WCOL bit is set and SSPxBUF is updated. This may result in a corrupted transfer.

The user should verify that the WCOL is clear after each write to SSPxBUF to ensure the transfer is correct. In all cases, WCOL must be cleared in software.

20.4.10.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit (SSPxCON2<6>) is cleared when the slave has sent an Acknowledge ($\overline{ACK}$ = 0) and is set when the slave does not Acknowledge ($\overline{ACK}$ = 1). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

20.4.11 I²C MASTER MODE RECEPTION

Master mode reception is enabled by programming the Receive Enable bit, RCEN (SSPxCON2<3>).

Note:	The MSSP module must be in an Idle state before the RCEN bit is set or the RCEN bit will be disregarded.

The Baud Rate Generator begins counting and on each rollover. The state of the SCLx pin changes (high-to-low/low-to-high) and data is shifted into the SSPxSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPxSR are loaded into the SSPxBUF, the BF flag bit is set, the SSPxIF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCLx low. The MSSP is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable bit, ACKEN (SSPxCON2<4>).

20.4.11.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPxBUF from SSPxSR. It is cleared when the SSPxBUF register is read.

20.4.11.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when 8 bits are received into the SSPxSR and the BF flag bit is already set from a previous reception.

20.4.11.3 WCOL Status Flag

If the user writes the SSPxBUF when a receive is already in progress (i.e., SSPxSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write doesn't occur).

20.4.17.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

a) A low level is sampled on SDAx when SCLx goes from low level to high level.
b) SCLx goes low before SDAx is asserted low, indicating that another master is attempting to transmit a data '1'.

When the user deasserts SDAx and the pin is allowed to float high, the BRG is loaded with SSPxADD<6:0> and counts down to 0. The SCLx pin is then deasserted and when sampled high, the SDAx pin is sampled.

If SDAx is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', see Figure 20-31). If SDAx is sampled high, the BRG is reloaded and begins counting. If SDAx goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDAx at exactly the same time.

If SCLx goes from high-to-low before the BRG times out and SDAx has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition (see Figure 20-32).

If, at the end of the BRG time-out, both SCLx and SDAx are still high, the SDAx pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCLx pin, the SCLx pin is driven low and the Repeated Start condition is complete.

FIGURE 20-31: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

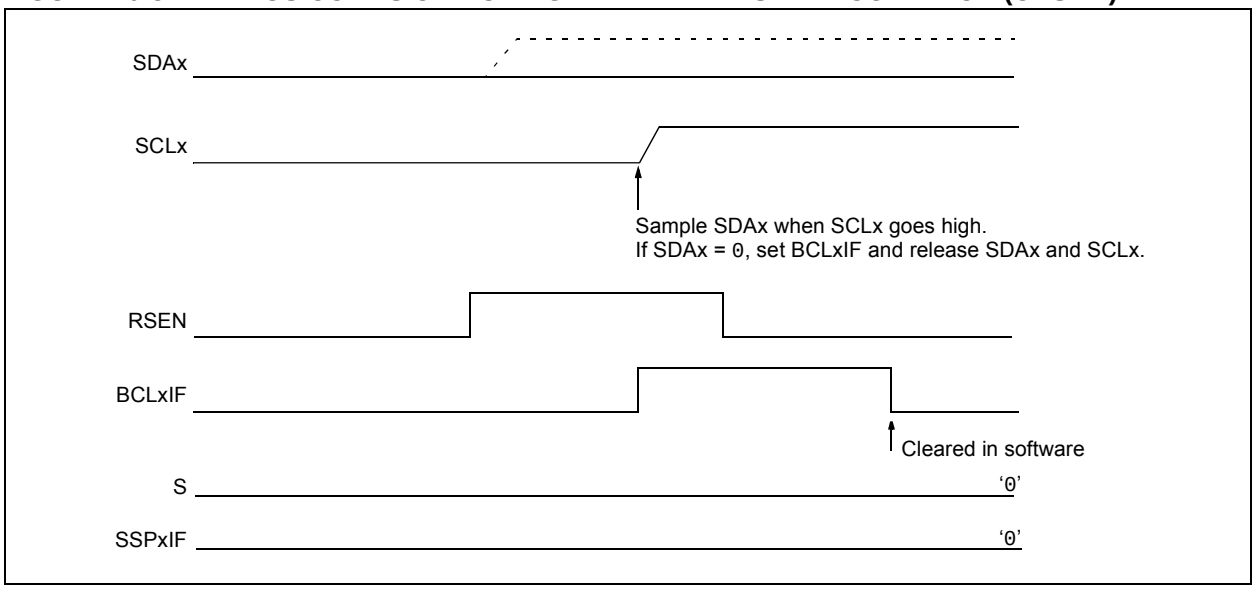


FIGURE 20-32: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)

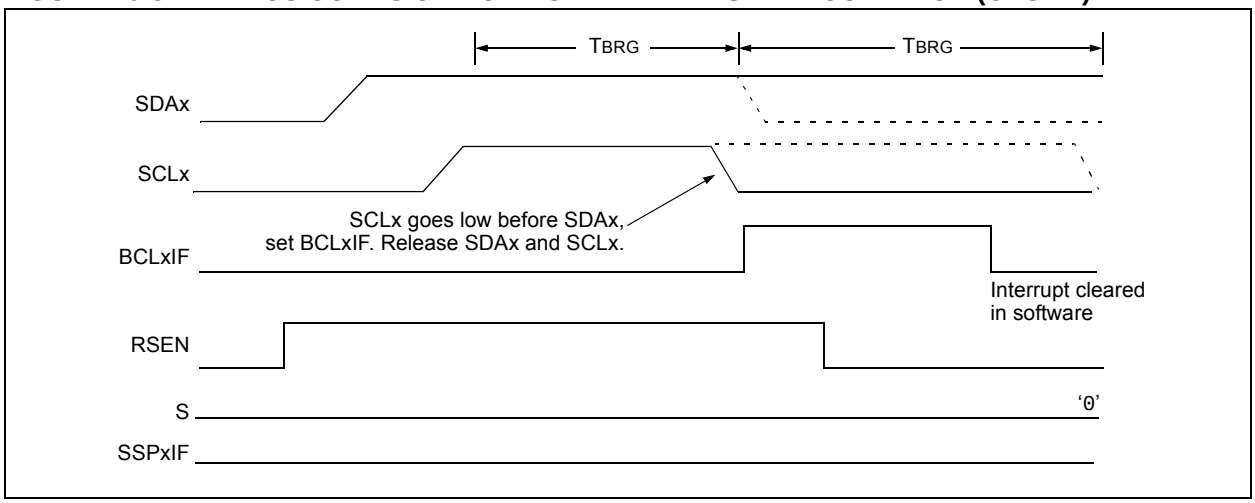


TABLE 21-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	69
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	71
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	71
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	71
PIR3	SSP2IF	BCL2IF	RC2IF	TX2IF(1)	TMR4IF	CCP5IF	CCP4IF	CCP3IF	71
PIE3	SSP2IE	BCL2IE	RC2IE	TX2IE(1)	TMR4IE	CCP5IE	CCP4IE	CCP3IE	71
IPR3	SSP2IP	BCL2IP	RC2IP	TX2IP(1)	TMR4IP	CCP5IP	CCP4IP	CCP3IP	71
RCSTAx	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	71
TXREGx	EUSARTx Transmit Register								71
TXSTAx	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	71
BAUDCONx	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN	72
SPBRGHx	EUSARTx Baud Rate Generator Register High Byte								72
SPBRGx	EUSARTx Baud Rate Generator Register Low Byte								72

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.

Note 1: These bits are only available in 80-pin and 100-pin devices; otherwise, they are unimplemented and read as '0'.

23.0 COMPARATOR MODULE

The analog comparator module contains two comparators that can be configured in a variety of ways. The inputs can be selected from the analog inputs, multiplexed with pins, RF1 through RF6, as well as the on-chip voltage reference (see **Section 24.0 "Comparator Voltage Reference Module"**). The digital outputs (normal or inverted) are available at the pin level and can also be read through the control register.

The CMCON register (Register 23-1) selects the comparator input and output configuration. Block diagrams of the various comparator configurations are shown in Figure 23-1.

REGISTER 23-1: CMCON: COMPARATOR CONTROL REGISTER

R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1
C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **C2OUT**: Comparator 2 Output bit
When C2INV = 0:
1 = C2 VIN+ > C2 VIN-
0 = C2 VIN+ < C2 VIN-
When C2INV = 1:
1 = C2 VIN+ < C2 VIN-
0 = C2 VIN+ > C2 VIN-

bit 6 **C1OUT**: Comparator 1 Output bit
When C1INV = 0:
1 = C1 VIN+ > C1 VIN-
0 = C1 VIN+ < C1 VIN-
When C1INV = 1:
1 = C1 VIN+ < C1 VIN-
0 = C1 VIN+ > C1 VIN-

bit 5 **C2INV**: Comparator 2 Output Inversion bit
1 = C2 output is inverted
0 = C2 output is not inverted

bit 4 **C1INV**: Comparator 1 Output Inversion bit
1 = C1 output is inverted
0 = C1 output is not inverted

bit 3 **CIS**: Comparator Input Switch bit
When CM<2:0> = 110:
1 = C1 VIN- connects to RF5/AN10/CVREF
C2 VIN- connects to RF3/AN8
0 = C1 VIN- connects to RF6/AN11
C2 VIN- connects to RA4/AN9

bit 2-0 **CM<2:0>**: Comparator Mode bits
Figure 23-1 shows the Comparator modes and the CM<2:0> bit settings.

RETURN **Return from Subroutine**

Syntax: RETURN {s}

Operands: s ∈ [0,1]

Operation: (TOS) → PC;
if s = 1,
(WS) → W,
(STATUSS) → STATUS,
(BSRS) → BSR,
PCLATU, PCLATH are unchanged

Status Affected: None

Encoding:

0000	0000	0001	001s

Description: Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the program counter. If 's'= 1, the contents of the shadow registers WS, STATUSS and BSRS are loaded into their corresponding registers W, STATUS and BSR. If 's' = 0, no update of these registers occurs (default).

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	Process Data	POP PC from stack
No operation	No operation	No operation	No operation

Example: RETURN

After Instruction:
PC = TOS

RLCF **Rotate Left f through Carry**

Syntax: RLCF f {,d {,a}}

Operands: 0 ≤ f ≤ 255
d ∈ [0,1]
a ∈ [0,1]

Operation: (f<n>) → dest<n + 1>,
(f<7>) → C,
(C) → dest<0>

Status Affected: C, N, Z

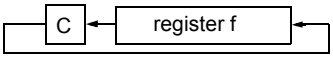
Encoding:

0011	01da	ffff	ffff

Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f' (default).

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See **Section 26.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.



Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: RLCF REG, 0, 0

Before Instruction
REG = 1110 0110
C = 0
After Instruction
REG = 1110 0110
W = 1100 1100
C = 1

MOVSS **Move Indexed to Indexed**

Syntax: MOVSS [z_s], [z_d]

Operands: $0 \le z_s \le 127$
$0 \le z_d \le 127$

Operation: ((FSR2) + z_s) → ((FSR2) + z_d)

Status Affected: None

Encoding:

1st word (source)	1110	1011	1zzz	$zzzz_s$
2nd word (dest.)	1111	xxxx	xzzz	$zzzz_d$

Description: The contents of the source register are moved to the destination register. The addresses of the source and destination registers are determined by adding the 7-bit literal offsets 'z_s' or 'z_d', respectively, to the value of FSR2. Both registers can be located anywhere in the 4096-byte data memory space (000h to FFFh).

The MOVSS instruction cannot use the PCL, TOSU, TOSH or TOSL as the destination register.

If the resultant source address points to an indirect addressing register, the value returned will be 00h. If the resultant destination address points to an indirect addressing register, the instruction will execute as a NOP.

Words: 2

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Determine source addr	Determine source addr	Read source reg
Decode	Determine dest addr	Determine dest addr	Write to dest reg

Example: MOVSS [05h], [06h]

Before Instruction
FSR2 = 80h
Contents of 85h = 33h
Contents of 86h = 11h
After Instruction
FSR2 = 80h
Contents of 85h = 33h
Contents of 86h = 33h

PUSHL **Store Literal at FSR2, Decrement FSR2**

Syntax: PUSHL k

Operands: $0 \le k \le 255$

Operation: k → (FSR2),
FSR2 – 1 → FSR2

Status Affected: None

Encoding:

1110	1010	kkkk	kkkk

Description: The 8-bit literal 'k' is written to the data memory address specified by FSR2. FSR2 is decremented by 1 after the operation.

This instruction allows users to push values onto a software stack.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read 'k'	Process data	Write to destination

Example: PUSHL 08h

Before Instruction
FSR2H:FSR2L = 01ECh
Memory (01ECh) = 00h

After Instruction
FSR2H:FSR2L = 01EBh
Memory (01ECh) = 08h

C

D