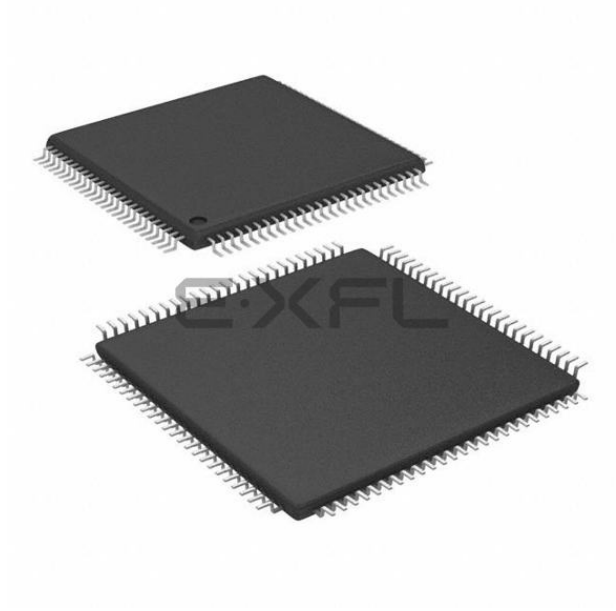


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	41.667MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	70
Program Memory Size	96KB (48K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3808 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf96j65-i-pt

TABLE 1-5: PIC18F86J60/86J65/87J60 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTD is a bidirectional I/O port.
RD0	72	I/O	ST	Digital I/O.
RD1	69	I/O	ST	Digital I/O.
RD2	68	I/O	ST	Digital I/O.
				PORTE is a bidirectional I/O port.
RE0/P2D	4			
RE0		I/O	ST	Digital I/O.
P2D		O	—	ECCP2 PWM Output D.
RE1/P2C	3			
RE1		I/O	ST	Digital I/O.
P2C		O	—	ECCP2 PWM Output C.
RE2/P2B	78			
RE2		I/O	ST	Digital I/O.
P2B		O	—	ECCP2 PWM Output B.
RE3/P3C	77			
RE3		I/O	ST	Digital I/O.
P3C(2)		O	—	ECCP3 PWM Output C.
RE4/P3B	76			
RE4		I/O	ST	Digital I/O.
P3B(2)		O	—	ECCP3 PWM Output B.
RE5/P1C	75			
RE5		I/O	ST	Digital I/O.
P1C(2)		O	—	ECCP1 PWM Output C.
RE6/P1B	74			
RE6		I/O	ST	Digital I/O.
P1B(2)		O	—	ECCP1 PWM Output B.
RE7/ECCP2/P2A	73			
RE7		I/O	ST	Digital I/O.
ECCP2(3)		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
P2A(3)		O	—	ECCP2 PWM Output A.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for ECCP2/P2A when CCP2MX Configuration bit is set.

2: Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

3: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared.

4: Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

TABLE 1-5: PIC18F86J60/86J65/87J60 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTG is a bidirectional I/O port.
RG0/ECCP3/P3A	56			
RG0		I/O	ST	Digital I/O.
ECCP3		I/O	ST	Capture 3 input/Compare 3 output/PWM3 output.
P3A		O	—	ECCP3 PWM Output A.
RG1/TX2/CK2	55			
RG1		I/O	ST	Digital I/O.
TX2		O	—	EUSART2 asynchronous transmit.
CK2		I/O	ST	EUSART2 synchronous clock (see related RX2/DT2 pin).
RG2/RX2/DT2	42			
RG2		I/O	ST	Digital I/O.
RX2		I	ST	EUSART2 asynchronous receive.
DT2		I/O	ST	EUSART2 synchronous data (see related TX2/CK2 pin).
RG3/CCP4/P3D	41			
RG3		I/O	ST	Digital I/O.
CCP4		I/O	ST	Capture 4 input/Compare 4 output/PWM4 output.
P3D		O	—	ECCP3 PWM Output D.
RG4/CCP5/P1D	10			
RG4		I/O	ST	Digital I/O.
CCP5		I/O	ST	Capture 5 input/Compare 5 output/PWM5 output.
P1D		O	—	ECCP1 PWM Output D.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for ECCP2/P2A when CCP2MX Configuration bit is set.

2: Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

3: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared.

4: Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

TABLE 1-5: PIC18F86J60/86J65/87J60 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTH is a bidirectional I/O port.
RH0	79	I/O	ST	Digital I/O.
RH1	80	I/O	ST	Digital I/O.
RH2	1	I/O	ST	Digital I/O.
RH3	2	I/O	ST	Digital I/O.
RH4/AN12/P3C	22			
RH4		I/O	ST	Digital I/O.
AN12		I	Analog	Analog Input 12.
P3C(4)		O	—	ECCP3 PWM Output C.
RH5/AN13/P3B	21			
RH5		I/O	ST	Digital I/O.
AN13		I	Analog	Analog Input 13.
P3B(4)		O	—	ECCP3 PWM Output B.
RH6/AN14/P1C	20			
RH6		I/O	ST	Digital I/O.
AN14		I	Analog	Analog Input 14.
P1C(4)		O	—	ECCP1 PWM Output C.
RH7/AN15/P1B	19			
RH7		I/O	ST	Digital I/O.
AN15		I	Analog	Analog Input 15.
P1B(4)		O	—	ECCP1 PWM Output B.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for ECCP2/P2A when CCP2MX Configuration bit is set.

2: Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

3: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared.

4: Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

8.2 Address and Data Width

The PIC18F97J60 family of devices can be independently configured for different address and data widths on the same memory bus. Both address and data widths are set by Configuration bits in the CONFIG3L register. As Configuration bits, this means that these options can only be configured by programming the device and are not controllable in software.

The BW bit selects an 8-bit or 16-bit data bus width. Setting this bit (default) selects a data width of 16 bits.

The EMB<1:0> bits determine both the program memory operating mode and the address bus width. The available options are 20-bit, 16-bit and 12-bit, as well as the default Microcontroller mode (external bus disabled). Selecting a 16-bit or 12-bit width makes a corresponding number of high-order lines available for I/O functions. These pins are no longer affected by the setting of the EBDIS bit. For example, selecting a 16-Bit Addressing mode (EMB<1:0> = 01) disables A<19:16> and allows the PORTH<3:0> bits to function without interruptions from the bus. Using the smaller address widths allows users to tailor the memory bus to the size of the external memory space for a particular design, while freeing up pins for dedicated I/O operation.

Because the EMB bits have the effect of disabling pins for memory bus operations, it is important to always select an address width at least equal to the data width. If a 12-bit address width is used with a 16-bit data width, the upper four bits of data will not be available in the bus.

All combinations of address and data widths require multiplexing of address and data information on the same lines. The address and data multiplexing, as well as I/O ports made available by the use of smaller address widths, are summarized in Table 8-2.

8.2.1 ADDRESS SHIFTING ON THE EXTERNAL BUS

By default, the address presented on the external bus is the value of the PC. In practical terms, this means that addresses in the external memory device below the top of on-chip memory are unavailable to the microcontroller. To access these physical locations, the glue logic between the microcontroller and the external memory must somehow translate addresses.

To simplify the interface, the external bus offers an extension of Extended Microcontroller mode that automatically performs address shifting. This feature is controlled by the EASHFT Configuration bit. Setting this bit offsets addresses on the bus by the size of the microcontroller's on-chip program memory and sets the bottom address at 0000h. This allows the device to use the entire range of physical addresses of the external memory.

8.2.2 21-BIT ADDRESSING

As an extension of 20-bit address width operation, the external memory bus can also fully address a 2-Mbyte memory space. This is done by using the Bus Address Bit 0 (BA0) control line as the Least Significant bit of the address. The $\overline{UB}$ and $\overline{LB}$ control signals may also be used with certain memory devices to select the upper and lower bytes within a 16-bit wide data word.

This addressing mode is available in both 8-Bit Data Width and certain 16-Bit Data Width modes. Additional details are provided in **Section 8.6.3 "16-Bit Byte Select Mode"** and **Section 8.7 "8-Bit Data Width Mode"**.

TABLE 8-2: ADDRESS AND DATA LINES FOR DIFFERENT ADDRESS AND DATA WIDTHS

Data Width	Address Width	Multiplexed Data and Address Lines (and corresponding ports)	Address Only Lines (and corresponding ports)	Ports Available for I/O
8-bit	12-bit	AD<7:0> (PORTD<7:0>)	AD<11:8> (PORTE<3:0>)	PORTE<7:4>, All of PORTH
	16-bit		AD<15:8> (PORTE<7:0>)	All of PORTH
	20-bit		A<19:16>, AD<15:8> (PORTH<3:0>, PORTE<7:0>)	—
16-bit	16-bit	AD<15:0> (PORTD<7:0>, PORTE<7:0>)	—	All of PORTH
	20-bit		A<19:16> (PORTH<3:0>)	—

11.4 PORTC, TRISC and LATC Registers

PORTC is an 8-bit wide, bidirectional port; it is fully implemented on all devices. The corresponding Data Direction register is TRISC. Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., put the contents of the output latch on the selected pin). Only PORTC pins, RC2 through RC7, are digital only pins and can tolerate input voltages up to 5.5V.

The Output Latch register (LATC) is also memory mapped. Read-modify-write operations on the LATC register read and write the latched output value for PORTC.

PORTC is multiplexed with several peripheral functions (Table 11-7). The pins have Schmitt Trigger input buffers. RC1 is normally configured by Configuration bit, CCP2MX, as the default peripheral pin for the ECCP2 module and Enhanced PWM output, P2A (default state, CCP2MX = 1).

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

Note:	These pins are configured as digital inputs on any device Reset.

The contents of the TRISC register are affected by peripheral overrides. Reading TRISC always returns the current contents, even though a peripheral device may be overriding one or more of the pins.

EXAMPLE 11-3: INITIALIZING PORTC

```
CLRF    PORTC   ; Initialize PORTC by
                ; clearing output
                ; data latches
CLRF    LATC    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   0CFh    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISC   ; Set RC<3:0> as inputs
                ; RC<5:4> as outputs
                ; RC<7:6> as inputs
```

TABLE 11-11: PORTE FUNCTIONS (CONTINUED)

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RE5/AD13/ P1C	RE5	0	O	DIG	LATE<5> data output.
		1	I	ST	PORTE<5> data input; weak pull-up when REPU bit is set.
	AD13(1)	x	O	DIG	External memory interface, Address/Data Bit 13 output.(2)
		x	I	TTL	External memory interface, Data Bit 13 input.(2)
	P1C(3)	0	O	DIG	ECCP1 Enhanced PWM output, Channel C; takes priority over port and PSP data. May be configured for tri-state during Enhanced PWM shutdown events.
RE6/AD14/ P1B(4)	RE6	0	O	DIG	LATE<6> data output.
		1	I	ST	PORTE<6> data input; weak pull-up when REPU bit is set.
	AD14(1)	x	O	DIG	External memory interface, Address/Data Bit 14 output.(2)
		x	I	TTL	External memory interface, Data Bit 14 input.(2)
	P1B(3)	0	O	DIG	ECCP1 Enhanced PWM output, Channel B; takes priority over port and PSP data. May be configured for tri-state during Enhanced PWM shutdown events.
RE7/AD15/ ECCP2/P2A(4)	RE7	0	O	DIG	LATE<7> data output.
		1	I	ST	PORTE<7> data input; weak pull-up when REPU bit is set.
	AD15(1)	x	O	DIG	External memory interface, Address/Data Bit 15 output.(2)
		x	I	TTL	External memory interface, Data Bit 15 input.(2)
	ECCP2(5)	0	O	DIG	ECCP2 compare output and PWM output; takes priority over port data.
		1	I	ST	ECCP2 capture input.
	P2A(5)	0	O	DIG	ECCP2 Enhanced PWM output, Channel A; takes priority over port and PSP data. May be configured for tri-state during Enhanced PWM shutdown events.

Legend: O = Output, I = Input, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

Note 1: EMB functions are implemented on 100-pin devices only.

2: External memory interface I/O takes priority over all other digital and PSP I/O.

3: Default assignments for P1B/P1C and P3B/P3C when ECCPMX Configuration bit is set (80-pin and 100-pin devices).

4: Unimplemented on 64-pin devices.

5: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared (80-pin and 100-pin devices in Microcontroller mode).

6: Unimplemented on 64-pin and 80-pin devices.

TABLE 11-12: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
PORTE	RE7(1)	RE6(1)	RE5	RE4	RE3	RE2	RE1	RE0	72
LATE	LATE7(1)	LATE6(1)	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	72
TRISE	TRISE7(1)	TRISE6(1)	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	71
LATA	RDPU	REPU	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	72

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTE.

Note 1: Unimplemented on 64-pin devices; read as '0'.

14.0 TIMER2 MODULE

The Timer2 timer module incorporates the following features:

- 8-Bit Timer and Period registers (TMR2 and PR2, respectively)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4 and 1:16)
- Software programmable postscaler (1:1 through 1:16)
- Interrupt on TMR2 to PR2 match
- Optional use as the shift clock for the MSSPx modules

This module is controlled through the T2CON register (Register 14-1) which enables or disables the timer and configures the prescaler and postscaler. Timer2 can be shut off by clearing control bit, TMR2ON (T2CON<2>), to minimize power consumption.

A simplified block diagram of the module is shown in Figure 14-1.

14.1 Timer2 Operation

In normal operation, TMR2 is incremented from 00h on each clock (FOSC/4). A 4-bit counter/prescaler on the clock input gives direct input, divide-by-4 and divide-by-16 prescale options. These options are selected by the prescaler control bits, T2CKPS<1:0> (T2CON<1:0>). The value of TMR2 is compared to that of the Period register, PR2, on each clock cycle. When the two values match, the comparator generates a match signal as the timer output. This signal also resets the value of TMR2 to 00h on the next cycle and drives the output counter/postscaler (see **Section 14.2 "Timer2 Interrupt"**).

The TMR2 and PR2 registers are both directly readable and writable. The TMR2 register is cleared on any device Reset, while the PR2 register initializes at FFh. Both the prescaler and postscaler counters are cleared on the following events:

- A write to the TMR2 register
- A write to the T2CON register
- Any device Reset (Power-on Reset, $\overline{\text{MCLR}}$ Reset, Watchdog Timer Reset or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

REGISTER 14-1: T2CON: TIMER2 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **T2OUTPS<3:0>**: Timer2 Output Postscale Select bits
0000 = 1:1 Postscale
0001 = 1:2 Postscale
•
•
•
1111 = 1:16 Postscale

bit 2 **TMR2ON**: Timer2 On bit
1 = Timer2 is on
0 = Timer2 is off

bit 1-0 **T2CKPS<1:0>**: Timer2 Clock Prescale Select bits
00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

18.4.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> bits contain the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The PWM duty cycle is calculated by the equation:

EQUATION 18-2:

$$\text{PWM Duty Cycle} = (\text{CCPR1L:CCP1CON<5:4>}) \bullet T_{OSC} \bullet (\text{TMR2 Prescale Value})$$

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not copied into CCPR1H until a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double-buffer the PWM duty cycle. This double-buffering is essential for glitchless PWM operation. When the CCPR1H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock or two bits of the TMR2 prescaler, the ECCP1 pin is cleared. The maximum PWM resolution (bits) for a given PWM frequency is given by the following equation:

EQUATION 18-3:

$$\text{PWM Resolution (max)} = \frac{\log\left(\frac{F_{OSC}}{F_{PWM}}\right)}{\log(2)} \text{ bits}$$

Note:	If the PWM duty cycle value is longer than the PWM period, the ECCP1 pin will not be cleared.

18.4.3 PWM OUTPUT CONFIGURATIONS

The P1M<1:0> bits in the CCP1CON register allow one of four configurations:

- Single Output
- Half-Bridge Output
- Full-Bridge Output, Forward mode
- Full-Bridge Output, Reverse mode

The Single Output mode is the standard PWM mode discussed in **Section 18.4 "Enhanced PWM Mode"**. The Half-Bridge and Full-Bridge Output modes are covered in detail in the sections that follow.

The general relationship of the outputs in all configurations is summarized in Figure 18-2.

TABLE 18-4: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 40 MHz

PWM Frequency	2.44 kHz	9.77 kHz	39.06 kHz	156.25 kHz	312.50 kHz	416.67 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	FFh	FFh	FFh	3Fh	1Fh	17h
Maximum Resolution (bits)	10	10	10	8	7	6.58

18.4.6 PROGRAMMABLE DEAD-BAND DELAY

In half-bridge applications, where all power switches are modulated at the PWM frequency at all times, the power switches normally require more time to turn off than to turn on. If both the upper and lower power switches are switched at the same time (one turned on and the other turned off), both switches may be on for a short period of time until one switch completely turns off. During this brief interval, a very high current (*shoot-through current*) may flow through both power switches, shorting the bridge supply. To avoid this potentially destructive shoot-through current from flowing during switching, turning on either of the power switches is normally delayed to allow the other switch to completely turn off.

In the Half-Bridge Output mode, a digitally programmable dead-band delay is available to avoid shoot-through current from destroying the bridge power switches. The delay occurs at the signal transition from the non-active state to the active state. See Figure 18-4 for the illustration. The lower seven bits of the ECCP1DEL register (Register 18-2) set the delay period in terms of microcontroller instruction cycles (TCY or 4 TOSC).

18.4.7 ENHANCED PWM AUTO-SHUTDOWN

When the ECCP1 is programmed for any of the Enhanced PWM modes, the active output pins may be configured for auto-shutdown. Auto-shutdown immediately places the Enhanced PWM output pins into a defined shutdown state when a shutdown event occurs.

A shutdown event can be caused by either of the two comparator modules or the FLT0 pin (or any combination of these three sources). The comparators may be used to monitor a voltage input proportional to a current being monitored in the bridge circuit. If the voltage exceeds a threshold, the comparator switches state and triggers a shutdown. Alternatively, a low-level digital signal on the FLT0 pin can also trigger a shutdown. The auto-shutdown feature can be disabled by not selecting any auto-shutdown sources. The auto-shutdown sources to be used are selected using the ECCP1AS<2:0> bits (ECCP1AS<6:4>).

When a shutdown occurs, the output pins are asynchronously placed in their shutdown states, specified by the PSS1AC<1:0> and PSS1BD<1:0> bits (ECCP1AS<3:0>). Each pin pair (P1A/P1C and P1B/P1D) may be set to drive high, drive low or be tri-stated (not driving). The ECCP1ASE bit (ECCP1AS<7>) is also set to hold the Enhanced PWM outputs in their shutdown states.

The ECCP1ASE bit is set by hardware when a shutdown event occurs. If automatic restarts are not enabled, the ECCP1ASE bit is cleared by firmware when the cause of the shutdown clears. If automatic restarts are enabled, the ECC1PASE bit is automatically cleared when the cause of the auto-shutdown has cleared.

If the ECCP1ASE bit is set when a PWM period begins, the PWM outputs remain in their shutdown state for that entire PWM period. When the ECCP1ASE bit is cleared, the PWM outputs will return to normal operation at the beginning of the next PWM period.

Note:	Writing to the ECCP1ASE bit is disabled while a shutdown condition is active.

REGISTER 18-2: ECCP1DEL: ECCP1 DEAD-BAND DELAY REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
P1RSEN	P1DC6	P1DC5	P1DC4	P1DC3	P1DC2	P1DC1	P1DC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **P1RSEN:** PWM Restart Enable bit

1 = Upon auto-shutdown, the ECCP1ASE bit clears automatically once the shutdown event goes away; the PWM restarts automatically

0 = Upon auto-shutdown, ECCP1ASE must be cleared in software to restart the PWM

bit 6-0 **P1DC<6:0>:** PWM Delay Count bits

Delay time, in number of FOSC/4 (4 * TOSC) cycles, between the scheduled time and actual time for a PWM signal to transition to active.

19.2.1.3 Transmit Buffer

Any space within the 8-Kbyte memory which is not programmed as part of the receive FIFO buffer is considered to be the transmit buffer. The responsibility of managing where packets are located in the transmit buffer belongs to the application. Whenever the application decides to transmit a packet, the ETXST and ETXND Pointers are programmed with addresses specifying where, within the transmit buffer, the particular packet to transmit is located. The hardware does not check that the start and end addresses do not overlap with the receive buffer. To prevent buffer corruption, the firmware must not transmit a packet while the ETXST and ETXND Pointers are overlapping the receive buffer, or while the ETXND Pointers are too close to the receive buffer. See **Section 19.5.2 "Transmitting Packets"** for more information.

19.2.1.4 Buffer Arbiter and Access Arbitration

The Ethernet buffer is clocked at one-half of the microcontroller clock rate. Varying amounts of memory access bandwidth are available depending on the clock speed. The total bandwidth available, in bytes per second, is equal to twice the instruction rate (2 * FCY or FOSC/2). For example, at a system clock speed of 41.667 MHz, the total available memory bandwidth that is available is 20.834 Mbyte/s. At an Ethernet signaling rate of 10 Mbit/s, the Ethernet RX engine requires 1.25 Mbyte/s of buffer memory bandwidth to operate without causing an overrun. If Full-Duplex mode is used, an additional 1.25 Mbyte/s is required to allow for simultaneous RX and TX activity.

Because of the finite available memory bandwidth, a three-channel arbiter is used to allocate bandwidth between the RX engine, the TX and DMA engines, and the microcontroller's CPU (i.e., the application accessing EDATA). The arbiter gives the EDATA register accesses first priority, while all remaining bandwidth is shared between the RX and TX/DMA blocks.

With arbitration, bandwidth limitations require that some care be taken in balancing the needs of the module's hardware with that of the application. Accessing the EDATA register too often may result in the RX or TX blocks causing a buffer overrun or underrun, respectively. If such a memory access failure occurs, the BUFER bit (ESTAT<6>), and either the TXERIF or RXERIF interrupt flag, becomes set, and a TX or RX interrupt occurs (if enabled). In either case, the current packet will be lost or aborted.

To eliminate the risk of lost packets, run the microcontroller core at higher speeds. Following the arbitration restrictions, shown in Table 19-2, will prevent memory access failures from occurring. Also, avoid using segments of application code which perform back-to-back accesses of the EDATA register. Instead, insert one or more instructions (including NOP instructions) between each read or write to EDATA.

19.2.1.5 DMA Access to the Buffer

The integrated DMA controller must read from the buffer when calculating a checksum, and it must read and write to the buffer when copying memory. The DMA follows the same wrapping rules as previously described for the receive buffer. While it sequentially reads, it will be subject to a wrapping condition at the end of the receive buffer. All writes it does will not be subject to any wrapping conditions. See **Section 19.9 "Direct Memory Access Controller"** for more information.

TABLE 19-2: BUFFER ARBITRATION RESTRICTIONS VS. CLOCK SPEED

FOSC (MHz)	FCY (MHz)	Available Bandwidth (Mbyte/s)			Application Restrictions to Prevent Underrun/Overrun
		Total	After RX	After TX	
41.667	10.42	20.83	19.58	18.33	Access EDATA no more than once every 2 TCY
31.250	7.81	15.63	14.38	13.13	Access EDATA no more than once every 2 TCY
25.000	6.25	12.50	11.25	10.00	Access EDATA no more than once every 2 TCY
20.833	5.21	10.42	9.17	7.92	Access EDATA no more than once every 2 TCY
13.889	3.47	6.94	5.69	4.44	Access EDATA no more than once every 2 TCY
12.500	3.13	6.25	5.00	3.75	Access EDATA no more than once every 2 TCY
8.333	2.08	4.17	2.92	1.67	Access EDATA no more than once every 3 TCY
6.250	1.56	3.13	1.88	0.63	Access EDATA no more than once every 5 TCY
4.167	1.04	2.08	0.83	< 0	Do not use DMA, do not use full duplex, access EDATA no more than once every 3 TCY
2.778	0.69	1.39	0.14	< 0	Do not use DMA, do not use full duplex, access EDATA no more than once every 10 TCY

REGISTER 19-12: PHSTAT2: PHYSICAL LAYER STATUS REGISTER 2

U-0	U-0	R-0	R-0	R-0	R-0	R-x	U-0
—	—	TXSTAT	RXSTAT	COLSTAT	LSTAT	r	—
bit 15							bit 8

U-0	U-0	R-0	U-0	U-0	U-0	U-0	U-0
—	—	r	—	—	—	—	—
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **TXSTAT:** PHY Transmit Status bit
1 = PHY is transmitting data
0 = PHY is not transmitting data

bit 12 **RXSTAT:** PHY Receive Status bit
1 = PHY is receiving data
0 = PHY is not receiving data

bit 11 **COLSTAT:** PHY Collision Status bit
1 = A collision is occuring (PHY is both transmitting and receiving while in Half-Duplex mode)
0 = A collision is not occuring

bit 10 **LSTAT:** PHY Collision Status bit
1 = Link is up
0 = Link is down

bit 9 **Reserved:** Ignore on read

bit 8-6 **Unimplemented:** Read as ‘0’

bit 5 **Reserved:** Ignore on read

bit 4-0 **Unimplemented:** Read as ‘0’

20.3.8 OPERATION IN POWER-MANAGED MODES

In SPI Master mode, module clocks may be operating at a different speed than when in full-power mode. In the case of Sleep mode, all clocks are halted.

In Idle modes, a clock is provided to the peripherals. That clock should be from the primary clock source, the secondary clock (Timer1 oscillator at 32.768 kHz) or the INTRC source. See **Section 3.7 "Clock Sources and Oscillator Switching"** for additional information.

In most cases, the speed that the master clocks SPI data is not important; however, this should be evaluated for each system.

If MSSP interrupts are enabled, they can wake the controller from Sleep mode, or one of the Idle modes, when the master completes sending data. If an exit from Sleep or Idle mode is not desired, MSSP interrupts should be disabled.

If the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the devices wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in any power-managed mode and data to be shifted into the SPI Transmit/Receive Shift register. When all 8 bits have been received, the MSSP interrupt flag bit will be set, and if enabled, will wake the device.

20.3.9 EFFECTS OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

20.3.10 BUS MODE COMPATIBILITY

Table 20-1 shows the compatibility between the standard SPI modes and the states of the CKP and CKE control bits.

TABLE 20-1: SPI BUS MODES

Standard SPI Mode Terminology	Control Bits State	
	CKP	CKE
0, 0	0	1
0, 1	0	0
1, 0	1	1
1, 1	1	0

There is also an SMP bit which controls when the data is sampled.

20.3.11 SPI CLOCK SPEED AND MODULE INTERACTIONS

Because MSSP1 and MSSP2 are independent modules, they can operate simultaneously at different data rates. Setting the SSPM<3:0> bits of the SSPxCON1 register determines the rate for the corresponding module.

An exception is when both modules use Timer2 as a time base in Master mode. In this instance, any changes to the Timer2 operation will affect both MSSP modules equally. If different bit rates are required for each module, the user should select one of the other three time base options for one of the modules.

20.4.5 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the I^2C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master. The exception is the general call address, which can address all devices. When this address is used, all devices should, in theory, respond with an Acknowledge.

The general call address is one of eight addresses reserved for specific purposes by the I^2C protocol. It consists of all '0's with R/$\overline{W}$ = 0.

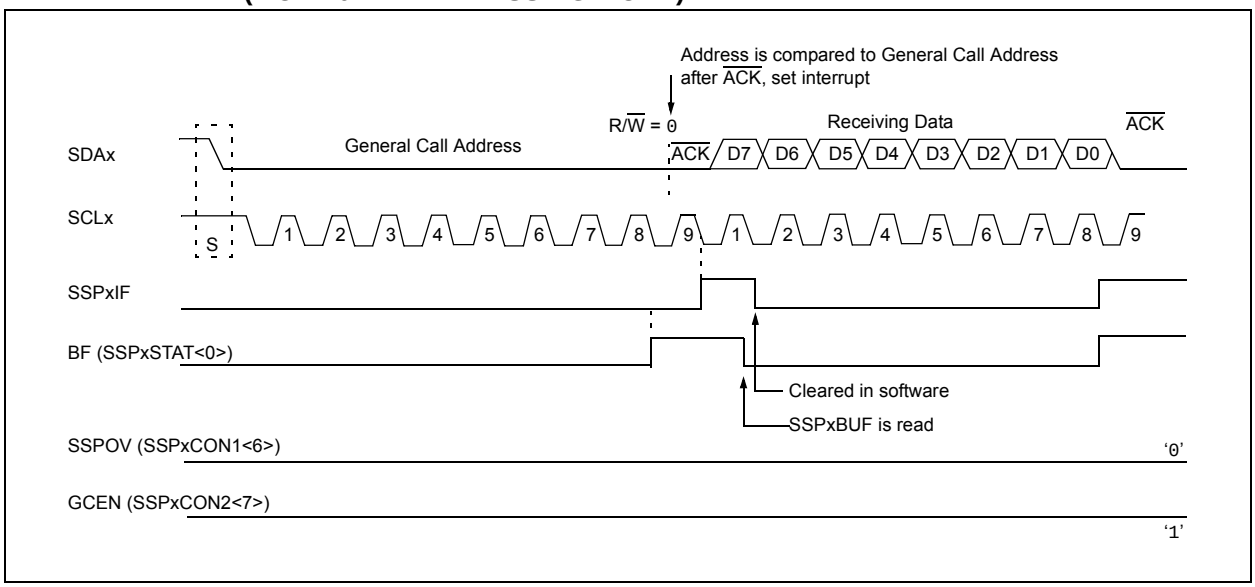
The general call address is recognized when the General Call Enable bit, GCEN, is enabled (SSPxCON2<7> set). Following a Start bit detect, 8 bits are shifted into the SSPxSR and the address is compared against the SSPxADD. It is also compared to the general call address and fixed in hardware.

If the general call address matches, the SSPxSR is transferred to the SSPxBUF, the BF flag bit is set (eighth bit) and on the falling edge of the ninth bit ($\overline{ACK}$ bit), the SSPxIF interrupt flag bit is set.

When the interrupt is serviced, the source for the interrupt can be checked by reading the contents of the SSPxBUF. The value can be used to determine if the address was device-specific or a general call address.

In 10-Bit Addressing mode, the SSPxADD is required to be updated for the second half of the address to match, and the UA bit is set (SSPxSTAT<1>). If the general call address is sampled when the GCEN bit is set, while the slave is configured in 10-Bit Addressing mode, then the second half of the address is not necessary, the UA bit will not be set and the slave will begin receiving data after the Acknowledge (Figure 20-17).

FIGURE 20-17: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE (7 OR 10-BIT ADDRESSING MODE)



21.1.3 AUTO-BAUD RATE DETECT

The Enhanced USARTx module supports the automatic detection and calibration of baud rate. This feature is active only in Asynchronous mode and while the WUE bit is clear.

The automatic baud rate measurement sequence (Figure 21-1) begins whenever a Start bit is received and the ABDEN bit is set. The calculation is self-averaging.

In the Auto-Baud Rate Detect (ABD) mode, the clock to the BRG is reversed. Rather than the BRG clocking the incoming RXx signal, the RXx signal is timing the BRG. In ABD mode, the internal Baud Rate Generator is used as a counter to time the bit period of the incoming serial byte stream.

Once the ABDEN bit is set, the state machine will clear the BRG and look for a Start bit. The Auto-Baud Rate Detect must receive a byte with the value 55h (ASCII "U", which is also the LIN/J2602 bus Sync character) in order to calculate the proper bit rate. The measurement is taken over both a low and high bit time in order to minimize any effects caused by asymmetry of the incoming signal. After a Start bit, the SPBRGx begins counting up, using the preselected clock source on the first rising edge of RXx. After eight bits on the RXx pin or the fifth rising edge, an accumulated value totalling the proper BRG period is left in the SPBRGHx:SPBRGx register pair. Once the 5th edge is seen (this should correspond to the Stop bit), the ABDEN bit is automatically cleared.

If a rollover of the BRG occurs (an overflow from FFFFh to 0000h), the event is trapped by the ABDOVF status bit (BAUDCONx<7>). It is set in hardware by BRG rollovers and can be set or cleared by the user in software. ABD mode remains active after rollover events and the ABDEN bit remains set (Figure 21-2).

While calibrating the baud rate period, the BRG registers are clocked at 1/8th the preconfigured clock rate. Note that the BRG clock will be configured by the BRG16 and BRGH bits. Independent of the BRG16 bit setting, both the SPBRGx and SPBRGHx will be used as a 16-bit counter. This allows the user to verify that no carry occurred for 8-bit modes by checking for 00h in the SPBRGHx register. Refer to Table 21-4 for counter clock rates to the BRG.

While the ABD sequence takes place, the EUSARTx state machine is held in Idle. The RCxIF interrupt is set once the fifth rising edge on RXx is detected. The value in the RCREGx needs to be read to clear the RCxIF interrupt. The contents of RCREGx should be discarded.

Note 1:	If the WUE bit is set with the ABDEN bit, Auto-Baud Rate Detection will occur on the byte *following* the Break character.
2:	It is up to the user to determine that the incoming character baud rate is within the range of the selected BRG clock source. Some combinations of oscillator frequency and EUSARTx baud rates are not possible due to bit error rates. Overall system timing and communication baud rates must be taken into consideration when using the Auto-Baud Rate Detection feature.

TABLE 21-4: BRG COUNTER CLOCK RATES

BRG16	BRGH	BRG Counter Clock
0	0	FOSC/512
0	1	FOSC/128
1	0	FOSC/128
1	1	FOSC/32

Note: During the ABD sequence, SPBRGx and SPBRGHx are both used as a 16-bit counter, independent of the BRG16 setting.

21.1.3.1 ABD and EUSARTx Transmission

Since the BRG clock is reversed during ABD acquisition, the EUSARTx transmitter cannot be used during ABD. This means that whenever the ABDEN bit is set, TXREGx cannot be written to. Users should also ensure that ABDEN does not become set during a transmit sequence. Failing to do this may result in unpredictable EUSARTx operation.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (AV_{DD} and AV_{SS}), or the voltage level on the RA3/AN3/V_{REF+} and RA2/AN2/V_{REF-} pins.

The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in **Sleep**, the A/D conversion clock must be derived from the A/D Converter's internal RC oscillator.

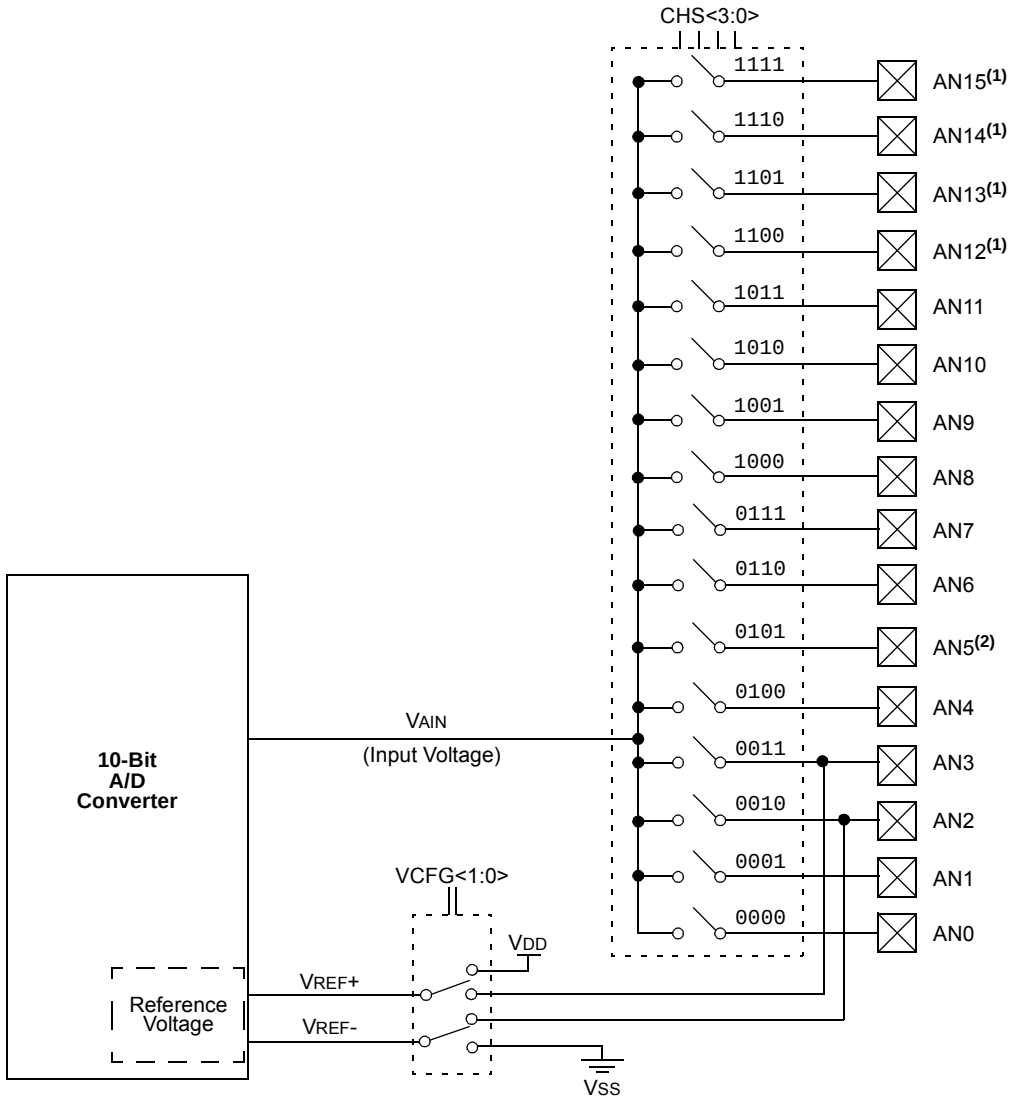
The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

Each port pin associated with the A/D Converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/$\overline{DONE}$ bit (ADCON0<1>) is cleared and the A/D Interrupt Flag bit, ADIF, is set.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted. The value in the ADRESH:ADRESL register pair is not modified for a Power-on Reset. These registers will contain unknown data after a Power-on Reset.

The block diagram of the A/D module is shown in Figure 22-1.

FIGURE 22-1: A/D BLOCK DIAGRAM



Note 1: Channels AN15 through AN12 are not available in 64-pin devices.
2: Channel AN5 is implemented in 100-pin devices only.

REGISTER 25-6: CONFIG3H: CONFIGURATION REGISTER 3 HIGH (BYTE ADDRESS 300005h)

U-0	U-0	U-0	U-0	U-0	R/WO-1	R/WO-1	R/WO-1
—(1)	—(1)	—(1)	—(1)	—	ETHLED	ECCPMX(2)	CCP2MX(2)
bit 7							bit 0

Legend:		
R = Readable bit	WO = Write-Once bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed	'1' = Bit is set	'0' = Bit is cleared

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **ETHLED:** Ethernet LED Enable bit
- 1 = RA0/RA1 are multiplexed with LEDA/LEDB when the Ethernet module is enabled and function as I/O when the Ethernet is disabled
- 0 = RA0/RA1 function as I/O regardless of Ethernet module status

bit 1 **ECCPMX:** ECCP MUX bit(2)
- 1 = ECCP1 outputs (P1B/P1C) are multiplexed with RE6 and RE5; ECCP3 outputs (P3B/P3C) are multiplexed with RE4 and RE3
- 0 = ECCP1 outputs (P1B/P1C) are multiplexed with RH7 and RH6; ECCP3 outputs (P3B/P3C) are multiplexed with RH5 and RH4

bit 0 **CCP2MX:** ECCP2 MUX bit(2)
- 1 = ECCP2/P2A is multiplexed with RC1
- 0 = ECCP2/P2A is multiplexed with RE7 in Microcontroller mode (80-pin and 100-pin devices) or with RB3 in Extended Microcontroller mode (100-pin devices only)

Note 1: The value of these bits in program memory should always be '1'. This ensures that the location is executed as a NOP if it is accidentally executed.

2: Implemented in 80-pin and 100-pin devices only.

RETURN **Return from Subroutine**

Syntax: RETURN {s}

Operands: s ∈ [0,1]

Operation: (TOS) → PC;
if s = 1,
(WS) → W,
(STATUSS) → STATUS,
(BSRS) → BSR,
PCLATU, PCLATH are unchanged

Status Affected: None

Encoding:

0000	0000	0001	001s

Description: Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the program counter. If 's'= 1, the contents of the shadow registers WS, STATUSS and BSRS are loaded into their corresponding registers W, STATUS and BSR. If 's' = 0, no update of these registers occurs (default).

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	Process Data	POP PC from stack
No operation	No operation	No operation	No operation

Example: RETURN

After Instruction:
PC = TOS

RLCF **Rotate Left f through Carry**

Syntax: RLCF f {,d {,a}}

Operands: 0 ≤ f ≤ 255
d ∈ [0,1]
a ∈ [0,1]

Operation: (f<n>) → dest<n + 1>,
(f<7>) → C,
(C) → dest<0>

Status Affected: C, N, Z

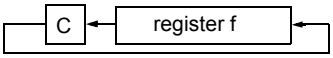
Encoding:

0011	01da	ffff	ffff

Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f' (default).

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See **Section 26.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.



Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: RLCF REG, 0, 0

Before Instruction
REG = 1110 0110
C = 0
After Instruction
REG = 1110 0110
W = 1100 1100
C = 1

28.4.2 TIMING CONDITIONS

The temperature and voltages specified in Table 28-5 apply to all timing specifications unless otherwise noted. Figure 28-3 specifies the load conditions for the timing specifications.

TABLE 28-5: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial Operating voltage VDD range as described in DC spec **Section 28.1 "DC Characteristics: Supply Voltage, PIC18F97J60 Family (Industrial)"** and **Section 28.3 "DC Characteristics: PIC18F97J60 Family (Industrial)"**.

FIGURE 28-3: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

RL = 464Ω

CL = 50 pF for all pins except OSC2/CLKO and including D and E outputs as ports

CL = 15 pF for OSC2/CLKO

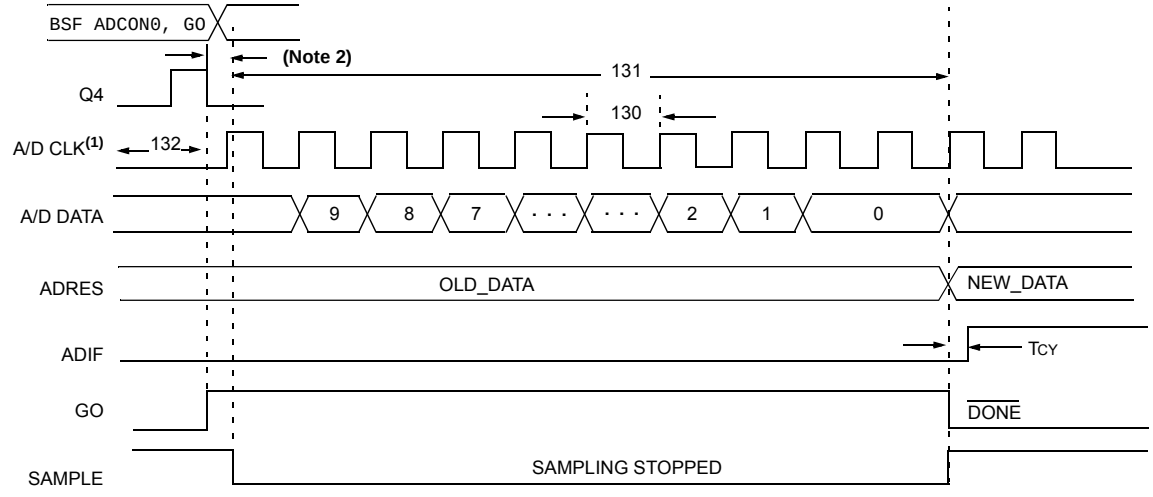
TABLE 28-26: A/D CONVERTER CHARACTERISTICS: PIC18F97J60 FAMILY (INDUSTRIAL)

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
A01	NR	Resolution	—	—	10	bit	ΔVREF ≥ 2.0V
A03	EIL	Integral Linearity Error	—	—	<±1	LSb	ΔVREF ≥ 2.0V
A04	EDL	Differential Linearity Error	—	—	<±1	LSb	ΔVREF ≥ 2.0V
A06	EOFF	Offset Error	—	—	<±3	LSb	ΔVREF ≥ 2.0V
A07	EGN	Gain Error	—	—	<±3	LSb	ΔVREF ≥ 2.0V
A10	—	Monotonicity	Guaranteed(1)			—	VSS ≤ VAIN ≤ VREF
A20	ΔVREF	Reference Voltage Range (VREFH – VREFL) Reference Voltage Range (VREFH – VREFL)	1.8 3	— —	— —	V V	VDD < 3.0V VDD ≥ 3.0V
	VREFSUM	Reference Voltage Sum (VREFH + VREFL)	—	—	AVDD + 0.5	V	
A21	VREFH	Reference Voltage High	VREFL	—	AVDD	V	
A22	VREFL	Reference Voltage Low	AVSS	—	VREFH	V	
A25	VAIN	Analog Input Voltage	VREFL	—	VREFH	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	2.5	kΩ	
A50	IREF	VREF Input Current(2) VREF Input Current(2)	— —	— —	5 1000	μA μA	During VAIN acquisition. During A/D conversion cycle.

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

2: VREFH current is from RA3/AN3/VREF+ pin or AVDD, whichever is selected as the VREFH source. VREFL current is from RA2/AN2/VREF- pin or AVSS, whichever is selected as the VREFL source.

FIGURE 28-21: A/D CONVERSION TIMING

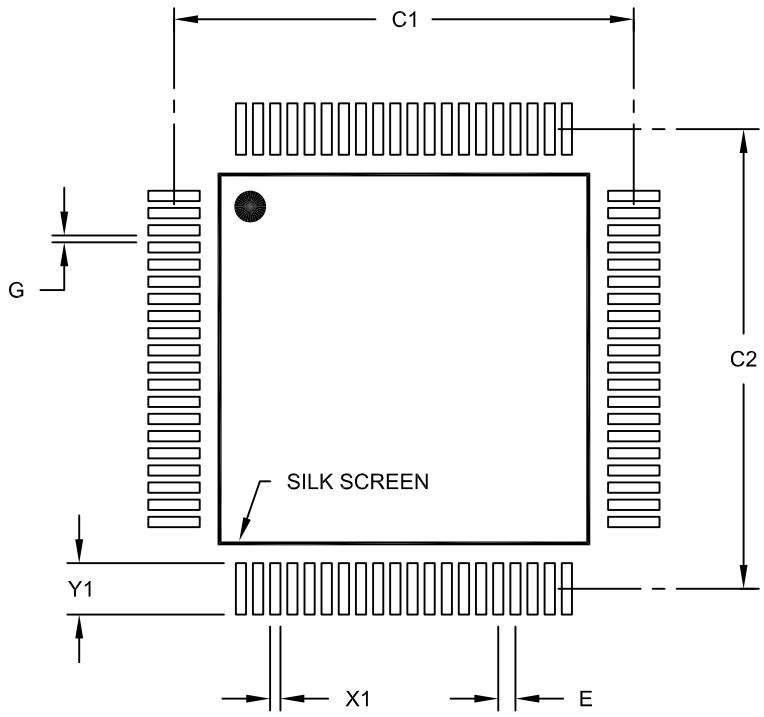


Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

2: This is a minimal RC delay (typically 100 ns), which also disconnects the holding capacitor from the analog input.

80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X80)	X1			0.30
Contact Pad Length (X80)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2092A