Infineon Technologies - C165L25FHABFQMA1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	77
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	PG-TQFP-100
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c165l25fhabfqma1

Edition 2000-12

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide.

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

This document describes several derivatives of the C165 group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

Table 1 C165 Derivative Synopsis

Derivative[1)]	Max. Operating Frequency	Operating Voltage	Package
SAF-C165-LM	20 MHz	4.5 to 5.5 V	MQFP-100
SAB-C165-LM	20 MHz	4.5 to 5.5 V	MQFP-100
SAF-C165-L25M	25 MHz	4.5 to 5.5 V	MQFP-100
SAB-C165-L25M	25 MHz	4.5 to 5.5 V	MQFP-100
SAF-C165-LF	20 MHz	4.5 to 5.5 V	TQFP-100
SAB-C165-LF	20 MHz	4.5 to 5.5 V	TQFP-100
SAF-C165-L25F	25 MHz	4.5 to 5.5 V	TQFP-100
SAB-C165-L25F	25 MHz	4.5 to 5.5 V	TQFP-100
SAF-C165-LM3V	20 MHz	3.0 to 3.6 V	MQFP-100
SAB-C165-LM3V	20 MHz	3.0 to 3.6 V	MQFP-100
SAF-C165-LF3V	20 MHz	3.0 to 3.6 V	TQFP-100
SAB-C165-LF3V	20 MHz	3.0 to 3.6 V	TQFP-100

1) This Data Sheet is valid for devices starting with and including design step HA.

For simplicity all versions are referred to by the term **C165** throughout this document.

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the C165 please refer to the “**Product Catalog Microcontrollers**”, which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
$\overline{\text{RSTIN}}$	79	81	I/O	Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the C165. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}. A spike filter suppresses input pulses < 10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. In bidirectional reset mode (enabled by setting bit BDRSTEN in register SYSCON) the $\overline{\text{RSTIN}}$ line is internally pulled low for the duration of the internal reset sequence upon any reset (HW, SW, WDT). See note below this table. *Note: To let the reset configuration of PORT0 settle a reset duration of ca. 1 ms is recommended.*
$\overline{\text{RSTOUT}}$	80	82	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{NMI}}$	81	83	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the C165 to go into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
V_{DD}	7, 28, 38, 49, 69, 78	9, 30, 40, 51, 71, 80	–	Digital Supply Voltage: + 5 V or + 3 V during normal operation and idle mode. ≥ 2.5 V during power down mode.
V_{SS}	4, 27, 39, 50, 70, 77	6, 29, 41, 52, 72, 79	–	Digital Ground.

Note: The following behavioural differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated like on a hardware reset. Especially the bootstrap loader may be activated when P0L.4 is low.
- Pin $\overline{\text{RSTIN}}$ may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.

Memory Organization

The memory space of the C165 is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 MBytes. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bitaddressable.

The C165 is prepared to incorporate on-chip program memory (not in the ROM-less derivatives, of course) for code or constant data. The internal ROM area can be mapped either to segment 0 or segment 1.

2 KBytes of on-chip Internal RAM (IRAM) are provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2×512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the C166 Family.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16 MBytes of external RAM and/or ROM can be connected to the microcontroller.

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

– 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
– 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
– 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
– 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/ output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.
In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. The C165 offers the possibility to switch the $\overline{CS}$ outputs to an unlatched mode. In this mode the internal filter logic is switched off and the $\overline{CS}$ signals are directly generated from the address. The unlatched $\overline{CS}$ mode is enabled by setting CSCFG (SYSCON.6).

Access to very slow memories or memories with varying access times is supported via a particular ‘Ready’ function.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration and allows to share external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7 … P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to ‘1’ the Slave Mode is selected where pin $\overline{HLDA}$ is switched to input. This allows to directly connect the slave controller to another master controller without glue logic.

For applications which require less than 16 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte, or to 64 KByte. In this case Port 4 outputs four, two, or no address lines at all. It outputs all 8 address lines, if an address space of 16 MBytes is used.

Table 3 C165 Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
External Interrupt 0	CC8IR	CC8IE	CC8INT	$00'0060_H$	18_H
External Interrupt 1	CC9IR	CC9IE	CC9INT	$00'0064_H$	19_H
External Interrupt 2	CC10IR	CC10IE	CC10INT	$00'0068_H$	$1A_H$
External Interrupt 3	CC11IR	CC11IE	CC11INT	$00'006C_H$	$1B_H$
External Interrupt 4	CC12IR	CC12IE	CC12INT	$00'0070_H$	$1C_H$
External Interrupt 5	CC13IR	CC13IE	CC13INT	$00'0074_H$	$1D_H$
External Interrupt 6	CC14IR	CC14IE	CC14INT	$00'0078_H$	$1E_H$
External Interrupt 7	CC15IR	CC15IE	CC15INT	$00'007C_H$	$1F_H$
GPT1 Timer 2	T2IR	T2IE	T2INT	$00'0088_H$	22_H
GPT1 Timer 3	T3IR	T3IE	T3INT	$00'008C_H$	23_H
GPT1 Timer 4	T4IR	T4IE	T4INT	$00'0090_H$	24_H
GPT2 Timer 5	T5IR	T5IE	T5INT	$00'0094_H$	25_H
GPT2 Timer 6	T6IR	T6IE	T6INT	$00'0098_H$	26_H
GPT2 CAPREL Reg.	CRIR	CRIE	CRINT	$00'009C_H$	27_H
ASC0 Transmit	S0TIR	S0TIE	S0TINT	$00'00A8_H$	$2A_H$
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	$00'011C_H$	47_H
ASC0 Receive	S0RIR	S0RIE	S0RINT	$00'00AC_H$	$2B_H$
ASC0 Error	S0EIR	S0EIE	S0EINT	$00'00B0_H$	$2C_H$
SSC Transmit	SCTIR	SCTIE	SCTINT	$00'00B4_H$	$2D_H$
SSC Receive	SCRIR	SCRIE	SCRINT	$00'00B8_H$	$2E_H$
SSC Error	SCEIR	SCEIE	SCEINT	$00'00BC_H$	$2F_H$
Unassigned node	XP0IR	XP0IE	XP0INT	$00'0100_H$	40_H
Unassigned node	XP1IR	XP1IE	XP1INT	$00'0104_H$	41_H
Unassigned node	XP2IR	XP2IE	XP2INT	$00'0108_H$	42_H
Unassigned node	XP3IR	XP3IE	XP3INT	$00'010C_H$	43_H
Unassigned node	CC29IR	CC29IE	CC29INT	$00'0110_H$	44_H
Unassigned node	CC30IR	CC30IE	CC30INT	$00'0114_H$	45_H
Unassigned node	CC31IR	CC31IE	CC31INT	$00'0118_H$	46_H

The C165 also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 4 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 4 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions: – Hardware Reset – Software Reset – W-dog Timer Overflow	–	 RESET RESET RESET	 $00'0000_H$ $00'0000_H$ $00'0000_H$	 00_H 00_H 00_H	 III III III
Class A Hardware Traps: – Non-Maskable Interrupt – Stack Overflow – Stack Underflow	 NMI STKOF STKUF	 NMITRAP STOTRAP STUTRAP	 $00'0008_H$ $00'0010_H$ $00'0018_H$	 02_H 04_H 06_H	 II II II
Class B Hardware Traps: – Undefined Opcode – Protected Instruction Fault – Illegal Word Operand Access – Illegal Instruction Access – Illegal External Bus Access	 UNDOPC PRTFLT ILLOPA ILLINA ILLBUS	 BTRAP BTRAP BTRAP BTRAP BTRAP	 $00'0028_H$ $00'0028_H$ $00'0028_H$ $00'0028_H$ $00'0028_H$	 $0A_H$ $0A_H$ $0A_H$ $0A_H$ $0A_H$	 I I I I I
Reserved	–	–	[$2C_H$ – $3C_H$]	[$0B_H$ – $0F_H$]	–
Software Traps – TRAP Instruction	–	–	Any [$00'0000_H$ – $00'01FC_H$] in steps of 4_H	Any [00_H – $7F_H$]	Current CPU Priority

Instruction Set Summary

Table 5 lists the instructions of the C165 in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **“C166 Family Instruction Set Manual”**.

This document also provides a detailed description of each instruction.

Table 5 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2

Special Function Registers Overview

The following table lists all SFRs which are implemented in the C165 in alphabetical order.
Bit-addressable SFRs are marked with the letter "**b**" in column "Name". SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter "**E**" in column "Physical Address". Registers within on-chip X-peripherals are marked with the letter "**X**" in column "Physical Address".

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Table 6 C165 Registers, Ordered by Name

Name	Physical Address	8-Bit Addr.	Description	Reset Value
ADDRSEL1	$FE18_H$	$0C_H$	Address Select Register 1	0000_H
ADDRSEL2	$FE1A_H$	$0D_H$	Address Select Register 2	0000_H
ADDRSEL3	$FE1C_H$	$0E_H$	Address Select Register 3	0000_H
ADDRSEL4	$FE1E_H$	$0F_H$	Address Select Register 4	0000_H
BUSCON0 b	$FF0C_H$	86_H	Bus Configuration Register 0	$0XX0_H$
BUSCON1 b	$FF14_H$	$8A_H$	Bus Configuration Register 1	0000_H
BUSCON2 b	$FF16_H$	$8B_H$	Bus Configuration Register 2	0000_H
BUSCON3 b	$FF18_H$	$8C_H$	Bus Configuration Register 3	0000_H
BUSCON4 b	$FF1A_H$	$8D_H$	Bus Configuration Register 4	0000_H
CAPREL	$FE4A_H$	25_H	GPT2 Capture/Reload Register	0000_H
CC10IC b	$FF8C_H$	$C6_H$	EX2IN Interrupt Control Register	0000_H
CC11IC b	$FF8E_H$	$C7_H$	EX3IN Interrupt Control Register	0000_H
CC12IC b	$FF90_H$	$C8_H$	EX4IN Interrupt Control Register	0000_H
CC13IC b	$FF92_H$	$C9_H$	EX5IN Interrupt Control Register	0000_H
CC14IC b	$FF94_H$	CA_H	EX6IN Interrupt Control Register	0000_H
CC15IC b	$FF96_H$	CB_H	EX7IN Interrupt Control Register	0000_H
CC29IC b	$F184_H$ **E**	$C2_H$	Software Interrupt Control Register	0000_H
CC30IC b	$F18C_H$ **E**	$C6_H$	Software Interrupt Control Register	0000_H
CC31IC b	$F194_H$ **E**	CA_H	Software Interrupt Control Register	0000_H
CC8IC b	$FF88_H$	$C4_H$	EX0IN Interrupt Control Register	0000_H
CC9IC b	$FF8A_H$	$C5_H$	EX1IN Interrupt Control Register	0000_H

DC Characteristics (Reduced Supply Voltage Range) (cont'd)
(Operating Conditions apply)[1)]

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
PORT0 configuration current[8)]	I_{P0H}[5)]	–	- 5	µA	$V_{IN} = V_{IHmin}$
	I_{P0L}[6)]	- 100	–	µA	$V_{IN} = V_{ILmax}$
XTAL1 input current	I_{IL} CC	–	± 20	µA	0 V < V_{IN} < V_{DD}
Pin capacitance[9)] (digital inputs/outputs)	C_{IO} CC	–	10	pF	f = 1 MHz T_A = 25 °C

1) Keeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current I_{OV}.

2) Valid in bidirectional reset mode only.

3) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

4) These parameters describe the $\overline{\text{RSTIN}}$ pullup, which equals a resistance of ca. 50 to 250 kΩ.

5) The maximum current may be drawn while the respective signal line remains inactive.

6) The minimum current must be drawn in order to drive the respective signal line active.

7) This specification is valid during Reset and during Hold-mode or Adapt-mode. During Hold-mode Port 6 pins are only affected, if they are used (configured) for $\overline{\text{CS}}$ output and the open drain function is not enabled. The $\overline{\text{READY}}$-pullup is always active, except for Powerdown mode.

8) This specification is valid during Reset and during Adapt-mode.

9) Not 100% tested, guaranteed by design and characterization.

AC Characteristics

Multiplexed Bus (Reduced Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 6 TCL + $2t_A + t_C + t_F$ (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	11 + t_A	–	TCL - 14 + t_A	–	ns
Address setup to ALE	t_6	CC	5 + t_A	–	TCL - 20 + t_A	–	ns
Address hold after ALE	t_7	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	- 10 + t_A	–	-10 + t_A	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_{10}	CC	–	6	–	6	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_{11}	CC	–	31	–	TCL + 6	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	34 + t_C	–	2TCL - 16 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	59 + t_C	–	3TCL - 16 +t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	22 + t_C	–	2TCL - 28 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	47 + t_C	–	3TCL - 28 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	45 + t_A + t_C	–	3TCL - 30 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	57 + $2t_A$ + t_C	–	4TCL - 43 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns

Multiplexed Bus (Reduced Supply Voltage Range) (cont'd)
(Operating Conditions apply)
ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
Data valid to $\overline{\text{WrCS}}$	t_{50}	CC	28 + t_C	–	2TCL - 22 + t_C	–	ns
Data hold after $\overline{\text{RdCS}}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{\text{RdCS}}$	t_{52}	SR	–	30 + t_F	–	2TCL - 20 + t_F	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{54}	CC	30 + t_F	–	2TCL - 20 + t_F	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{56}	CC	30 + t_F	–	2TCL - 20 + t_F	–	ns

1) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

AC Characteristics

Demultiplexed Bus (Standard Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 4 TCL + 2t_A + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6	CC	4 + t_A	–	TCL - 16 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	- 10 + t_A	–	- 10 + t_A	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	20 + t_C	–	2TCL - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	40 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	50 + 2t_A + t_C	–	4TCL - 30 + 2t_A + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay[1)])	t_{20}	SR	–	26 + 2t_A + t_F[1)]	–	2TCL - 14 + 22t_A + t_F[1)]	ns
Data float after $\overline{RD}$ rising edge (no RW-delay[1)])	t_{21}	SR	–	10 + 2t_A + t_F[1)]	–	TCL - 10 + 22t_A + t_F[1)]	ns

Demultiplexed Bus (Standard Supply Voltage Range) (cont'd)
(Operating Conditions apply)
ALE cycle time = 4 TCL + 2t_A + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
Data float after $\overline{\text{RdCS}}$ (with RW-delay)[1]	t_{53}	SR	–	20 + t_F	–	2TCL - 20 + 2t_A + t_F [1]	ns
Data float after $\overline{\text{RdCS}}$ (no RW-delay)[1]	t_{68}	SR	–	0 + t_F	–	TCL - 20 + 2t_A + t_F [1]	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{55}	CC	- 6 + t_F	–	- 6 + t_F	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{57}	CC	6 + t_F	–	TCL - 14 + t_F	–	ns

1) RW-delay and t_A refer to the next following bus cycle (including an access to an on-chip X-Peripheral).

2) Read data are latched with the same clock edge that triggers the address change and the rising $\overline{\text{RD}}$ edge. Therefore address changes before the end of $\overline{\text{RD}}$ have no impact on read cycles.

3) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

Demultiplexed Bus (Reduced Supply Voltage Range) (cont'd)
(Operating Conditions apply)
ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
Data float after $\overline{\text{RdCS}}$ (with RW-delay)[1]	t_{53}	SR	–	30 + t_F	–	2TCL - 20 + $2t_A$ + t_F [1]	ns
Data float after $\overline{\text{RdCS}}$ (no RW-delay)[1]	t_{68}	SR	–	5 + t_F	–	TCL - 20 + $2t_A$ + t_F [1]	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{55}	CC	- 16 + t_F	–	- 16 + t_F	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{57}	CC	9 + t_F	–	TCL - 16 + t_F	–	ns

1) RW-delay and t_A refer to the next following bus cycle (including an access to an on-chip X-Peripheral).

2) Read data are latched with the same clock edge that triggers the address change and the rising $\overline{\text{RD}}$ edge. Therefore address changes before the end of $\overline{\text{RD}}$ have no impact on read cycles.

3) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

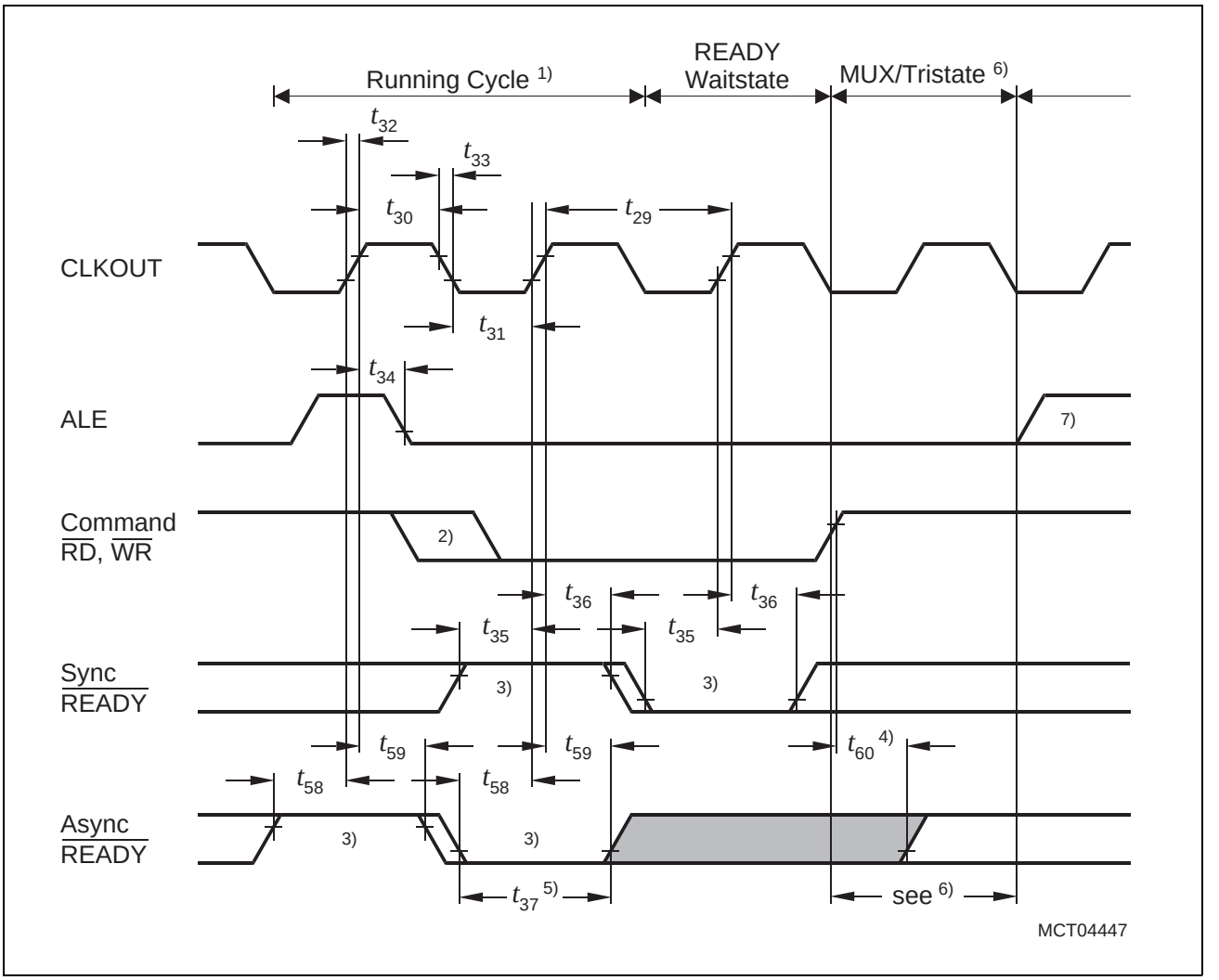


Figure 21 CLKOUT and READY

Notes

1) Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).
2) The leading edge of the respective command depends on RW-delay.
3) READY sampled HIGH at this sampling point generates a READY controlled waitstate, READY sampled LOW at this sampling point terminates the currently running bus cycle.
4) READY may be deactivated in response to the trailing (rising) edge of the corresponding command (RD or WR).
5) If the Asynchronous READY signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill t_{37} in order to be safely synchronized. This is guaranteed, if READY is removed in response to the command (see Note 4)).
6) Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here.
For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.
7) The next external bus cycle may start here.

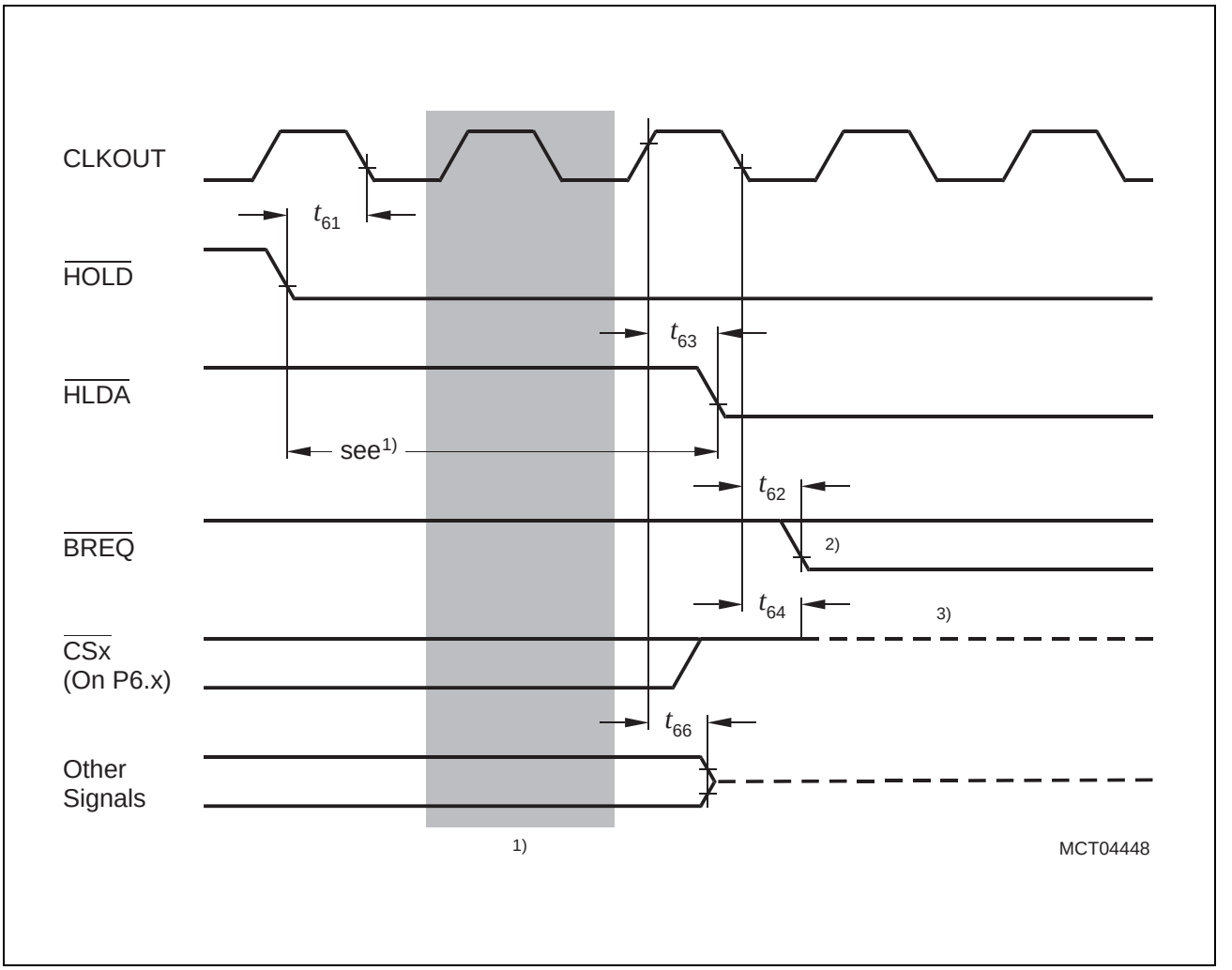


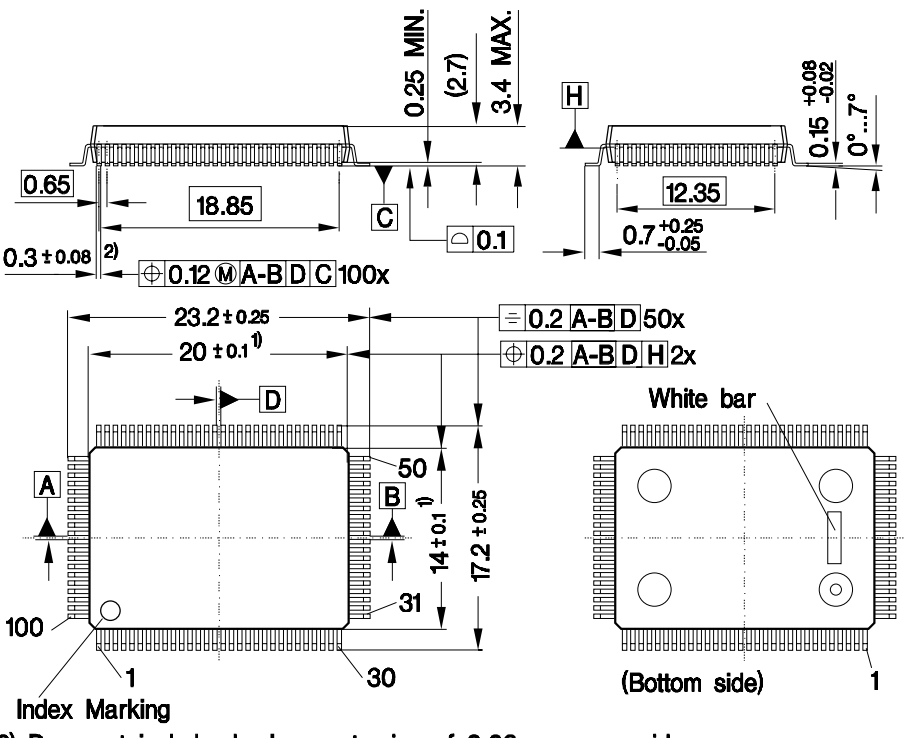
Figure 22 External Bus Arbitration, Releasing the Bus

Notes

1) The C165 will complete the currently running bus cycle before granting bus access.
2) This is the first possibility for $\overline{\text{BREQ}}$ to get active.
3) The $\overline{\text{CS}}$ outputs will be resistive high (pullup) after t_{64}.

Package Outlines

P-MQFP-100 (SMD)
(Plastic Metric Quad Flat Package)



2) Does not include dambar protrusion of 0.08 max. per side
1) Does not include plastic or metal protrusion of 0.25 max. per side

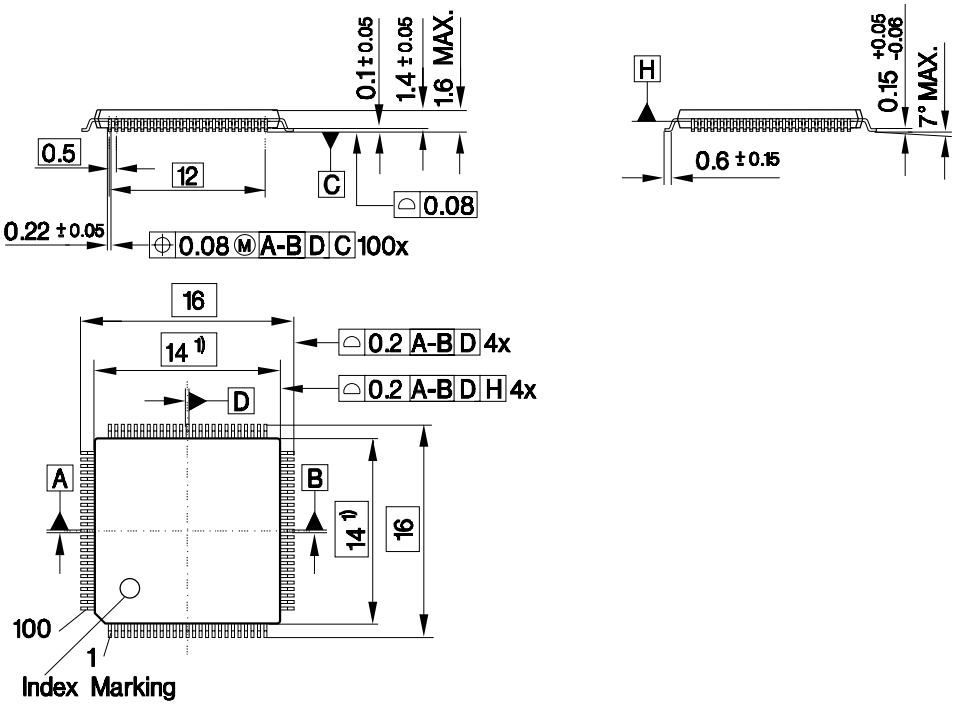
GPR05365

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

P-TQFP-100 (SMD)
(Plastic Thin Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPP05614

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm