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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	77
Program Memory Size	-
Program Memory Type	ROMIess
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	P-MQFP-100
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c165l25mhabxqma1

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External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

- 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
- 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/ output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.

In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Up to 5 external $\overline{\text{CS}}$ signals (4 windows plus default) can be generated in order to save external glue logic. The C165 offers the possibility to switch the $\overline{\text{CS}}$ outputs to an unlatched mode. In this mode the internal filter logic is switched off and the $\overline{\text{CS}}$ signals are directly generated from the address. The unlatched $\overline{\text{CS}}$ mode is enabled by setting CSCFG (SYSCON.6).

Access to very slow memories or memories with varying access times is supported via a particular 'Ready' function.

A HOLD/HLDA protocol is available for bus arbitration and allows to share external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7 ... P6.5 (BREQ, HLDA, HOLD) are automatically controlled by the EBC. In Master Mode (default after reset) the HLDA pin is an output. By setting bit DP6.7 to '1' the Slave Mode is selected where pin HLDA is switched to input. This allows to directly connect the slave controller to another master controller without glue logic.

For applications which require less than 16 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte, or to 64 KByte. In this case Port 4 outputs four, two, or no address lines at all. It outputs all 8 address lines, if an address space of 16 MBytes is used.



Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C165's instructions can be executed in just one machine cycle which requires 80 ns at 25 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16×16 bit multiplication in 5 cycles and a 32-/16 bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.



Figure 5

CPU Block Diagram



Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C165 is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C165 supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicity decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C165 has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

Table 3 shows all of the possible C165 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).



General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 16 TCL.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.





Figure 6 Block Diagram of GPT1

With its maximum resolution of 8 TCL, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock. The count direction (up/down) for each timer is programmable by software. Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5 and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the C165 to measure absolute time differences or to perform pulse multiplication without software overhead.



The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.







Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the RSTOUT pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided by 2/128. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 20 μ s and 336 ms can be monitored (@ 25 MHz).

The default Watchdog Timer interval after reset is 5.24 ms (@ 25 MHz).

Parallel Ports

The C165 provides up to 77 I/O lines which are organized into six input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of three I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A23/19/17 ... A16 in systems where segmentation is enabled to access more than 64 KBytes of memory. Port 6 provides optional chip select signals.

Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal BHE/WRH, and the system clock output CLKOUT.

Port 5 is used for timer control signals.



Table 6		C165 Reg	gist	ers, Oro	dered by Name (cont'd)	
Name		Physica Addres	al S	8-Bit Addr.	Description	Reset Value
СР		FE10 _H		08 _H	CPU Context Pointer Register	FC00 _H
CRIC	b	FF6A _H		B5 _H	GPT2 CAPREL Interrupt Ctrl. Reg.	0000 _H
CSP		FE08 _H		04 _H	CPU Code Seg. Pointer Reg. (read only)	0000 _H
DP0H	b	F102 _H	Ε	81 _H	P0H Direction Control Register	00 _H
DP0L	b	F100 _H	Ε	80 _H	P0L Direction Control Register	00 _H
DP1H	b	F106 _H	Ε	83 _H	P1H Direction Control Register	00 _H
DP1L	b	F104 _H	Ε	82 _H	P1L Direction Control Register	00 _H
DP2	b	FFC2 _H		E1 _H	Port 2 Direction Control Register	0000 _H
DP3	b	FFC6 _H		E3 _H	Port 3 Direction Control Register	0000 _H
DP4	b	FFCA _H		E5 _H	Port 4 Direction Control Register	00 _H
DP6	b	FFCE _H		E7 _H	Port 6 Direction Control Register	00 _H
DPP0		FE00 _H		00 _H	CPU Data Page Pointer 0 Reg. (10 bits)	0000 _H
DPP1		FE02 _H		01 _H	CPU Data Page Pointer 1 Reg. (10 bits)	0001 _H
DPP2		FE04 _H		02 _H	CPU Data Page Pointer 2 Reg. (10 bits)	0002 _H
DPP3		FE06 _H		03 _H	CPU Data Page Pointer 3 Reg. (10 bits)	0003 _H
EXICON	b	F1C0 _H	Ε	E0 _H	External Interrupt Control Register	0000 _H
IDCHIP		F07C _H	Ε	3E _H	Identifier	05XX _H
IDMANUF		F07E _H	Ε	3F _H	Identifier	1820 _H
IDMEM		F07A _H	Ε	3D _H	Identifier	0000 _H
IDMEM2		F076 _H	Ε	3B _H	Identifier	0000 _H
IDPROG		F078 _H	Ε	3C _H	Identifier	0000 _H
MDC	b	FF0E _H		87 _H	CPU Multiply Divide Control Register	0000 _H
MDH		FE0C _H		06 _H	CPU Multiply Divide Reg. – High Word	0000 _H
MDL		FE0E _H		07 _H	CPU Multiply Divide Reg. – Low Word	0000 _H
ODP2	b	F1C2 _H	Ε	E1 _H	Port 2 Open Drain Control Register	0000 _H
ODP3	b	F1C6 _H	Ε	E3 _H	Port 3 Open Drain Control Register	0000 _H
ODP6	b	F1CE _H	Ε	E7 _H	Port 6 Open Drain Control Register	00 _H
ONES	b	FF1E _H		8F _H	Constant Value 1's Register (read only)	FFFF _H

P0H

P0L

00_H

00_H

Port 0 High Reg. (Upper half of PORT0)

Port 0 Low Reg. (Lower half of PORT0)

81_H

80_H

FF02_H

 $FF00_{H}$

b

b



Table 6		C165 Regist	ers, Oro	dered by Name (cont'd)	
Name		Physical Address	8-Bit Addr.	Description	Reset Value
P1H	b	FF06 _H	83 _H	Port 1 High Reg. (Upper half of PORT1)	00 _H
P1L	b	FF04 _H	82 _H	Port 1 Low Reg.(Lower half of PORT1)	00 _H
P2	b	FFC0 _H	E0 _H	Port 2 Register	0000 _H
P3	b	FFC4 _H	E2 _H	Port 3 Register	0000 _H
P4	b	FFC8 _H	E4 _H	Port 4 Register (8 bits)	00 _H
P5	b	FFA2 _H	D1 _H	Port 5 Register (read only)	XXXX _H
P6	b	FFCC _H	E6 _H	Port 6 Register (8 bits)	00 _H
PECC0		FEC0 _H	60 _H	PEC Channel 0 Control Register	0000 _H
PECC1		FEC2 _H	61 _H	PEC Channel 1 Control Register	0000 _H
PECC2		FEC4 _H	62 _H	PEC Channel 2 Control Register	0000 _H
PECC3		FEC6 _H	63 _H	PEC Channel 3 Control Register	0000 _H
PECC4		FEC8 _H	64 _H	PEC Channel 4 Control Register	0000 _H
PECC5		FECA _H	65 _H	PEC Channel 5 Control Register	0000 _H
PECC6		FECCH	66 _H	PEC Channel 6 Control Register	0000 _H
PECC7		FECE _H	67 _H	PEC Channel 7 Control Register	0000 _H
PSW	b	FF10 _H	88 _H	CPU Program Status Word	0000 _H
RP0H	b	F108 _H E	84 _H	System Startup Config. Reg. (Rd. only)	XX _H
S0BG		FEB4 _H	5A _H	Serial Channel 0 Baud Rate Generator Reload Register	0000 _H
S0CON	b	FFB0 _H	D8 _H	Serial Channel 0 Control Register	0000 _H
S0EIC	b	FF70 _H	B8 _H	Serial Channel 0 Error Interrupt Ctrl. Reg	0000 _H
SORBUF		FEB2 _H	59 _H	Serial Channel 0 Receive Buffer Reg. (read only)	ХХ _Н
SORIC	b	FF6E _H	B7 _H	Serial Channel 0 Receive Interrupt Control Register	0000 _H
SOTBIC	b	F19C _H E	CEH	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000 _H
S0TBUF		FEB0 _H	58 _H	Serial Channel 0 Transmit Buffer Register (write only)	00 _H
SOTIC	b	FF6C _H	B6 _H	Serial Channel 0 Transmit Interrupt Control Register	0000 _H



Table 6		C165 Registers, Ordered by Name (contid)									
Name XP1IC b		Physical Address			Description	Reset Value					
		b F18E _H E C		C7 _H	Software Interrupt Control Register	0000 _H					
XP2IC	b	F196 _H	Ε	CB _H	Software Interrupt Control Register	0000 _H					
XP3IC	b	F19E _H	Ε	CF _H	Software Interrupt Control Register	0000 _H					
ZEROS	b	FF1C _H		8E _H	Constant Value 0's Register (read only)	0000 _H					

11 - IN ,

¹⁾ The system configuration is selected during reset.

 $^{\mbox{2)}}$ The reset value depends on the indicated reset source.



DC Characteristics (Standard Supply Voltage Range) (cont'd)

(Operating Conditions apply)¹⁾

Parameter	Symbol	Limit	Values	Unit	Test Condition	
		min.	max.			
RSTIN active current ⁴⁾	I _{RSTL} ⁶⁾	- 100	_	μA	$V_{\rm IN} = V_{\rm IL}$	
READY/RD/WR inact. current ⁷⁾	I _{RWH} ⁵⁾	-	- 40	μA	V_{OUT} = 2.4 V	
READY/RD/WR active current ⁷⁾	$I_{\rm RWL}^{6)}$	- 500	-	μA	$V_{OUT} = V_{OLmax}$	
ALE inactive current ⁷⁾	$I_{ALEL}^{(5)}$	-	40	μA	$V_{OUT} = V_{OLmax}$	
ALE active current ⁷⁾	I _{ALEH} ⁶⁾	500	_	μA	V_{OUT} = 2.4 V	
Port 6 inactive current ⁷⁾	I _{P6H} ⁵⁾	-	- 40	μA	V_{OUT} = 2.4 V	
Port 6 active current ⁷⁾	I _{P6L} ⁶⁾	- 500	_	μA	$V_{\rm OUT} = V_{\rm OL1max}$	
PORT0 configuration current ⁸⁾	I _{P0H} ⁵⁾	-	- 10	μA	$V_{\rm IN} = V_{\rm IHmin}$	
	$I_{P0L}^{6)}$	- 100	_	μA	$V_{\rm IN} = V_{\rm ILmax}$	
XTAL1 input current	I _{IL} CC	-	± 20	μA	$0 V < V_{IN} < V_{DD}$	
Pin capacitance ⁹⁾ (digital inputs/outputs)	C _{IO} CC	_	10	pF	f = 1 MHz $T_A = 25 \text{ °C}$	

¹⁾ Keeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current I_{OV} .

²⁾ Valid in bidirectional reset mode only.

- ³⁾ This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.
- ⁴⁾ These parameters describe the $\overline{\text{RSTIN}}$ pullup, which equals a resistance of ca. 50 to 250 k Ω .
- ⁵⁾ The maximum current may be drawn while the respective signal line remains inactive.
- ⁶⁾ The minimum current must be drawn in order to drive the respective signal line active.
- ⁷⁾ This specification is valid during Reset and during Hold-mode or Adapt-mode. During Hold-mode Port 6 pins are only affected, if they are used (configured) for CS output and the open drain function is not enabled. The READY-pullup is always active, except for Powerdown mode.
- ⁸⁾ This specification is valid during Reset and during Adapt-mode.
- ⁹⁾ Not 100% tested, guaranteed by design and characterization.



Power Consumption C165 (Standard Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol	Lim	it Values	Unit	Test Condition
		min.	max.		
Power supply current (active) with all peripherals active	I _{DD5}	_	15 + 1.8 × <i>f</i> _{CPU}	mA	$\frac{\text{RSTIN} = V_{\text{IL}}}{f_{\text{CPU}} \text{ in [MHz]}^{1)}}$
Idle mode supply current with all peripherals active	I _{IDX5}	_	2 + 0.4 × f _{CPU}	mA	$\overline{\text{RSTIN}} = V_{\text{IH1}}$ $f_{\text{CPU}} \text{ in [MHz]}^{1)}$
Power-down mode supply current	I _{PDO5}	_	50	μA	$V_{\rm DD} = V_{\rm DDmax}^{2)}$

¹⁾ The supply current is a function of the operating frequency. This dependency is illustrated in Figure 8. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

²⁾ This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD} , all outputs (including pins configured as outputs) disconnected.

Power Consumption C165 (Reduced Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol	Lim	it Values	Unit	Test Condition
		min.	max.		
Power supply current (active) with all peripherals active	I _{DD3}	_	3 + 1.3 × f _{CPU}	mA	$\overline{\text{RSTIN}} = V_{\text{IL}}$ $f_{\text{CPU}} \text{ in [MHz]}^{1)}$
Idle mode supply current with all peripherals active	I _{IDX3}	_	1 + 0.4 × f _{CPU}	mA	$\overline{\text{RSTIN}} = V_{\text{IH1}}$ $f_{\text{CPU}} \text{ in [MHz]}^{1)}$
Power-down mode supply current	I _{PDO3}	_	30	μA	$V_{\rm DD} = V_{\rm DDmax}^{2}$

¹⁾ The supply current is a function of the operating frequency. This dependency is illustrated in Figure 8. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

²⁾ This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD} , all outputs (including pins configured as outputs) disconnected.





Figure 10 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal, the oscillator frequency is limited to a range of 4 MHz to 40 MHz.

It is strongly recommended to measure the oscillation allowance (or margin) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.

When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is guaranteed by design only (not 100% tested).



Demultiplexed Bus (Standard Supply Voltage Range) (cont'd)

(Operating Conditions apply)

ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. Cl = 25	PU Clock 5 MHz	Variable (1 / 2TCL =	Unit	
			min.	max.	min.	max.	
Data valid to \overline{WR}	<i>t</i> ₂₂	CC	$20 + t_{\rm C}$	_	2TCL - 20	-	ns
					+ t _C		
Data hold after \overline{WR}	t ₂₄	CC	10 + <i>t</i> _F	_	TCL - 10 + <i>t</i> _F	_	ns
ALE rising edge after RD, WR	t ₂₆	CC	- 10 + <i>t</i> _F	_	- 10 + <i>t</i> _F	_	ns
Address hold after $\overline{WR}^{2)}$	t ₂₈	CC	$0 + t_{F}$	-	$0 + t_{F}$	-	ns
ALE falling edge to $\overline{CS}^{3)}$	t ₃₈	CC	- 4 - t _A	10 - <i>t</i> _A	- 4 - <i>t</i> _A	10 - <i>t</i> _A	ns
CS low to Valid Data In ³⁾	t ₃₉	SR	_	$40 + t_{C} + 2t_{A}$	-	3TCL - 20 + <i>t</i> _C + 2 <i>t</i> _A	ns
$\overline{\text{CS}}$ hold after $\overline{\text{RD}}$, $\overline{\text{WR}}^{3)}$	<i>t</i> ₄₁	CC	6 + <i>t</i> _F	_	TCL - 14 + <i>t</i> _F	_	ns
ALE falling edge to RdCS, WrCS (with RW- delay)	t ₄₂	CC	16 + <i>t</i> _A	-	TCL - 4 + <i>t</i> _A	-	ns
ALE falling edge to RdCS, WrCS (no RW- delay)	t ₄₃	CC	$-4 + t_{A}$	_	-4 + t_A	_	ns
RdCS to Valid Data In (with RW-delay)	t ₄₆	SR	_	16 + <i>t</i> _C	-	2TCL - 24 + <i>t</i> _C	ns
RdCS to Valid Data In (no RW-delay)	t ₄₇	SR	_	$36 + t_{\rm C}$	-	3TCL - 24 + <i>t</i> _C	ns
RdCS, WrCS Low Time (with RW-delay)	t ₄₈	CC	30 + <i>t</i> _C	-	2TCL - 10 + <i>t</i> _C	-	ns
RdCS, WrCS Low Time (no RW-delay)	t ₄₉	CC	$50 + t_{\rm C}$	-	3TCL - 10 + <i>t</i> _C	-	ns
Data valid to WrCS	t ₅₀	CC	$26 + t_{\rm C}$	_	2TCL - 14 + <i>t</i> _C	_	ns
Data hold after RdCS	t ₅₁	SR	0	_	0	_	ns



Demultiplexed Bus (Reduced Supply Voltage Range) (cont'd)

(Operating Conditions apply)

ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. Cl = 20	PU Clock) MHz	Variable (1 / 2TCL =	Unit	
			min.	max.	min.	max.	
Data valid to \overline{WR}	t ₂₂	CC	$24 + t_{C}$	-	2TCL - 26	_	ns
					+ t _C		
Data hold after \overline{WR}	t ₂₄	CC	15 + <i>t</i> _F	_	TCL - 10 + <i>t</i> _F	_	ns
ALE rising edge after RD, WR	t ₂₆	CC	- 12 + <i>t</i> _F	-	- 12 + <i>t</i> _F	_	ns
Address hold after $\overline{WR}^{2)}$	t ₂₈	CC	$0 + t_{F}$	-	0 + <i>t</i> _F	_	ns
ALE falling edge to $\overline{CS}^{3)}$	t ₃₈	CC	- 8 - <i>t</i> _A	10 - <i>t</i> _A	- 8 - <i>t</i> _A	10 - <i>t</i> _A	ns
CS low to Valid Data In ³⁾	t ₃₉	SR	_	$47 + t_{C} + 2t_{A}$	_	3TCL - 28 + <i>t</i> _C + 2 <i>t</i> _A	ns
$\overline{\text{CS}}$ hold after $\overline{\text{RD}}$, $\overline{\text{WR}}^{3)}$	<i>t</i> ₄₁	CC	9 + t _F	_	TCL - 16 + <i>t</i> _F	_	ns
ALE falling edge to RdCS, WrCS (with RW- delay)	t ₄₂	CC	19 + <i>t</i> _A	-	TCL - 6 + <i>t</i> _A	-	ns
ALE falling edge to RdCS, WrCS (no RW- delay)	t ₄₃	CC	$-6 + t_{A}$	-	- 6 + <i>t</i> _A	-	ns
RdCS to Valid Data In (with RW-delay)	t ₄₆	SR	_	$20 + t_{\rm C}$	_	2TCL - 30 + <i>t</i> _C	ns
RdCS to Valid Data In (no RW-delay)	t ₄₇	SR	_	45 + t _C	_	3TCL - 30 + <i>t</i> _C	ns
RdCS, WrCS Low Time (with RW-delay)	t ₄₈	CC	38 + t _C	_	2TCL - 12 + <i>t</i> _C	_	ns
RdCS, WrCS Low Time (no RW-delay)	t ₄₉	CC	$63 + t_{\rm C}$	_	3TCL - 12 + <i>t</i> _C	_	ns
Data valid to WrCS	t ₅₀	CC	28 + <i>t</i> _C	_	2TCL - 22 + <i>t</i> _C	_	ns
Data hold after RdCS	t ₅₁	SR	0	-	0	-	ns





Figure 17 External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Normal ALE





Figure 18 External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Extended ALE





Figure 19 External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Normal ALE



Package Outlines



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Infineon goes for Business Excellence

"Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.

Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction."

Dr. Ulrich Schumacher

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