Infineon Technologies - C165L25MHAFXQMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	77
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	P-MQFP-100
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c165l25mhafxqma1

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
P4			IO	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines:
P4.0	23	25	O	A16 Least Significant Segment Address Line
P4.1	24	26	O	A17 Segment Address Line
P4.2	25	27	O	A18 Segment Address Line
P4.3	26	28	O	A19 Segment Address Line
P4.4	29	31	O	A20 Segment Address Line
P4.5	30	32	O	A21 Segment Address Line
P4.6	31	33	O	A22 Segment Address Line
P4.7	32	34	O	A23 Most Significant Segment Address Line
$\overline{RD}$	33	35	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
$\overline{WR}$/ $\overline{WRL}$	34	36	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{READY}$	35	37	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle waitstates until the pin returns to a low level. An internal pullup device holds this pin high when nothing is driving it.
ALE	36	38	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
$\overline{EA}$	37	39	I	External Access Enable pin. A low level at this pin during and after Reset forces the C165 to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
NC	40	42	–	This pin is not connected in the C165. No connection to the PCB is required.
PORT0 P0L.0-7 P0H.0-7	 41-48 51-58	 43-50 53-60	IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: D0 – D7 D0 – D7 P0H.0 – P0H.7: I/O D8 – D15 **Multiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: AD0 – AD7 AD0 – AD7 P0H.0 – P0H.7: A8 – A15 AD8 – AD15
PORT1 P1L.0-7 P1H.0-7	 59-66 67,68, 71-76	 61-68 69-70, 73-78	IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode.

Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C165 is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C165 supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicity decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C165 has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Table 3 shows all of the possible C165 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

The C165 also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 4 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 4 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions: – Hardware Reset – Software Reset – W-dog Timer Overflow	–	 RESET RESET RESET	 $00'0000_H$ $00'0000_H$ $00'0000_H$	 00_H 00_H 00_H	 III III III
Class A Hardware Traps: – Non-Maskable Interrupt – Stack Overflow – Stack Underflow	 NMI STKOF STKUF	 NMITRAP STOTRAP STUTRAP	 $00'0008_H$ $00'0010_H$ $00'0018_H$	 02_H 04_H 06_H	 II II II
Class B Hardware Traps: – Undefined Opcode – Protected Instruction Fault – Illegal Word Operand Access – Illegal Instruction Access – Illegal External Bus Access	 UNDOPC PRTFLT ILLOPA ILLINA ILLBUS	 BTRAP BTRAP BTRAP BTRAP BTRAP	 $00'0028_H$ $00'0028_H$ $00'0028_H$ $00'0028_H$ $00'0028_H$	 $0A_H$ $0A_H$ $0A_H$ $0A_H$ $0A_H$	 I I I I I
Reserved	–	–	[$2C_H$ – $3C_H$]	[$0B_H$ – $0F_H$]	–
Software Traps – TRAP Instruction	–	–	Any [$00'0000_H$ – $00'01FC_H$] in steps of 4_H	Any [00_H – $7F_H$]	Current CPU Priority

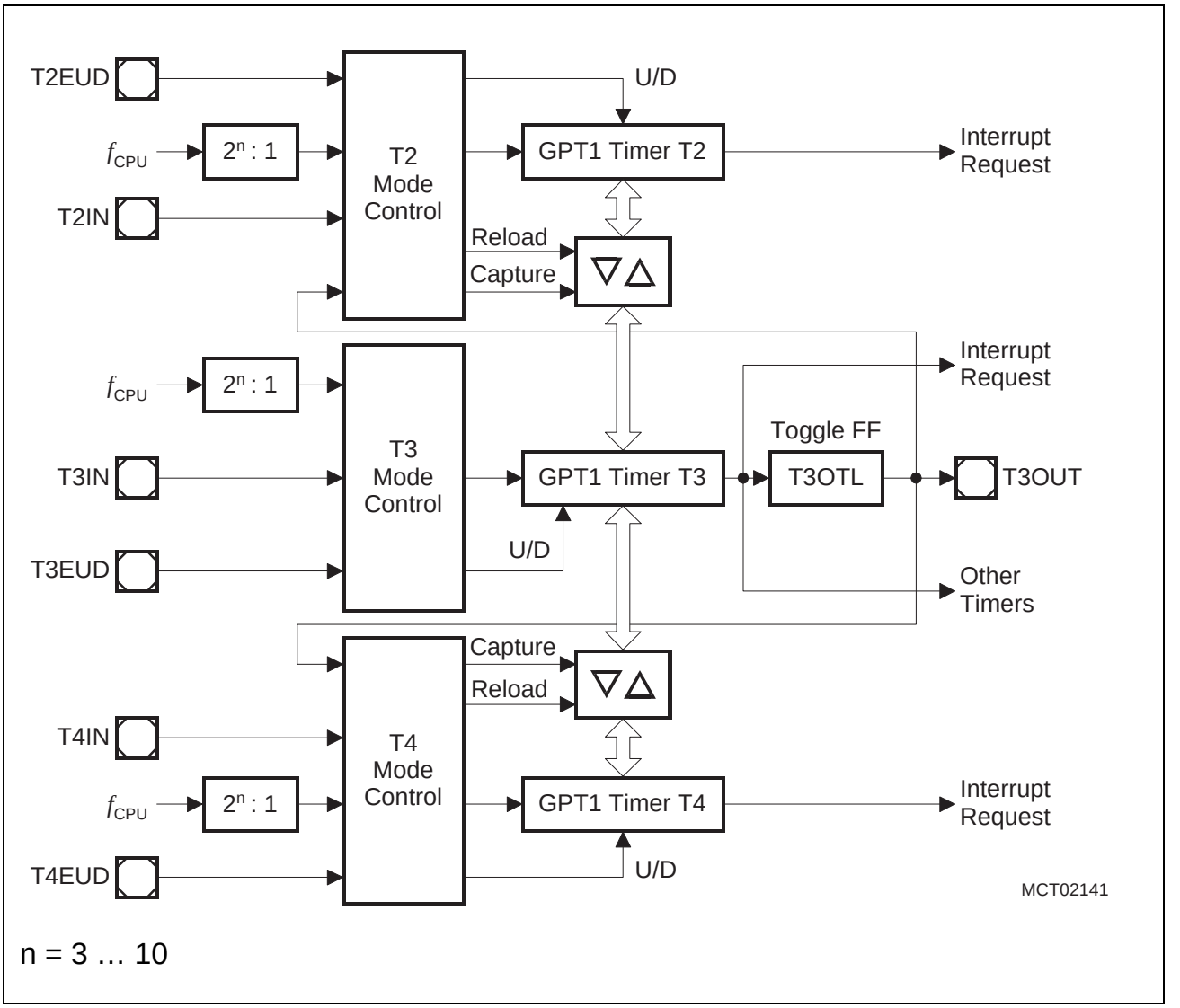


Figure 6 Block Diagram of GPT1

With its maximum resolution of 8 TCL, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock. The count direction (up/down) for each timer is programmable by software. Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5 and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the C165 to measure absolute time differences or to perform pulse multiplication without software overhead.

Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided by 2/128. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 20 µs and 336 ms can be monitored (@ 25 MHz).
The default Watchdog Timer interval after reset is 5.24 ms (@ 25 MHz).

Parallel Ports

The C165 provides up to 77 I/O lines which are organized into six input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of three I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A23/19/17 … A16 in systems where segmentation is enabled to access more than 64 KBytes of memory.
Port 6 provides optional chip select signals.
Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal $\overline{\text{BHE}}$/$\overline{\text{WRH}}$, and the system clock output CLKOUT.
Port 5 is used for timer control signals.

Instruction Set Summary

Table 5 lists the instructions of the C165 in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **“C166 Family Instruction Set Manual”**.

This document also provides a detailed description of each instruction.

Table 5 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2

Table 6 C165 Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
XP1IC	**b**	$F18E_H$	**E**	$C7_H$	Software Interrupt Control Register	0000_H
XP2IC	**b**	$F196_H$	**E**	CB_H	Software Interrupt Control Register	0000_H
XP3IC	**b**	$F19E_H$	**E**	CF_H	Software Interrupt Control Register	0000_H
ZEROS	**b**	$FF1C_H$		$8E_H$	Constant Value 0's Register (read only)	0000_H

1) The system configuration is selected during reset.

2) The reset value depends on the indicated reset source.

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C165. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 8 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Standard digital supply voltage (5 V versions)	V_{DD}	4.5	5.5	V	Active mode, f_{CPUmax} = 25 MHz
		2.5[1]	5.5	V	PowerDown mode
Reduced digital supply voltage (3 V versions)	V_{DD}	3.0	3.6	V	Active mode, f_{CPUmax} = 20 MHz
		2.5[1]	3.6	V	PowerDown mode
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	–	± 5	mA	Per pin[2)3)]
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	–	50	mA	[3)]
External Load Capacitance	C_L	–	100	pF	–
Ambient temperature	T_A	0	70	°C	SAB-C165 …
		- 40	85	°C	SAF-C165 …
		- 40	125	°C	SAK-C165 …

1) Output voltages and output currents will be reduced when V_{DD} leaves the range defined for active mode.

2) Overload conditions occur if the standard operatings conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$ + 0.5 V or $V_{OV} < V_{SS}$ – 0.5 V). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltage must remain within the specified limits. Proper operation is not guaranteed if overload conditions occur on functional pins such as XTAL1, $\overline{RD}$, $\overline{WR}$, etc.

3) Not 100% tested, guaranteed by design and characterization.

DC Characteristics (Reduced Supply Voltage Range)

(Operating Conditions apply)[1)]

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (TTL, all except XTAL1)	V_{IL} SR	- 0.5	0.8	V	–
Input low voltage XTAL1	V_{IL2} SR	- 0.5	0.3 V_{DD}	V	–
Input high voltage (TTL, all except $\overline{\text{RSTIN}}$ and XTAL1)	V_{IH} SR	1.8	V_{DD} + 0.5	V	–
Input high voltage $\overline{\text{RSTIN}}$ (when operated as input)	V_{IH1} SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage XTAL1	V_{IH2} SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Output low voltage (PORT0, PORT1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, $\overline{\text{RSTOUT}}$, $\overline{\text{RSTIN}}$[2)])	V_{OL} CC	–	0.45	V	I_{OL} = 1.6 mA
Output low voltage (all other outputs)	V_{OL1} CC	–	0.45	V	I_{OL} = 1.0 mA
Output high voltage[3)] (PORT0, PORT1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, $\overline{\text{RSTOUT}}$)	V_{OH} CC	0.9 V_{DD}	–	V	I_{OH} = - 0.5 mA
Output high voltage[3)] (all other outputs)	V_{OH1} CC	0.9 V_{DD}	–	V	I_{OH} = - 0.25 mA
Input leakage current (Port 5)	I_{OZ1} CC	–	± 200	nA	0 V < V_{IN} < V_{DD}
Input leakage current (all other)	I_{OZ2} CC	–	± 500	nA	0.45 V < V_{IN} < V_{DD}
$\overline{\text{RSTIN}}$ inactive current[4)]	I_{RSTH}[5)]	–	- 10	µA	V_{IN} = V_{IH1}
$\overline{\text{RSTIN}}$ active current[4)]	I_{RSTL}[6)]	- 100	–	µA	V_{IN} = V_{IL}
$\overline{\text{READY}}$/$\overline{\text{RD}}$/$\overline{\text{WR}}$ inact. current[7)]	I_{RWH}[5)]	–	- 10	µA	V_{OUT} = 2.4 V
$\overline{\text{READY}}$/$\overline{\text{RD}}$/$\overline{\text{WR}}$ active current[7)]	I_{RWL}[6)]	- 500	–	µA	V_{OUT} = V_{OLmax}
ALE inactive current[7)]	I_{ALEL}[5)]	–	20	µA	V_{OUT} = V_{OLmax}
ALE active current[7)]	I_{ALEH}[6)]	500	–	µA	V_{OUT} = 2.4 V
Port 6 inactive current[7)]	I_{P6H}[5)]	–	- 10	µA	V_{OUT} = 2.4 V
Port 6 active current[7)]	I_{P6L}[6)]	- 500	–	µA	V_{OUT} = V_{OL1max}

Power Consumption C165 (Standard Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD5}	–	$15 + 1.8 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IL}$ f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals active	I_{IDX5}	–	$2 + 0.4 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IH1}$ f_{CPU} in [MHz][1]
Power-down mode supply current	I_{PDO5}	–	50	µA	$V_{DD} = V_{DDmax}$[2]

1) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 8**. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

2) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD}, all outputs (including pins configured as outputs) disconnected.

Power Consumption C165 (Reduced Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD3}	–	$3 + 1.3 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IL}$ f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals active	I_{IDX3}	–	$1 + 0.4 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IH1}$ f_{CPU} in [MHz][1]
Power-down mode supply current	I_{PDO3}	–	30	µA	$V_{DD} = V_{DDmax}$[2]

1) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 8**. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

2) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD}, all outputs (including pins configured as outputs) disconnected.

AC Characteristics

Table 10 External Clock Drive XTAL1 (Standard Supply Voltage Range)
(Operating Conditions apply)

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		Unit
			min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	40	–	20	–	ns
High time[1]	t_1	SR	20[2]	–	6	–	ns
Low time[1]	t_2	SR	20[2]	–	6	–	ns
Rise time[1]	t_3	SR	–	10	–	6	ns
Fall time[1]	t_4	SR	–	10	–	6	ns

1) The clock input signal must reach the defined levels V_{IL2} and V_{IH2}.

2) The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

Table 11 External Clock Drive XTAL1 (Reduced Supply Voltage Range)
(Operating Conditions apply)

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		Unit
			min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	50	–	25	–	ns
High time[1]	t_1	SR	25[2]	–	8	–	ns
Low time[1]	t_2	SR	25[2]	–	8	–	ns
Rise time[1]	t_3	SR	–	10	–	6	ns
Fall time[1]	t_4	SR	–	10	–	6	ns

1) The clock input signal must reach the defined levels V_{IL2} and V_{IH2}.

2) The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

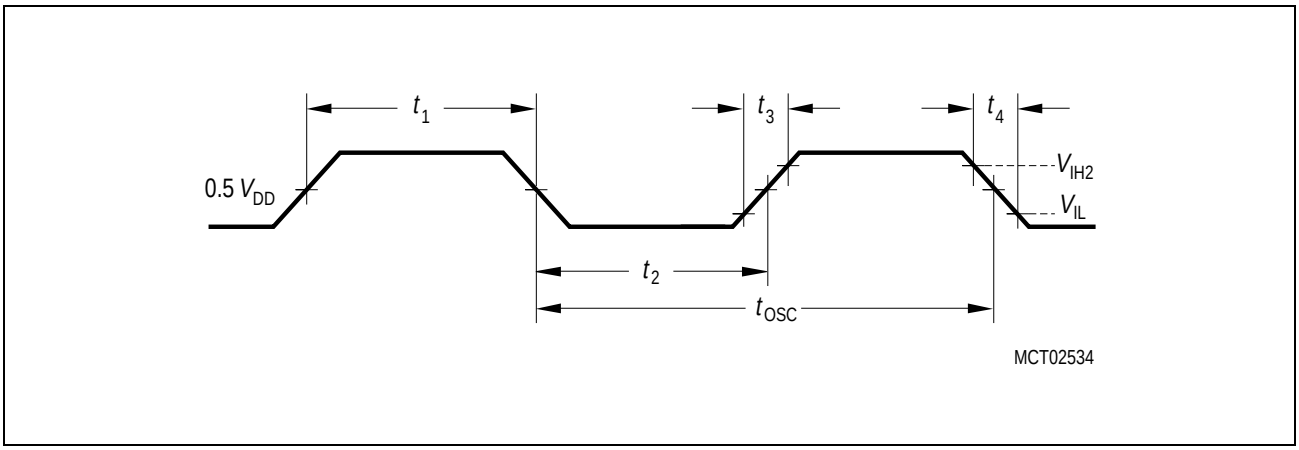


Figure 10 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal, the oscillator frequency is limited to a range of 4 MHz to 40 MHz.
It is strongly recommended to measure the oscillation allowance (or margin) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.
When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is guaranteed by design only (not 100% tested).

Multiplexed Bus (Standard Supply Voltage Range) (cont'd)
(Operating Conditions apply)
ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	20 + t_C	–	2TCL - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	40 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	50 + $2t_A$ + t_C	–	4TCL - 30 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$	t_{19}	SR	–	26 + t_F	–	2TCL - 14 + t_F	ns
Data valid to $\overline{WR}$	t_{22}	CC	20 + t_C	–	2TCL - 20 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{CS}$[1)]	t_{38}	CC	- 4 - t_A	10 - t_A	- 4 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In[1)]	t_{39}	SR	–	40 + t_C+$2t_A$	–	3TCL - 20 + t_C + $2t_A$	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$[1)]	t_{40}	CC	46 + t_F	–	3TCL - 14 + t_F	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{42}	CC	16 + t_A	–	TCL - 4 + t_A	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{43}	CC	- 4 + t_A	–	- 4 + t_A	–	ns

Multiplexed Bus (Reduced Supply Voltage Range) (cont'd)
(Operating Conditions apply)
ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
Data float after $\overline{RD}$	t_{19}	SR	–	36 + t_F	–	2TCL - 14 + t_F	ns
Data valid to $\overline{WR}$	t_{22}	CC	24 + t_C	–	2TCL - 26 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23}	CC	36 + t_F	–	2TCL - 14 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25}	CC	36 + t_F	–	2TCL - 14 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27}	CC	36 + t_F	–	2TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{CS}$[1)]	t_{38}	CC	- 8 - t_A	10 - t_A	- 8 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In[1)]	t_{39}	SR	–	47+ t_C + $2t_A$	–	3TCL - 28 + t_C + $2t_A$	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$[1)]	t_{40}	CC	57 + t_F	–	3TCL - 18 + t_F	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{42}	CC	19 + t_A	–	TCL - 6 + t_A	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{43}	CC	- 6 + t_A	–	- 6 + t_A	–	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{44}	CC	–	0	–	0	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{45}	CC	–	25	–	TCL	ns
$\overline{RdCS}$ to Valid Data In (with RW delay)	t_{46}	SR	–	20 + t_C	–	2TCL - 30 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW delay)	t_{47}	SR	–	45 + t_C	–	3TCL - 30 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay)	t_{48}	CC	38 + t_C	–	2TCL - 12 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay)	t_{49}	CC	63 + t_C	–	3TCL - 12 + t_C	–	ns

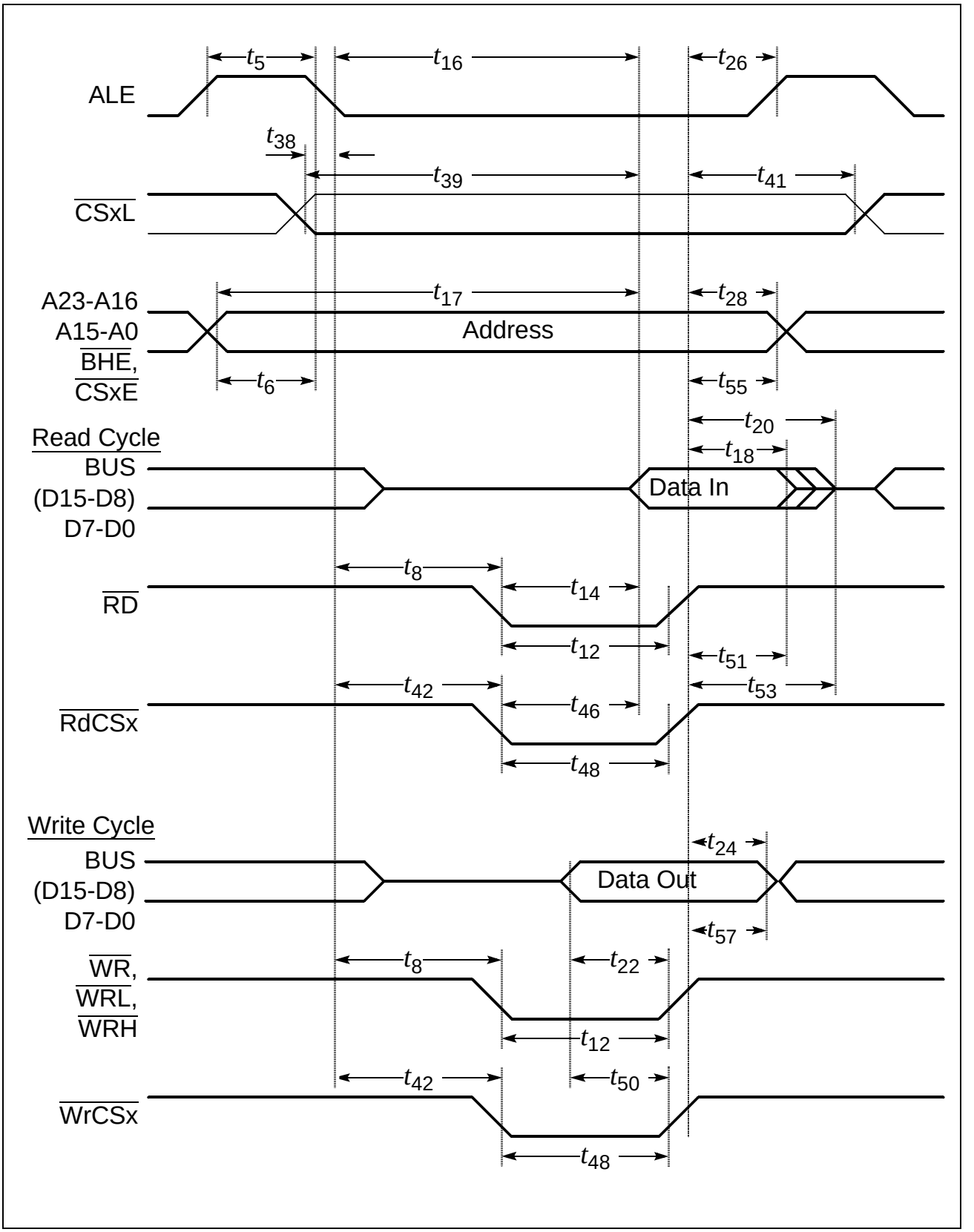


Figure 18 External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Extended ALE

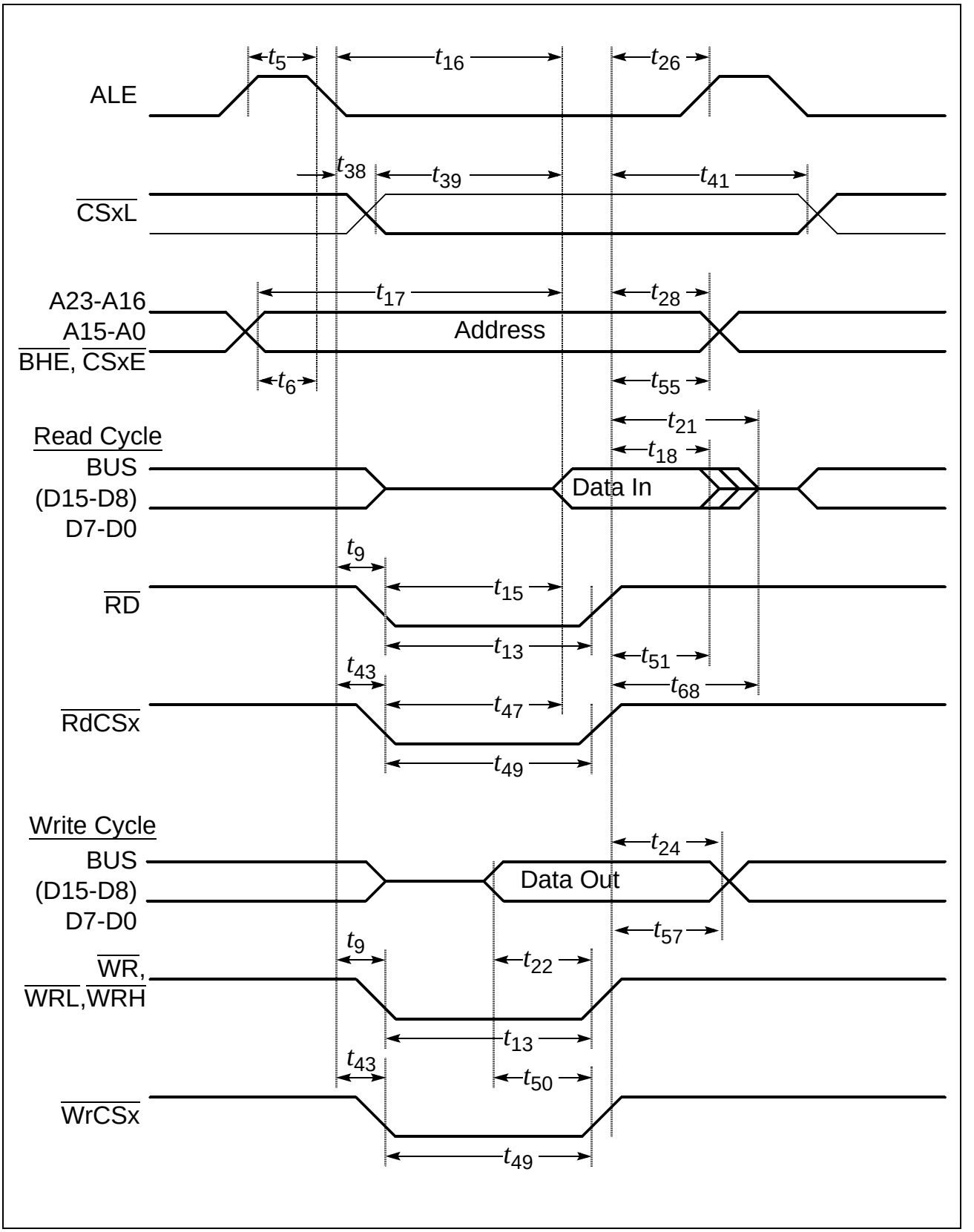


Figure 19 External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Normal ALE

AC Characteristics

CLKOUT and $\overline{\text{READY}}$ (Reduced Supply Voltage)

(Operating Conditions apply)

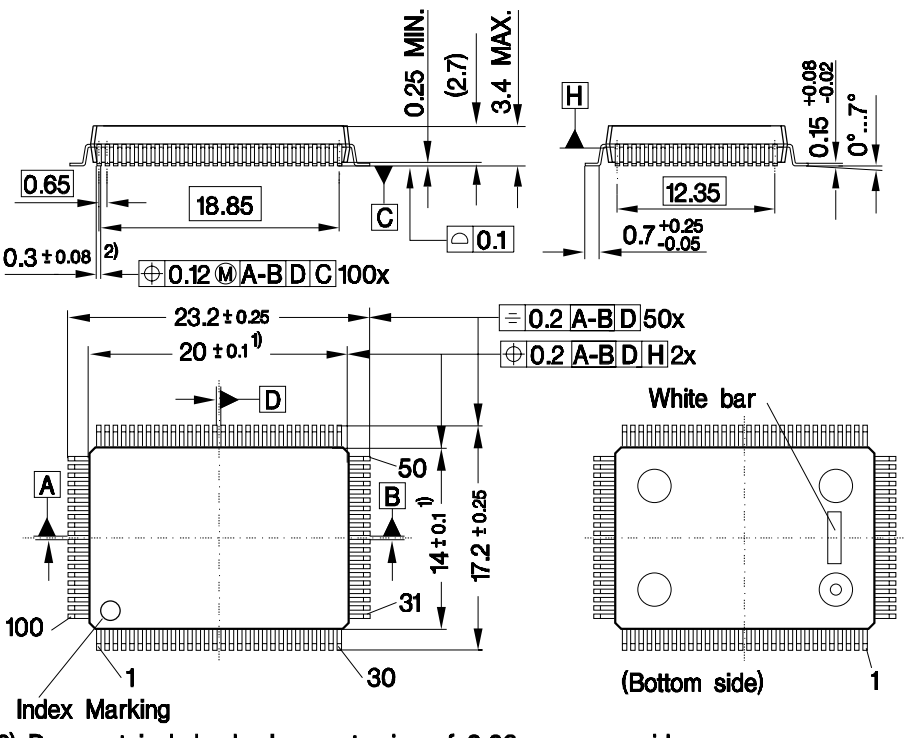
Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
CLKOUT cycle time	t_{29}	CC	50	50	2TCL	2TCL	ns
CLKOUT high time	t_{30}	CC	15	–	TCL - 10	–	ns
CLKOUT low time	t_{31}	CC	13	–	TCL - 12	–	ns
CLKOUT rise time	t_{32}	CC	–	12	–	12	ns
CLKOUT fall time	t_{33}	CC	–	8	–	8	ns
CLKOUT rising edge to ALE falling edge	t_{34}	CC	$0 + t_A$	$8 + t_A$	$0 + t_A$	$8 + t_A$	ns
Synchronous $\overline{\text{READY}}$ setup time to CLKOUT	t_{35}	SR	18	–	18	–	ns
Synchronous $\overline{\text{READY}}$ hold time after CLKOUT	t_{36}	SR	4	–	4	–	ns
Asynchronous $\overline{\text{READY}}$ low time	t_{37}	SR	68	–	$2TCL + t_{58}$	–	ns
Asynchronous $\overline{\text{READY}}$ setup time[1)]	t_{58}	SR	18	–	18	–	ns
Asynchronous $\overline{\text{READY}}$ hold time[1)]	t_{59}	SR	4	–	4	–	ns
Async. $\overline{\text{READY}}$ hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demultiplexed Bus)[2)]	t_{60}	SR	0	$0 + 2t_A + t_C + t_F$[2)]	0	$TCL - 25 + 2t_A + t_C + t_F$[2)]	ns

1) These timings are given for test purposes only, in order to assure recognition at a specific clock edge.

2) Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating $\overline{\text{READY}}$.
The $2t_A$ and t_C refer to the next following bus cycle, t_F refers to the current bus cycle.
The maximum limit for t_{60} must be fulfilled if the next following bus cycle is $\overline{\text{READY}}$ controlled.

Package Outlines

P-MQFP-100 (SMD)
(Plastic Metric Quad Flat Package)



2) Does not include dambar protrusion of 0.08 max. per side
1) Does not include plastic or metal protrusion of 0.25 max. per side

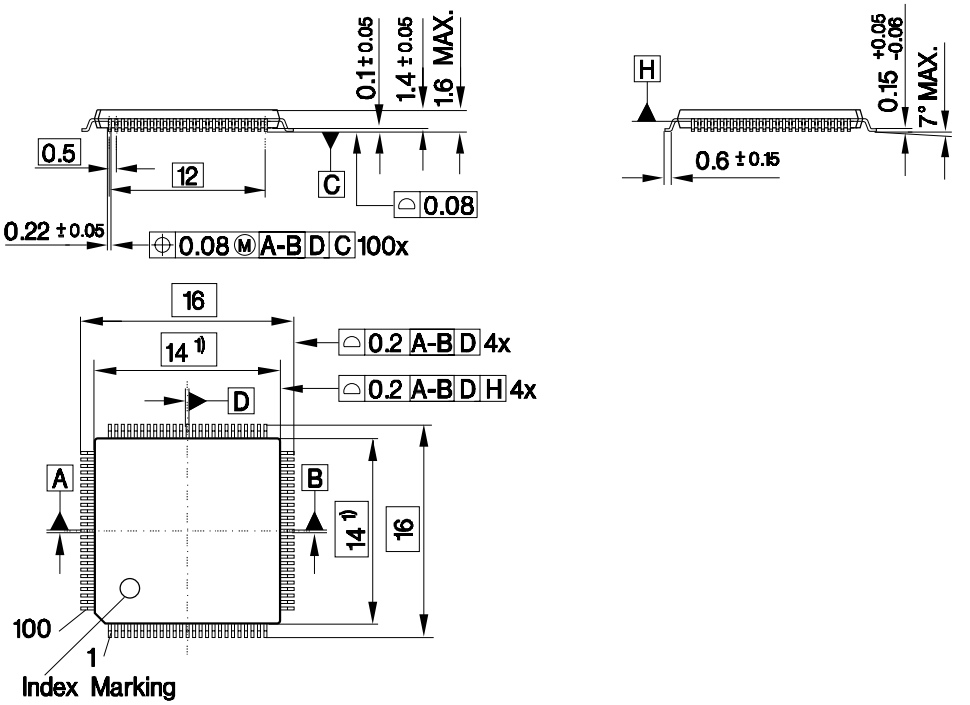
GPR05365

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

P-TQFP-100 (SMD)
(Plastic Thin Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPP05614

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm