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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	77
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	PG-TQFP-100
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c165lfhabxuma1

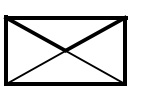
Revision History:	**2000-12**	V2.0
Previous Version:	1998-12	Update 0.5µ technology
	01.96	3 Volt Addendum
	07.95	25 MHz Addendum
	09.94	Data Sheet

Page	**Subjects (major changes since last revision)**
All	Converted to Infineon layout
2	ROM derivatives removed, 25-MHz derivatives and 3 V derivatives included
6ff	Pin numbers for TQFP added
14	Address window arbitration and master/slave mode introduced
32	New standard layout for section “Absolute Maximum Ratings”
33	Section “Operating Conditions” added
34f	Parameter “$\overline{\text{RSTIN}}$ pullup” replaced by “$\overline{\text{RSTIN}}$ current”
36f	DC Characteristics for reduced supply voltage added
38f	Separate specification for power consumption with greatly improved values
40ff	Description of clock generation improved
45, **55**, **65**	Timing adapted to 25 MHz
48, **58**, **66**	Timing for reduced supply voltage added

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com



C165

- High Performance 16-bit CPU with 4-Stage Pipeline
  - 80 ns Instruction Cycle Time at 25 MHz CPU Clock
  - 400 ns Multiplication (16 × 16 bit), 800 ns Division (32 / 16 bit)
  - Enhanced Boolean Bit Manipulation Facilities
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Single-Cycle Context Switching Support
  - 16 MBytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area
- 16-Priority-Level Interrupt System with 28 Sources, Sample-Rate down to 40 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- Clock Generation via prescaler or via direct clock input
- On-Chip Memory Modules
  - 2 KBytes On-Chip Internal RAM (IRAM)
- On-Chip Peripheral Modules
  - Two Multi-Functional General Purpose Timer Units with 5 Timers
  - Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
- Up to 16 MBytes External Address Space for Code and Data
  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed or Demultiplexed External Address/Data Buses with 8-Bit or 16-Bit Data Bus Width
  - Five Programmable Chip-Select Signals
  - Hold- and Hold-Acknowledge Bus Arbitration Support
- Idle and Power Down Modes
- Programmable Watchdog Timer
- Up to 77 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis
- Power Supply: the C165 can operate from a 5 V or a 3 V power supply
- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 100-Pin MQFP Package (0.65 mm pitch)
- 100-Pin TQFP Package (0.5 mm pitch)

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
P4			IO	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines:
P4.0	23	25	O	A16 Least Significant Segment Address Line
P4.1	24	26	O	A17 Segment Address Line
P4.2	25	27	O	A18 Segment Address Line
P4.3	26	28	O	A19 Segment Address Line
P4.4	29	31	O	A20 Segment Address Line
P4.5	30	32	O	A21 Segment Address Line
P4.6	31	33	O	A22 Segment Address Line
P4.7	32	34	O	A23 Most Significant Segment Address Line
$\overline{RD}$	33	35	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
$\overline{WR}$/ $\overline{WRL}$	34	36	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{READY}$	35	37	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle waitstates until the pin returns to a low level. An internal pullup device holds this pin high when nothing is driving it.
ALE	36	38	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
$\overline{EA}$	37	39	I	External Access Enable pin. A low level at this pin during and after Reset forces the C165 to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
V_{DD}	7, 28, 38, 49, 69, 78	9, 30, 40, 51, 71, 80	–	Digital Supply Voltage: + 5 V or + 3 V during normal operation and idle mode. ≥ 2.5 V during power down mode.
V_{SS}	4, 27, 39, 50, 70, 77	6, 29, 41, 52, 72, 79	–	Digital Ground.

Note: The following behavioural differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated like on a hardware reset. Especially the bootstrap loader may be activated when P0L.4 is low.
- Pin $\overline{\text{RSTIN}}$ may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

– 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
– 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
– 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
– 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/ output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.
In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. The C165 offers the possibility to switch the $\overline{CS}$ outputs to an unlatched mode. In this mode the internal filter logic is switched off and the $\overline{CS}$ signals are directly generated from the address. The unlatched $\overline{CS}$ mode is enabled by setting CSCFG (SYSCON.6).

Access to very slow memories or memories with varying access times is supported via a particular ‘Ready’ function.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration and allows to share external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7 … P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to ‘1’ the Slave Mode is selected where pin $\overline{HLDA}$ is switched to input. This allows to directly connect the slave controller to another master controller without glue logic.

For applications which require less than 16 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte, or to 64 KByte. In this case Port 4 outputs four, two, or no address lines at all. It outputs all 8 address lines, if an address space of 16 MBytes is used.

The CPU has a register context consisting of up to 16 wordwide GPRs at its disposal. These 16 GPRs are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 1024 words is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient C165 instruction set which includes the following instruction classes:

– Arithmetic Instructions
– Logical Instructions
– Boolean Bit Manipulation Instructions
– Compare and Loop Control Instructions
– Shift and Rotate Instructions
– Prioritize Instruction
– Data Movement Instructions
– System Stack Instructions
– Jump and Call Instructions
– Return Instructions
– System Control Instructions
– Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C165 is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C165 supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicity decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C165 has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Table 3 shows all of the possible C165 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

DC Characteristics (Standard Supply Voltage Range) (cont'd)
(Operating Conditions apply)[1]

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
$\overline{\text{RSTIN}}$ active current[4]	I_{RSTL}[6]	- 100	–	µA	$V_{IN} = V_{IL}$
$\overline{\text{READY}}$/$\overline{\text{RD}}$/$\overline{\text{WR}}$ inact. current[7]	I_{RWH}[5]	–	- 40	µA	V_{OUT} = 2.4 V
$\overline{\text{READY}}$/$\overline{\text{RD}}$/$\overline{\text{WR}}$ active current[7]	I_{RWL}[6]	- 500	–	µA	$V_{OUT} = V_{OLmax}$
ALE inactive current[7]	I_{ALEL}[5]	–	40	µA	$V_{OUT} = V_{OLmax}$
ALE active current[7]	I_{ALEH}[6]	500	–	µA	V_{OUT} = 2.4 V
Port 6 inactive current[7]	I_{P6H}[5]	–	- 40	µA	V_{OUT} = 2.4 V
Port 6 active current[7]	I_{P6L}[6]	- 500	–	µA	$V_{OUT} = V_{OL1max}$
PORT0 configuration current[8]	I_{P0H}[5]	–	- 10	µA	$V_{IN} = V_{IHmin}$
	I_{P0L}[6]	- 100	–	µA	$V_{IN} = V_{ILmax}$
XTAL1 input current	I_{IL} CC	–	± 20	µA	0 V < V_{IN} < V_{DD}
Pin capacitance[9] (digital inputs/outputs)	C_{IO} CC	–	10	pF	f = 1 MHz T_A = 25 °C

1) Keeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current I_{OV}.

2) Valid in bidirectional reset mode only.

3) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

4) These parameters describe the $\overline{\text{RSTIN}}$ pullup, which equals a resistance of ca. 50 to 250 kΩ.

5) The maximum current may be drawn while the respective signal line remains inactive.

6) The minimum current must be drawn in order to drive the respective signal line active.

7) This specification is valid during Reset and during Hold-mode or Adapt-mode. During Hold-mode Port 6 pins are only affected, if they are used (configured) for $\overline{\text{CS}}$ output and the open drain function is not enabled. The $\overline{\text{READY}}$-pullup is always active, except for Powerdown mode.

8) This specification is valid during Reset and during Adapt-mode.

9) Not 100% tested, guaranteed by design and characterization.

Power Consumption C165 (Standard Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD5}	–	$15 + 1.8 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IL}$ f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals active	I_{IDX5}	–	$2 + 0.4 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IH1}$ f_{CPU} in [MHz][1]
Power-down mode supply current	I_{PDO5}	–	50	µA	$V_{DD} = V_{DDmax}$[2]

1) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 8**. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

2) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD}, all outputs (including pins configured as outputs) disconnected.

Power Consumption C165 (Reduced Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD3}	–	$3 + 1.3 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IL}$ f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals active	I_{IDX3}	–	$1 + 0.4 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IH1}$ f_{CPU} in [MHz][1]
Power-down mode supply current	I_{PDO3}	–	30	µA	$V_{DD} = V_{DDmax}$[2]

1) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 8**. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

2) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD}, all outputs (including pins configured as outputs) disconnected.

AC Characteristics

Table 10 External Clock Drive XTAL1 (Standard Supply Voltage Range)
(Operating Conditions apply)

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		Unit
			min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	40	–	20	–	ns
High time[1]	t_1	SR	20[2]	–	6	–	ns
Low time[1]	t_2	SR	20[2]	–	6	–	ns
Rise time[1]	t_3	SR	–	10	–	6	ns
Fall time[1]	t_4	SR	–	10	–	6	ns

1) The clock input signal must reach the defined levels V_{IL2} and V_{IH2}.

2) The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

Table 11 External Clock Drive XTAL1 (Reduced Supply Voltage Range)
(Operating Conditions apply)

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		Unit
			min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	50	–	25	–	ns
High time[1]	t_1	SR	25[2]	–	8	–	ns
Low time[1]	t_2	SR	25[2]	–	8	–	ns
Rise time[1]	t_3	SR	–	10	–	6	ns
Fall time[1]	t_4	SR	–	10	–	6	ns

1) The clock input signal must reach the defined levels V_{IL2} and V_{IH2}.

2) The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

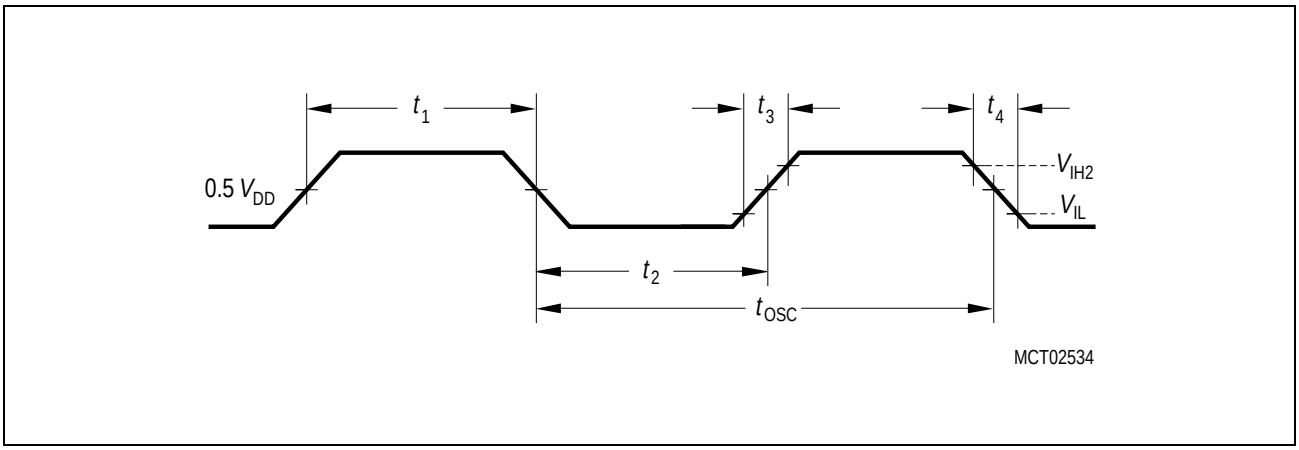


Figure 10 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal, the oscillator frequency is limited to a range of 4 MHz to 40 MHz.
It is strongly recommended to measure the oscillation allowance (or margin) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.
When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is guaranteed by design only (not 100% tested).

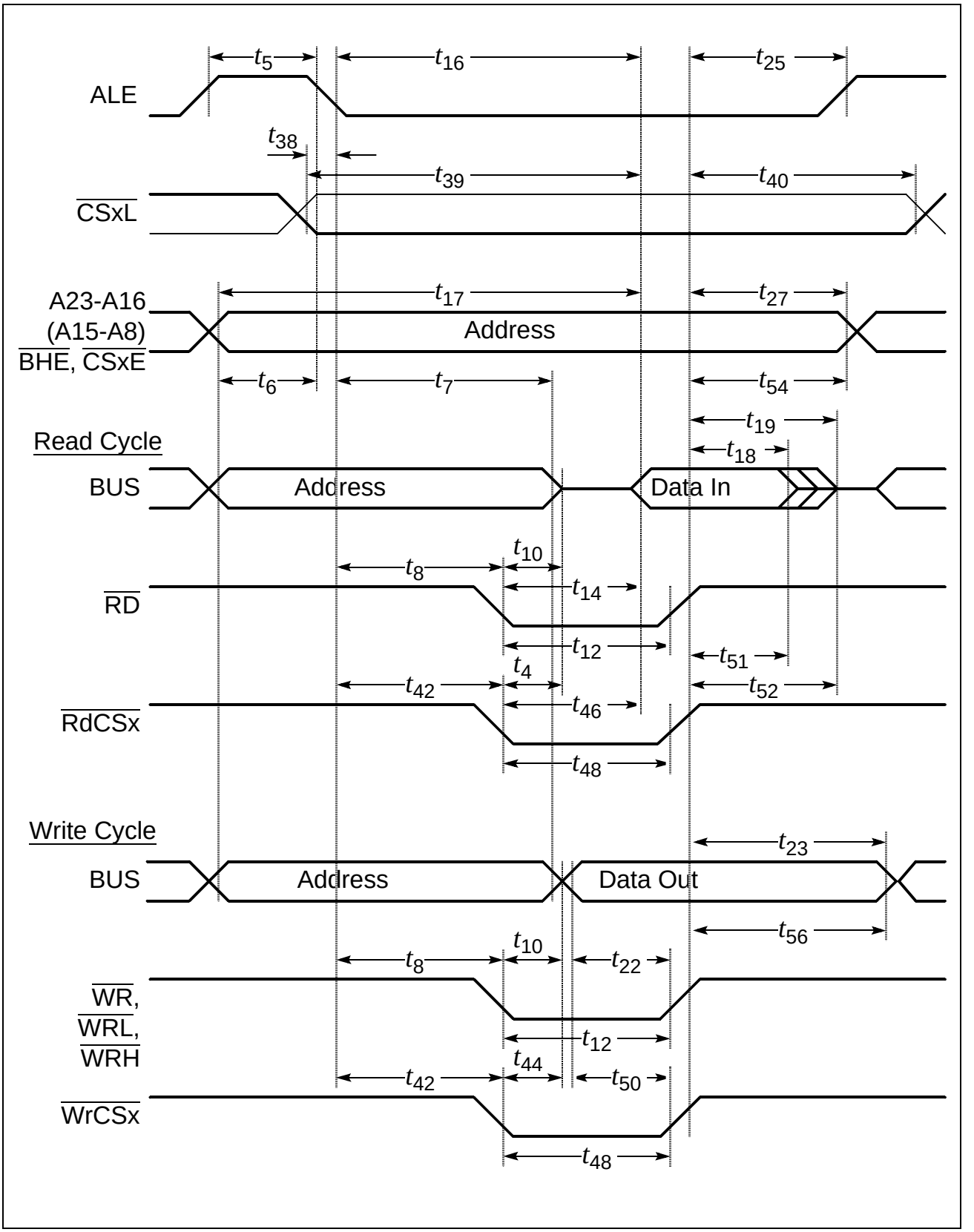


Figure 14 External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Extended ALE

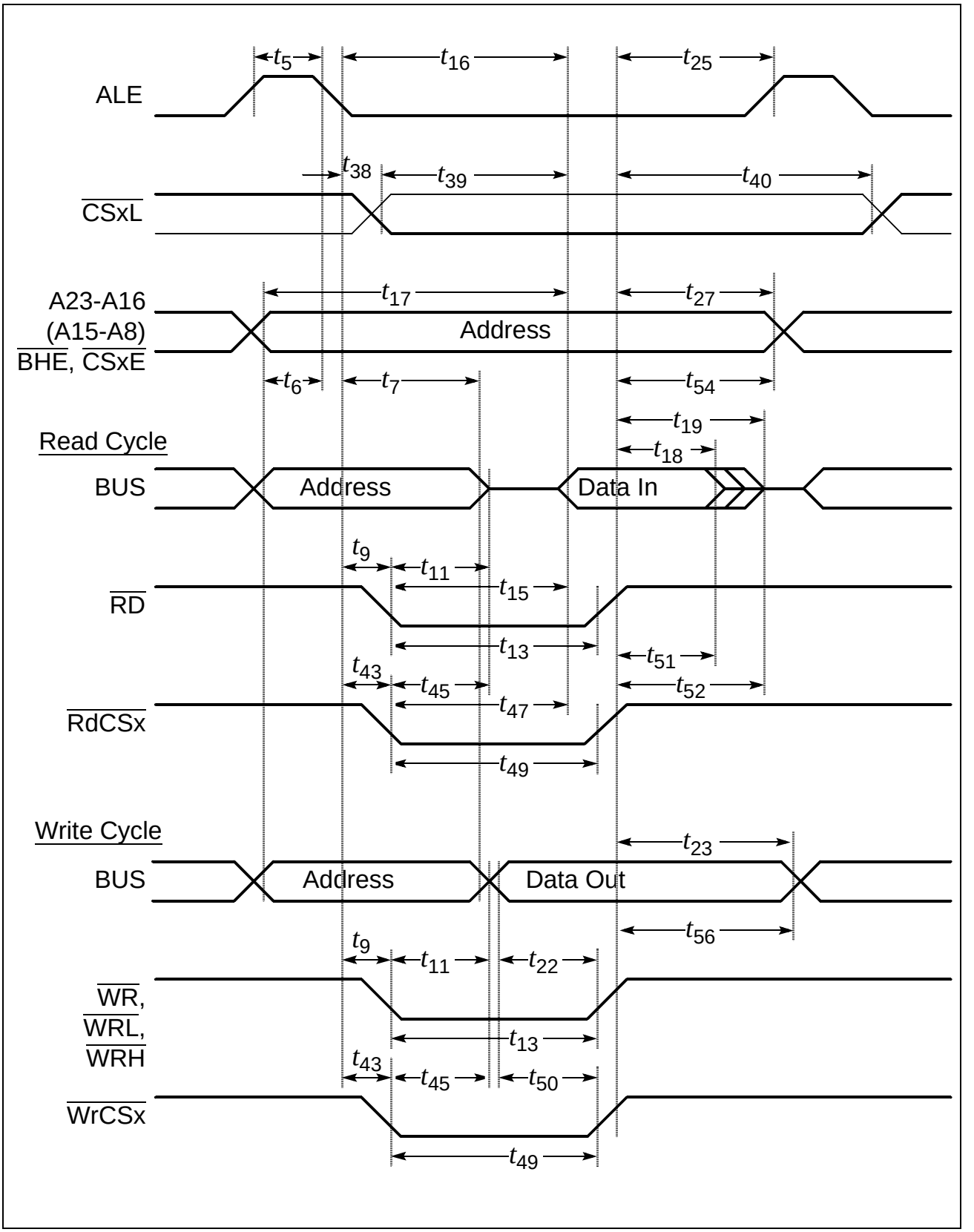


Figure 15 External Memory Cycle: Multiplexed Bus, No Read/Write Delay, Normal ALE

AC Characteristics

Demultiplexed Bus (Standard Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 4 TCL + 2t_A + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6	CC	4 + t_A	–	TCL - 16 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	- 10 + t_A	–	- 10 + t_A	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	20 + t_C	–	2TCL - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	40 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	50 + 2t_A + t_C	–	4TCL - 30 + 2t_A + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay[1)])	t_{20}	SR	–	26 + 2t_A + t_F[1)]	–	2TCL - 14 + 22t_A + t_F[1)]	ns
Data float after $\overline{RD}$ rising edge (no RW-delay[1)])	t_{21}	SR	–	10 + 2t_A + t_F[1)]	–	TCL - 10 + 22t_A + t_F[1)]	ns

Demultiplexed Bus (Standard Supply Voltage Range) (cont'd)
(Operating Conditions apply)
ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
Data valid to $\overline{WR}$	t_{22}	CC	20 + t_C	–	2TCL - 20 + t_C	–	ns
Data hold after $\overline{WR}$	t_{24}	CC	10 + t_F	–	TCL - 10 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{26}	CC	- 10 + t_F	–	- 10 + t_F	–	ns
Address hold after $\overline{WR}$[2]	t_{28}	CC	0 + t_F	–	0 + t_F	–	ns
ALE falling edge to $\overline{CS}$[3]	t_{38}	CC	- 4 - t_A	10 - t_A	- 4 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In[3]	t_{39}	SR	–	40 + t_C + $2t_A$	–	3TCL - 20 + t_C + $2t_A$	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$[3]	t_{41}	CC	6 + t_F	–	TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	t_{42}	CC	16 + t_A	–	TCL - 4 + t_A	–	ns
ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	t_{43}	CC	- 4 + t_A	–	- 4 + t_A	–	ns
$\overline{RdCS}$ to Valid Data In (with RW-delay)	t_{46}	SR	–	16 + t_C	–	2TCL - 24 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW-delay)	t_{47}	SR	–	36 + t_C	–	3TCL - 24 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW-delay)	t_{48}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW-delay)	t_{49}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	26 + t_C	–	2TCL - 14 + t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51}	SR	0	–	0	–	ns

Demultiplexed Bus (Reduced Supply Voltage Range) (cont'd)
(Operating Conditions apply)
ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
Data float after $\overline{\text{RdCS}}$ (with RW-delay)[1]	t_{53}	SR	–	30 + t_F	–	2TCL - 20 + $2t_A$ + t_F [1]	ns
Data float after $\overline{\text{RdCS}}$ (no RW-delay)[1]	t_{68}	SR	–	5 + t_F	–	TCL - 20 + $2t_A$ + t_F [1]	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{55}	CC	- 16 + t_F	–	- 16 + t_F	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{57}	CC	9 + t_F	–	TCL - 16 + t_F	–	ns

1) RW-delay and t_A refer to the next following bus cycle (including an access to an on-chip X-Peripheral).

2) Read data are latched with the same clock edge that triggers the address change and the rising $\overline{\text{RD}}$ edge. Therefore address changes before the end of $\overline{\text{RD}}$ have no impact on read cycles.

3) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

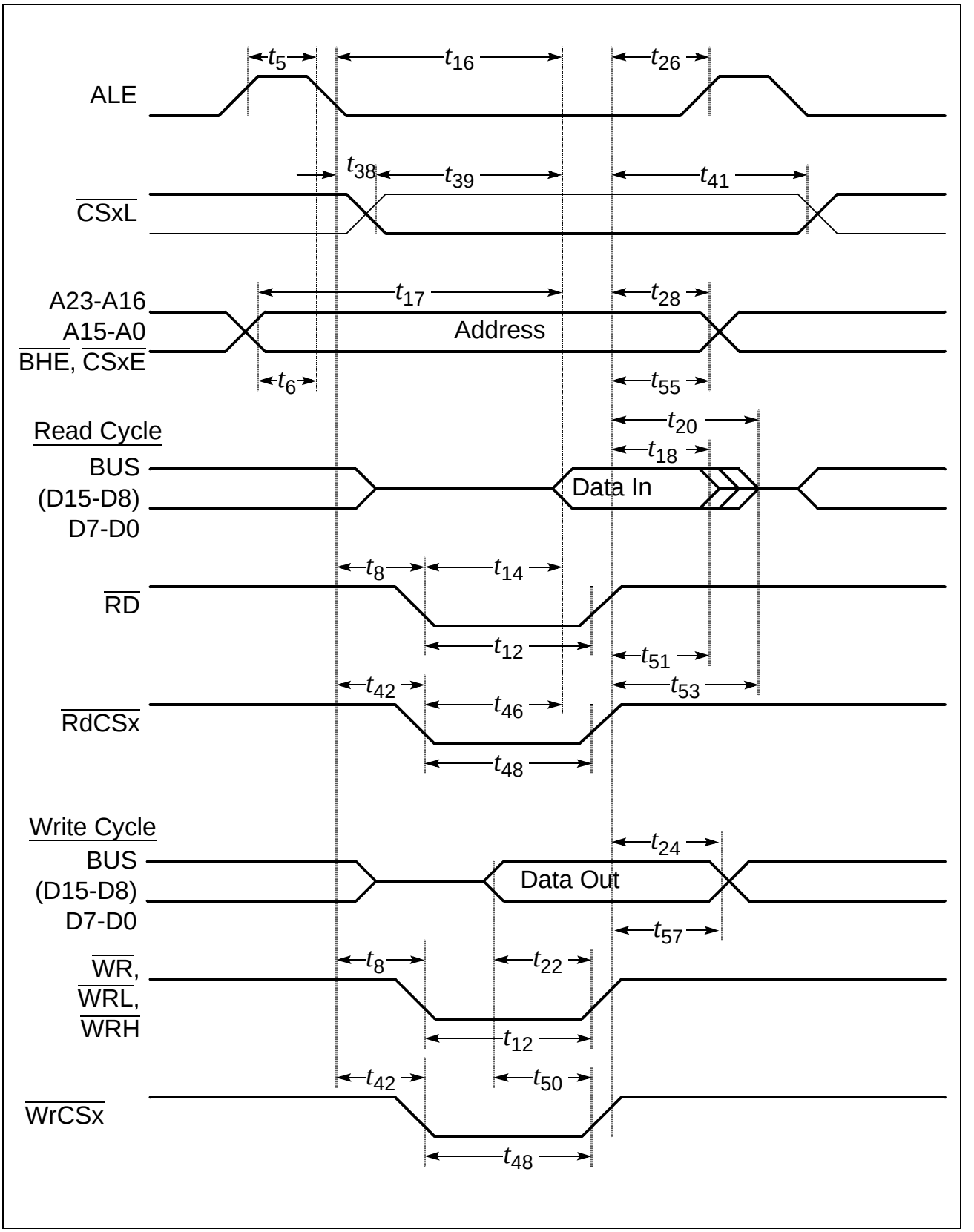


Figure 17 External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Normal ALE

AC Characteristics

External Bus Arbitration (Standard Supply Voltage)

(Operating Conditions apply)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
$\overline{\text{HOLD}}$ input setup time to CLKOUT	t_{61}	SR	20	–	20	–	ns
CLKOUT to $\overline{\text{HLDA}}$ high or $\overline{\text{BREQ}}$ low delay	t_{62}	CC	–	20	–	20	ns
CLKOUT to $\overline{\text{HLDA}}$ low or $\overline{\text{BREQ}}$ high delay	t_{63}	CC	–	20	–	20	ns
$\overline{\text{CSx}}$ release	t_{64}	CC	–	20	–	20	ns
$\overline{\text{CSx}}$ drive	t_{65}	CC	- 4	24	- 4	24	ns
Other signals release	t_{66}	CC	–	20	–	20	ns
Other signals drive	t_{67}	CC	- 4	24	- 4	24	ns

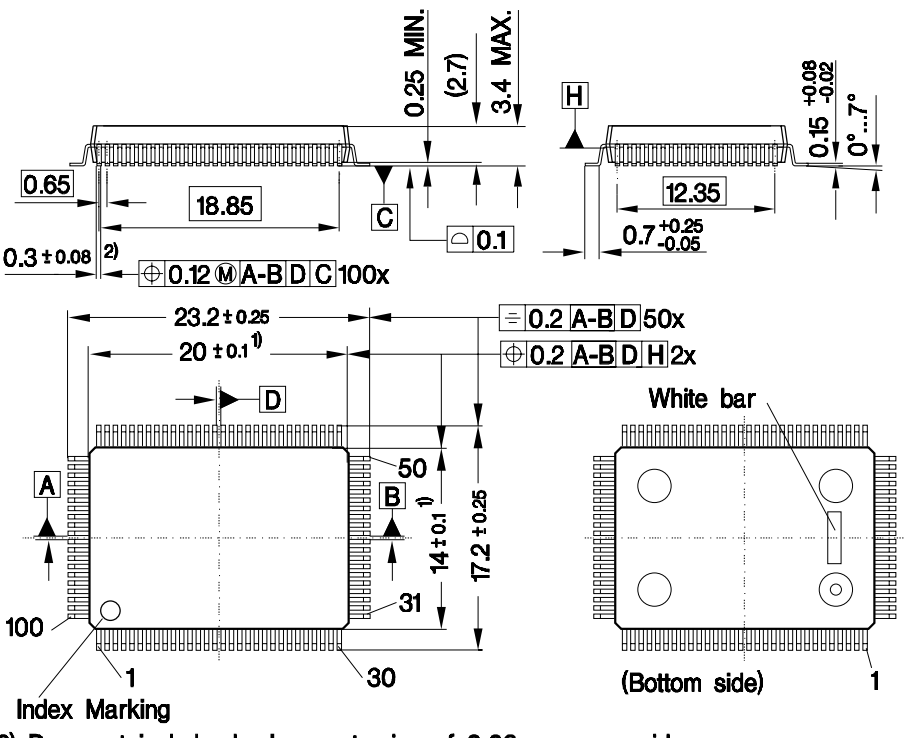
External Bus Arbitration (Reduced Supply Voltage)

(Operating Conditions apply)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
$\overline{\text{HOLD}}$ input setup time to CLKOUT	t_{61}	SR	30	–	30	–	ns
CLKOUT to $\overline{\text{HLDA}}$ high or $\overline{\text{BREQ}}$ low delay	t_{62}	CC	–	20	–	20	ns
CLKOUT to $\overline{\text{HLDA}}$ low or $\overline{\text{BREQ}}$ high delay	t_{63}	CC	–	20	–	20	ns
$\overline{\text{CSx}}$ release	t_{64}	CC	–	20	–	20	ns
$\overline{\text{CSx}}$ drive	t_{65}	CC	- 4	30	- 4	30	ns
Other signals release	t_{66}	CC	–	20	–	20	ns
Other signals drive	t_{67}	CC	- 4	30	- 4	30	ns

Package Outlines

P-MQFP-100 (SMD)
(Plastic Metric Quad Flat Package)



2) Does not include dambar protrusion of 0.08 max. per side
1) Does not include plastic or metal protrusion of 0.25 max. per side

GPR05365

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

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“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
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Dr. Ulrich Schumacher

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