Infineon Technologies - C165LMHABXQMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	77
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	P-MQFP-100
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c165lmhabxqma1

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
P4			IO	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines:
P4.0	23	25	O	A16 Least Significant Segment Address Line
P4.1	24	26	O	A17 Segment Address Line
P4.2	25	27	O	A18 Segment Address Line
P4.3	26	28	O	A19 Segment Address Line
P4.4	29	31	O	A20 Segment Address Line
P4.5	30	32	O	A21 Segment Address Line
P4.6	31	33	O	A22 Segment Address Line
P4.7	32	34	O	A23 Most Significant Segment Address Line
$\overline{RD}$	33	35	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
$\overline{WR}$/ $\overline{WRL}$	34	36	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{READY}$	35	37	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle waitstates until the pin returns to a low level. An internal pullup device holds this pin high when nothing is driving it.
ALE	36	38	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
$\overline{EA}$	37	39	I	External Access Enable pin. A low level at this pin during and after Reset forces the C165 to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
NC	40	42	–	This pin is not connected in the C165. No connection to the PCB is required.
PORT0 P0L.0-7 P0H.0-7	 41-48 51-58	 43-50 53-60	IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: D0 – D7 D0 – D7 P0H.0 – P0H.7: I/O D8 – D15 **Multiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: AD0 – AD7 AD0 – AD7 P0H.0 – P0H.7: A8 – A15 AD8 – AD15
PORT1 P1L.0-7 P1H.0-7	 59-66 67,68, 71-76	 61-68 69-70, 73-78	IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
P6			IO	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The Port 6 pins also serve for alternate functions:
P6.0	82	84	O	$\overline{CS0}$ Chip Select 0 Output
P6.1	83	85	O	$\overline{CS1}$ Chip Select 1 Output
P6.2	84	86	O	$\overline{CS2}$ Chip Select 2 Output
P6.3	85	87	O	$\overline{CS3}$ Chip Select 3 Output
P6.4	86	88	O	$\overline{CS4}$ Chip Select 4 Output
P6.5	87	89	I	$\overline{HOLD}$ External Master Hold Request Input
P6.6	88	90	I/O	$\overline{HLDA}$ Hold Acknowledge Outp.(master mode) or Input (slave mode)
P6.7	89	91	O	$\overline{BREQ}$ Bus Request Output
P2			IO	Port 2 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The following Port 2 pins serve for alternate functions:
P2.8	90	92	I	EX0IN Fast External Interrupt 0 Input
P2.9	91	93	I	EX1IN Fast External Interrupt 1 Input
P2.10	92	94	I	EX2IN Fast External Interrupt 2 Input
P2.11	93	95	I	EX3IN Fast External Interrupt 3 Input
P2.12	94	96	I	EX4IN Fast External Interrupt 4 Input
P2.13	95	97	I	EX5IN Fast External Interrupt 5 Input
P2.14	96	98	I	EX6IN Fast External Interrupt 6 Input
P2.15	97	99	I	EX7IN Fast External Interrupt 7 Input
P5			I	Port 5 is a 6-bit input-only port with Schmitt-Trigger char. The pins of Port 5 also serve as timer inputs:
P5.10	98	100	I	T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl Input
P5.11	99	1	I	T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl Input
P5.12	100	2	I	T6IN GPT2 Timer T6 Count Input
P5.13	1	3	I	T5IN GPT2 Timer T5 Count Input
P5.14	2	4	I	T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl Input
P5.15	3	5	I	T2EUD GPT1 Timer T2 Ext. Up/Down Ctrl Input

Functional Description

The architecture of the C165 combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. In addition the on-chip memory blocks allow the design of compact systems with maximum performance.
The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C165.

Note: All time specifications refer to a CPU clock of 25 MHz (see definition in the AC Characteristics section).

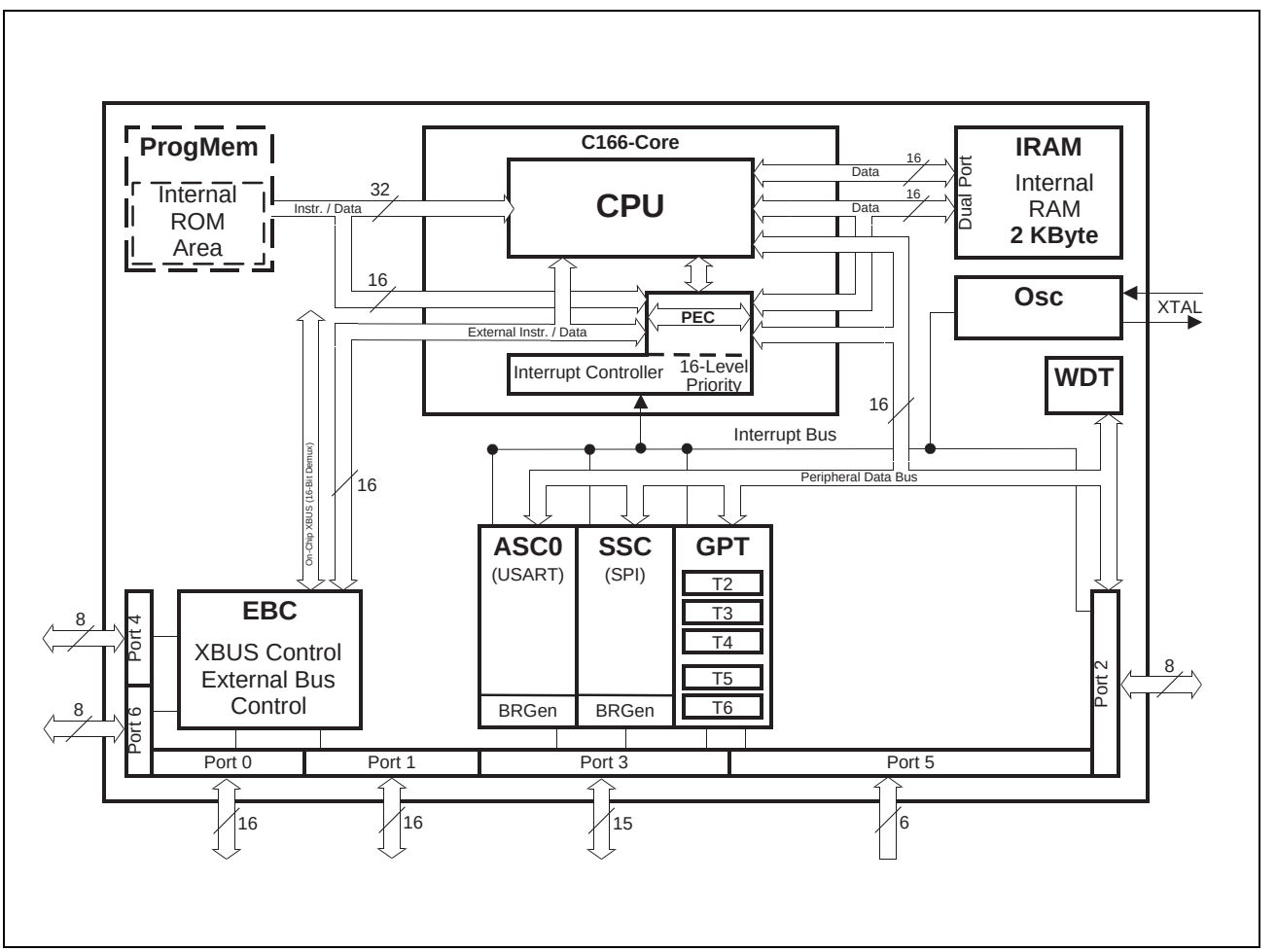


Figure 4 Block Diagram

The program memory, the internal RAM (IRAM) and the set of generic peripherals are connected to the CPU via separate buses. A fourth bus, the XBUS, connects external resources as well as additional on-chip resoures, the X-Peripherals (see **Figure 4**).

Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C165 is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C165 supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicity decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C165 has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Table 3 shows all of the possible C165 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Table 3 C165 Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
External Interrupt 0	CC8IR	CC8IE	CC8INT	$00'0060_H$	18_H
External Interrupt 1	CC9IR	CC9IE	CC9INT	$00'0064_H$	19_H
External Interrupt 2	CC10IR	CC10IE	CC10INT	$00'0068_H$	$1A_H$
External Interrupt 3	CC11IR	CC11IE	CC11INT	$00'006C_H$	$1B_H$
External Interrupt 4	CC12IR	CC12IE	CC12INT	$00'0070_H$	$1C_H$
External Interrupt 5	CC13IR	CC13IE	CC13INT	$00'0074_H$	$1D_H$
External Interrupt 6	CC14IR	CC14IE	CC14INT	$00'0078_H$	$1E_H$
External Interrupt 7	CC15IR	CC15IE	CC15INT	$00'007C_H$	$1F_H$
GPT1 Timer 2	T2IR	T2IE	T2INT	$00'0088_H$	22_H
GPT1 Timer 3	T3IR	T3IE	T3INT	$00'008C_H$	23_H
GPT1 Timer 4	T4IR	T4IE	T4INT	$00'0090_H$	24_H
GPT2 Timer 5	T5IR	T5IE	T5INT	$00'0094_H$	25_H
GPT2 Timer 6	T6IR	T6IE	T6INT	$00'0098_H$	26_H
GPT2 CAPREL Reg.	CRIR	CRIE	CRINT	$00'009C_H$	27_H
ASC0 Transmit	S0TIR	S0TIE	S0TINT	$00'00A8_H$	$2A_H$
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	$00'011C_H$	47_H
ASC0 Receive	S0RIR	S0RIE	S0RINT	$00'00AC_H$	$2B_H$
ASC0 Error	S0EIR	S0EIE	S0EINT	$00'00B0_H$	$2C_H$
SSC Transmit	SCTIR	SCTIE	SCTINT	$00'00B4_H$	$2D_H$
SSC Receive	SCRIR	SCRIE	SCRINT	$00'00B8_H$	$2E_H$
SSC Error	SCEIR	SCEIE	SCEINT	$00'00BC_H$	$2F_H$
Unassigned node	XP0IR	XP0IE	XP0INT	$00'0100_H$	40_H
Unassigned node	XP1IR	XP1IE	XP1INT	$00'0104_H$	41_H
Unassigned node	XP2IR	XP2IE	XP2INT	$00'0108_H$	42_H
Unassigned node	XP3IR	XP3IE	XP3INT	$00'010C_H$	43_H
Unassigned node	CC29IR	CC29IE	CC29INT	$00'0110_H$	44_H
Unassigned node	CC30IR	CC30IE	CC30INT	$00'0114_H$	45_H
Unassigned node	CC31IR	CC31IE	CC31INT	$00'0118_H$	46_H

Table 6 C165 Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
P1H	**b**	$FF06_H$		83_H	Port 1 High Reg. (Upper half of PORT1)	00_H
P1L	**b**	$FF04_H$		82_H	Port 1 Low Reg.(Lower half of PORT1)	00_H
P2	**b**	$FFC0_H$		$E0_H$	Port 2 Register	0000_H
P3	**b**	$FFC4_H$		$E2_H$	Port 3 Register	0000_H
P4	**b**	$FFC8_H$		$E4_H$	Port 4 Register (8 bits)	00_H
P5	**b**	$FFA2_H$		$D1_H$	Port 5 Register (read only)	$XXXX_H$
P6	**b**	$FFCC_H$		$E6_H$	Port 6 Register (8 bits)	00_H
PECC0		$FEC0_H$		60_H	PEC Channel 0 Control Register	0000_H
PECC1		$FEC2_H$		61_H	PEC Channel 1 Control Register	0000_H
PECC2		$FEC4_H$		62_H	PEC Channel 2 Control Register	0000_H
PECC3		$FEC6_H$		63_H	PEC Channel 3 Control Register	0000_H
PECC4		$FEC8_H$		64_H	PEC Channel 4 Control Register	0000_H
PECC5		$FECA_H$		65_H	PEC Channel 5 Control Register	0000_H
PECC6		$FECC_H$		66_H	PEC Channel 6 Control Register	0000_H
PECC7		$FECE_H$		67_H	PEC Channel 7 Control Register	0000_H
PSW	**b**	$FF10_H$		88_H	CPU Program Status Word	0000_H
RP0H	**b**	$F108_H$	**E**	84_H	System Startup Config. Reg. (Rd. only)	XX_H
S0BG		$FEB4_H$		$5A_H$	Serial Channel 0 Baud Rate Generator Reload Register	0000_H
S0CON	**b**	$FFB0_H$		$D8_H$	Serial Channel 0 Control Register	0000_H
S0EIC	**b**	$FF70_H$		$B8_H$	Serial Channel 0 Error Interrupt Ctrl. Reg	0000_H
S0RBUF		$FEB2_H$		59_H	Serial Channel 0 Receive Buffer Reg. (read only)	XX_H
S0RIC	**b**	$FF6E_H$		$B7_H$	Serial Channel 0 Receive Interrupt Control Register	0000_H
S0TBIC	**b**	$F19C_H$	**E**	CE_H	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000_H
S0TBUF		$FEB0_H$		58_H	Serial Channel 0 Transmit Buffer Register (write only)	00_H
S0TIC	**b**	$FF6C_H$		$B6_H$	Serial Channel 0 Transmit Interrupt Control Register	0000_H

Table 6 C165 Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
XP1IC	**b**	$F18E_H$	**E**	$C7_H$	Software Interrupt Control Register	0000_H
XP2IC	**b**	$F196_H$	**E**	CB_H	Software Interrupt Control Register	0000_H
XP3IC	**b**	$F19E_H$	**E**	CF_H	Software Interrupt Control Register	0000_H
ZEROS	**b**	$FF1C_H$		$8E_H$	Constant Value 0's Register (read only)	0000_H

1) The system configuration is selected during reset.

2) The reset value depends on the indicated reset source.

Absolute Maximum Ratings

Table 7 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	- 65	150	°C	–
Junction temperature	T_J	- 40	150	°C	under bias
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	- 0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	- 0.5	V_{DD} + 0.5	V	–
Input current on any pin during overload condition	–	- 10	10	mA	–
Absolute sum of all input currents during overload condition	–	–	|100|	mA	–
Power dissipation	P_{DISS}	–	1.5	W	–

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

DC Characteristics (Reduced Supply Voltage Range)

(Operating Conditions apply)[1)]

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Input low voltage (TTL, all except XTAL1)	V_{IL}	SR	- 0.5	0.8	V	–
Input low voltage XTAL1	V_{IL2}	SR	- 0.5	0.3 V_{DD}	V	–
Input high voltage (TTL, all except $\overline{\text{RSTIN}}$ and XTAL1)	V_{IH}	SR	1.8	V_{DD} + 0.5	V	–
Input high voltage $\overline{\text{RSTIN}}$ (when operated as input)	V_{IH1}	SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage XTAL1	V_{IH2}	SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Output low voltage (PORT0, PORT1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, $\overline{\text{RSTOUT}}$, $\overline{\text{RSTIN}}$[2)])	V_{OL}	CC	–	0.45	V	I_{OL} = 1.6 mA
Output low voltage (all other outputs)	V_{OL1}	CC	–	0.45	V	I_{OL} = 1.0 mA
Output high voltage[3)] (PORT0, PORT1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, $\overline{\text{RSTOUT}}$)	V_{OH}	CC	0.9 V_{DD}	–	V	I_{OH} = - 0.5 mA
Output high voltage[3)] (all other outputs)	V_{OH1}	CC	0.9 V_{DD}	–	V	I_{OH} = - 0.25 mA
Input leakage current (Port 5)	I_{OZ1}	CC	–	± 200	nA	0 V < V_{IN} < V_{DD}
Input leakage current (all other)	I_{OZ2}	CC	–	± 500	nA	0.45 V < V_{IN} < V_{DD}
$\overline{\text{RSTIN}}$ inactive current[4)]	I_{RSTH}[5)]		–	- 10	µA	V_{IN} = V_{IH1}
$\overline{\text{RSTIN}}$ active current[4)]	I_{RSTL}[6)]		- 100	–	µA	V_{IN} = V_{IL}
$\overline{\text{READY}}$/$\overline{\text{RD}}$/$\overline{\text{WR}}$ inact. current[7)]	I_{RWH}[5)]		–	- 10	µA	V_{OUT} = 2.4 V
$\overline{\text{READY}}$/$\overline{\text{RD}}$/$\overline{\text{WR}}$ active current[7)]	I_{RWL}[6)]		- 500	–	µA	V_{OUT} = V_{OLmax}
ALE inactive current[7)]	I_{ALEL}[5)]		–	20	µA	V_{OUT} = V_{OLmax}
ALE active current[7)]	I_{ALEH}[6)]		500	–	µA	V_{OUT} = 2.4 V
Port 6 inactive current[7)]	I_{P6H}[5)]		–	- 10	µA	V_{OUT} = 2.4 V
Port 6 active current[7)]	I_{P6L}[6)]		- 500	–	µA	V_{OUT} = V_{OL1max}

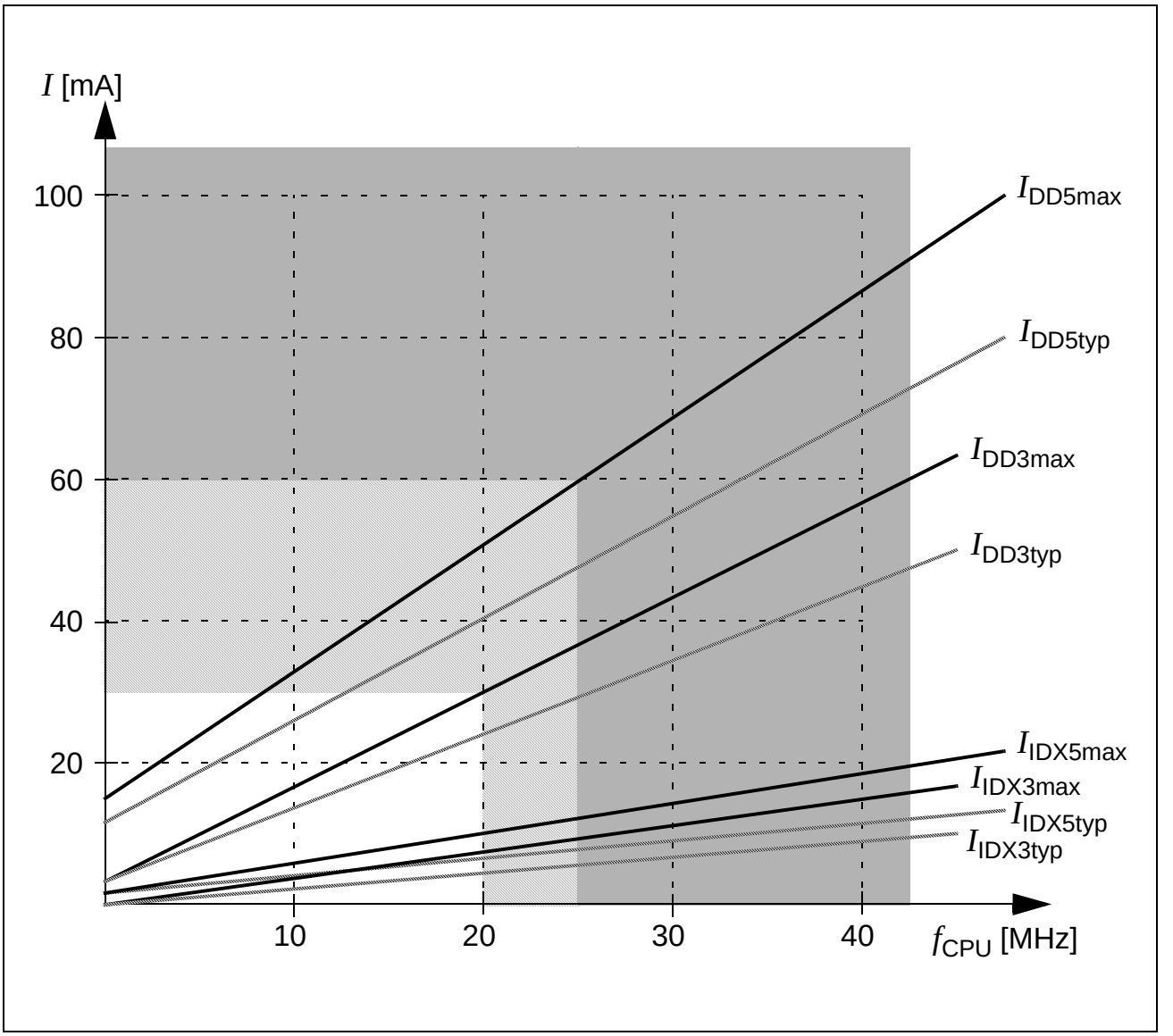


Figure 8 Supply/Idle Current as a Function of Operating Frequency

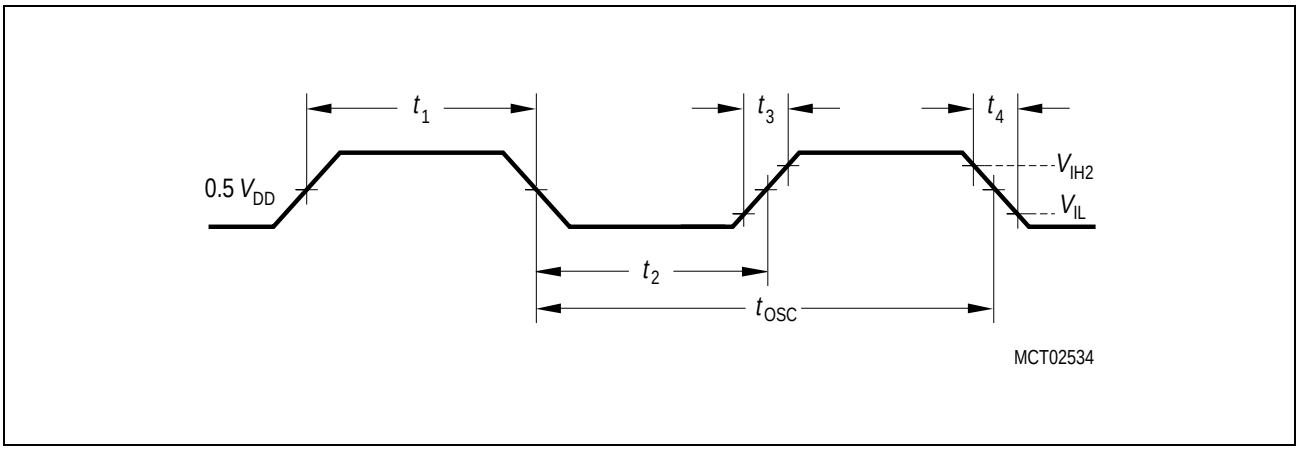


Figure 10 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal, the oscillator frequency is limited to a range of 4 MHz to 40 MHz.
It is strongly recommended to measure the oscillation allowance (or margin) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.
When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is guaranteed by design only (not 100% tested).

AC Characteristics

Multiplexed Bus (Reduced Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 6 TCL + $2t_A + t_C + t_F$ (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	11 + t_A	–	TCL - 14 + t_A	–	ns
Address setup to ALE	t_6	CC	5 + t_A	–	TCL - 20 + t_A	–	ns
Address hold after ALE	t_7	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	- 10 + t_A	–	-10 + t_A	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_{10}	CC	–	6	–	6	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_{11}	CC	–	31	–	TCL + 6	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	34 + t_C	–	2TCL - 16 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	59 + t_C	–	3TCL - 16 +t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	22 + t_C	–	2TCL - 28 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	47 + t_C	–	3TCL - 28 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	45 + t_A + t_C	–	3TCL - 30 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	57 + $2t_A$ + t_C	–	4TCL - 43 + $2t_A$ + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns

Multiplexed Bus (Reduced Supply Voltage Range) (cont'd)
(Operating Conditions apply)
ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
Data float after $\overline{RD}$	t_{19}	SR	–	36 + t_F	–	2TCL - 14 + t_F	ns
Data valid to $\overline{WR}$	t_{22}	CC	24 + t_C	–	2TCL - 26 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23}	CC	36 + t_F	–	2TCL - 14 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25}	CC	36 + t_F	–	2TCL - 14 + t_F	–	ns
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27}	CC	36 + t_F	–	2TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{CS}$[1)]	t_{38}	CC	- 8 - t_A	10 - t_A	- 8 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In[1)]	t_{39}	SR	–	47+ t_C + $2t_A$	–	3TCL - 28 + t_C + $2t_A$	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$[1)]	t_{40}	CC	57 + t_F	–	3TCL - 18 + t_F	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{42}	CC	19 + t_A	–	TCL - 6 + t_A	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{43}	CC	- 6 + t_A	–	- 6 + t_A	–	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{44}	CC	–	0	–	0	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{45}	CC	–	25	–	TCL	ns
$\overline{RdCS}$ to Valid Data In (with RW delay)	t_{46}	SR	–	20 + t_C	–	2TCL - 30 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW delay)	t_{47}	SR	–	45 + t_C	–	3TCL - 30 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay)	t_{48}	CC	38 + t_C	–	2TCL - 12 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay)	t_{49}	CC	63 + t_C	–	3TCL - 12 + t_C	–	ns

Multiplexed Bus (Reduced Supply Voltage Range) (cont'd)
(Operating Conditions apply)
ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
Data valid to $\overline{\text{WrCS}}$	t_{50}	CC	28 + t_C	–	2TCL - 22 + t_C	–	ns
Data hold after $\overline{\text{RdCS}}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{\text{RdCS}}$	t_{52}	SR	–	30 + t_F	–	2TCL - 20 + t_F	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{54}	CC	30 + t_F	–	2TCL - 20 + t_F	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{56}	CC	30 + t_F	–	2TCL - 20 + t_F	–	ns

1) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

AC Characteristics

Demultiplexed Bus (Standard Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 4 TCL + 2t_A + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6	CC	4 + t_A	–	TCL - 16 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	- 10 + t_A	–	- 10 + t_A	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	20 + t_C	–	2TCL - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	40 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	50 + 2t_A + t_C	–	4TCL - 30 + 2t_A + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay[1)])	t_{20}	SR	–	26 + 2t_A + t_F[1)]	–	2TCL - 14 + 22t_A + t_F[1)]	ns
Data float after $\overline{RD}$ rising edge (no RW-delay[1)])	t_{21}	SR	–	10 + 2t_A + t_F[1)]	–	TCL - 10 + 22t_A + t_F[1)]	ns

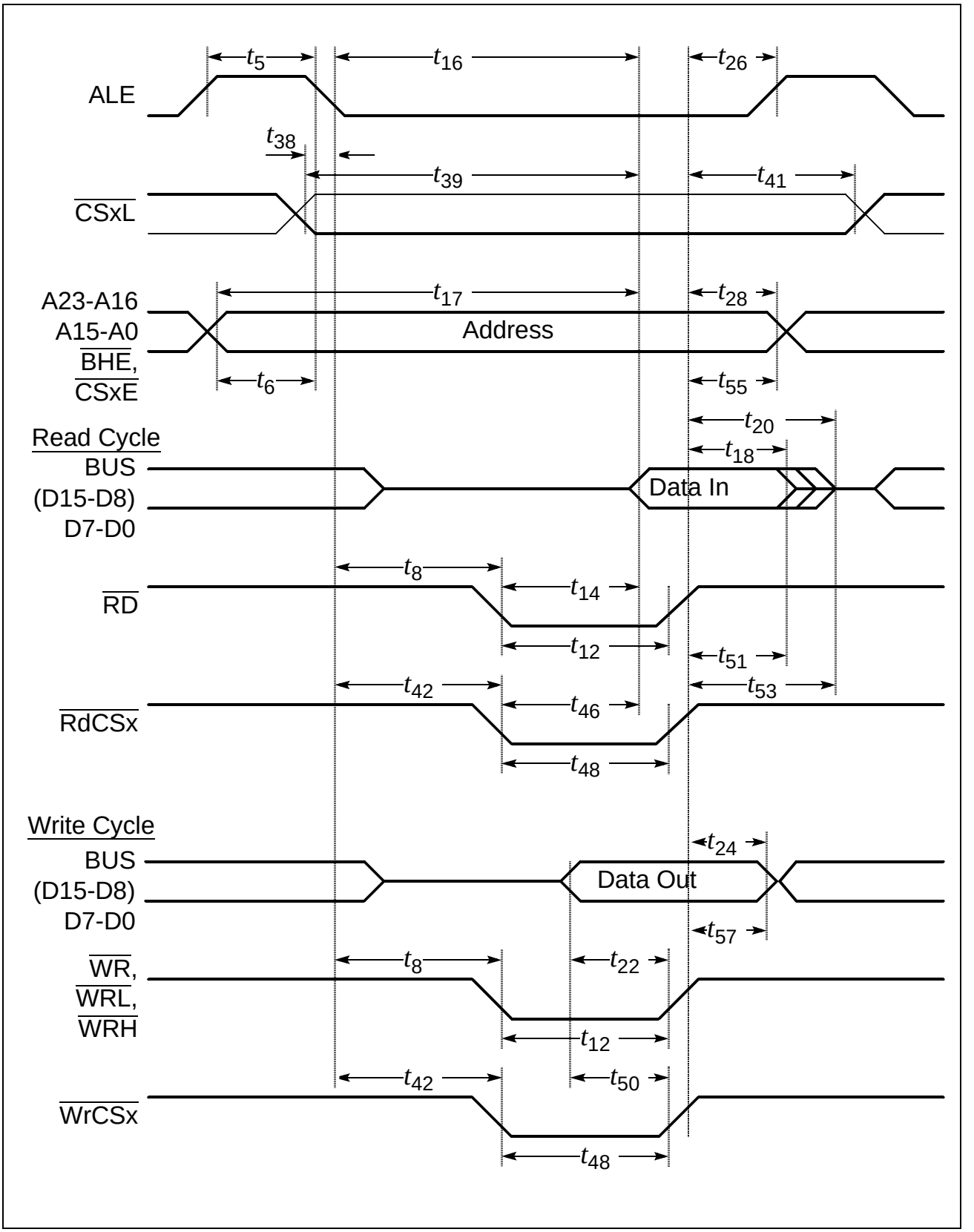


Figure 18 External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Extended ALE

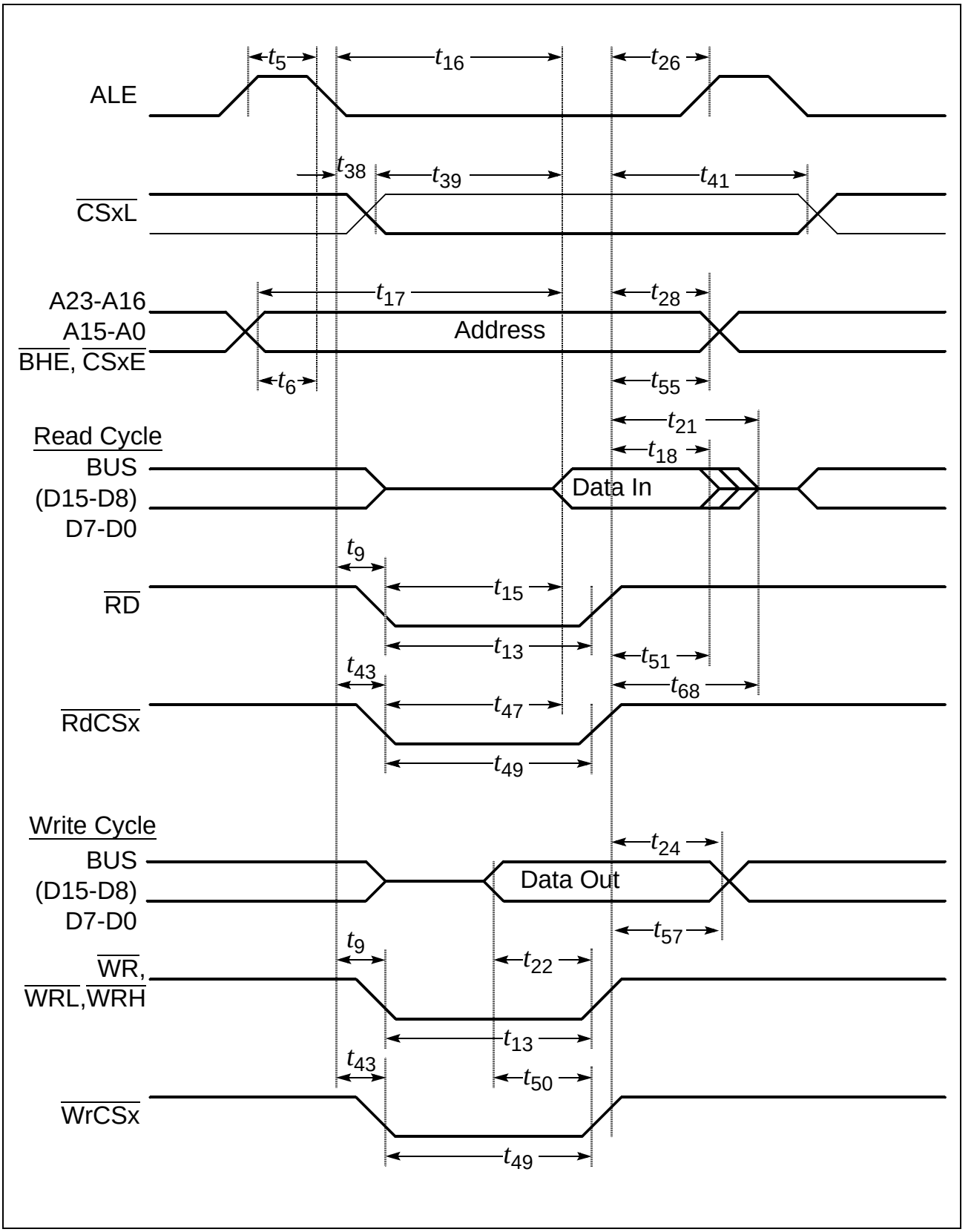
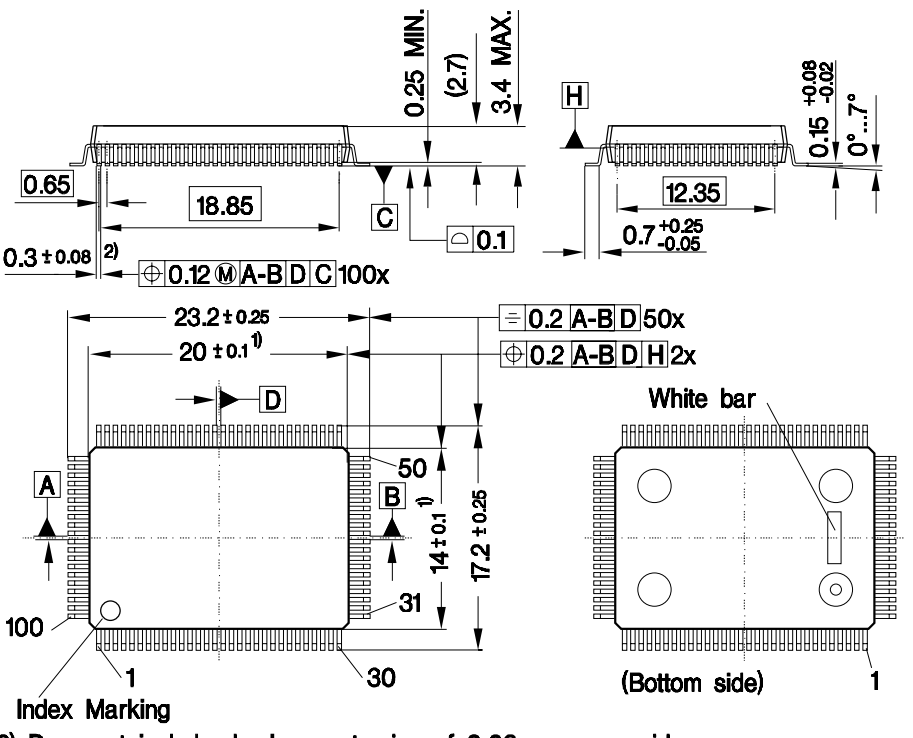


Figure 19 External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Normal ALE

Package Outlines

P-MQFP-100 (SMD)
(Plastic Metric Quad Flat Package)



2) Does not include dambar protrusion of 0.08 max. per side
1) Does not include plastic or metal protrusion of 0.25 max. per side

GPR05365

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

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“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

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