Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	77
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	P-MQFP-100
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sab-c165-lm-3v-ha

C165

16-Bit Single-Chip Microcontroller

Microcontrollers

Never stop thinking.

Pin Configuration TQFP Package
(top view)

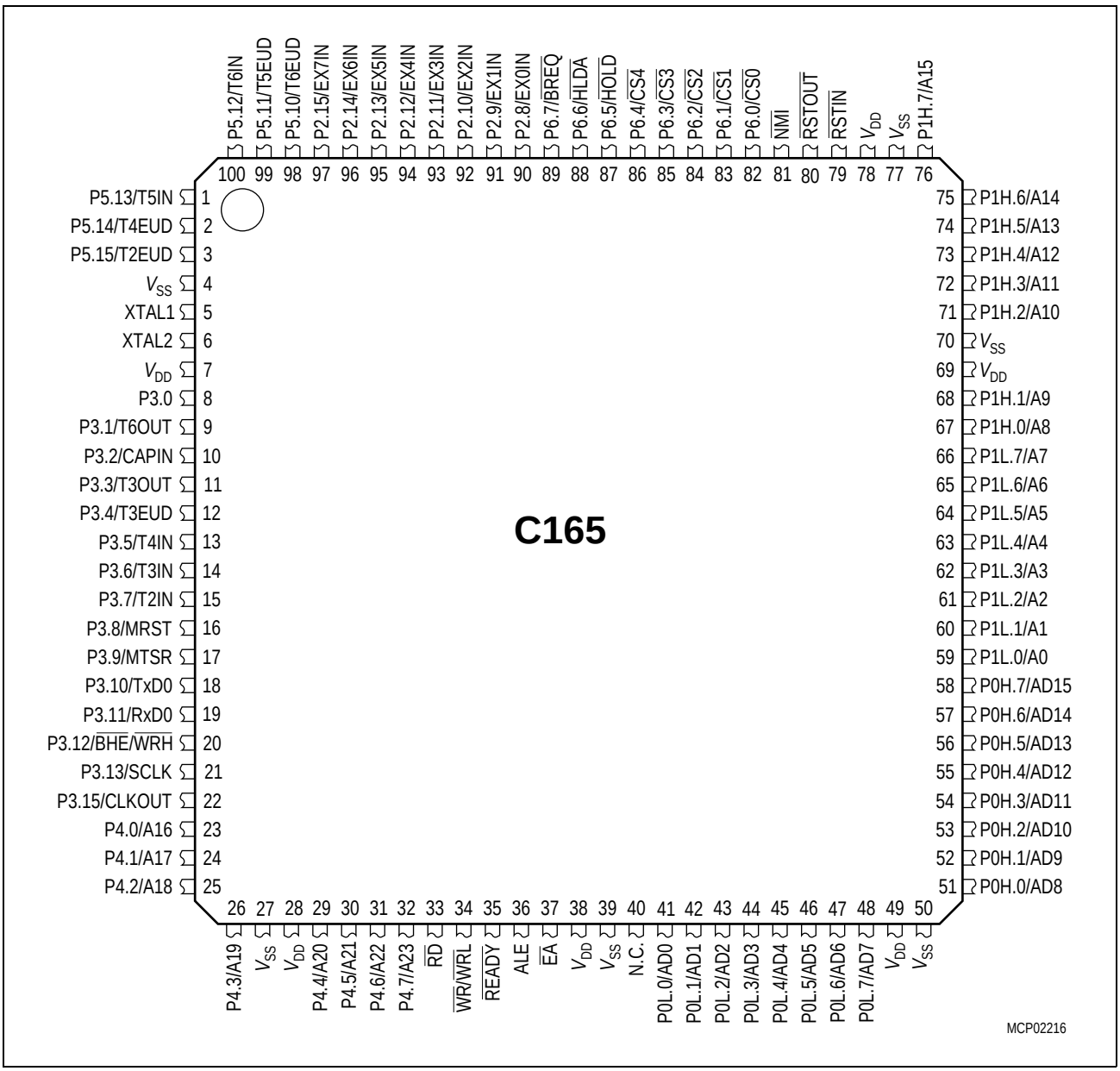

Figure 2

Pin Configuration MQFP Package
(top view)

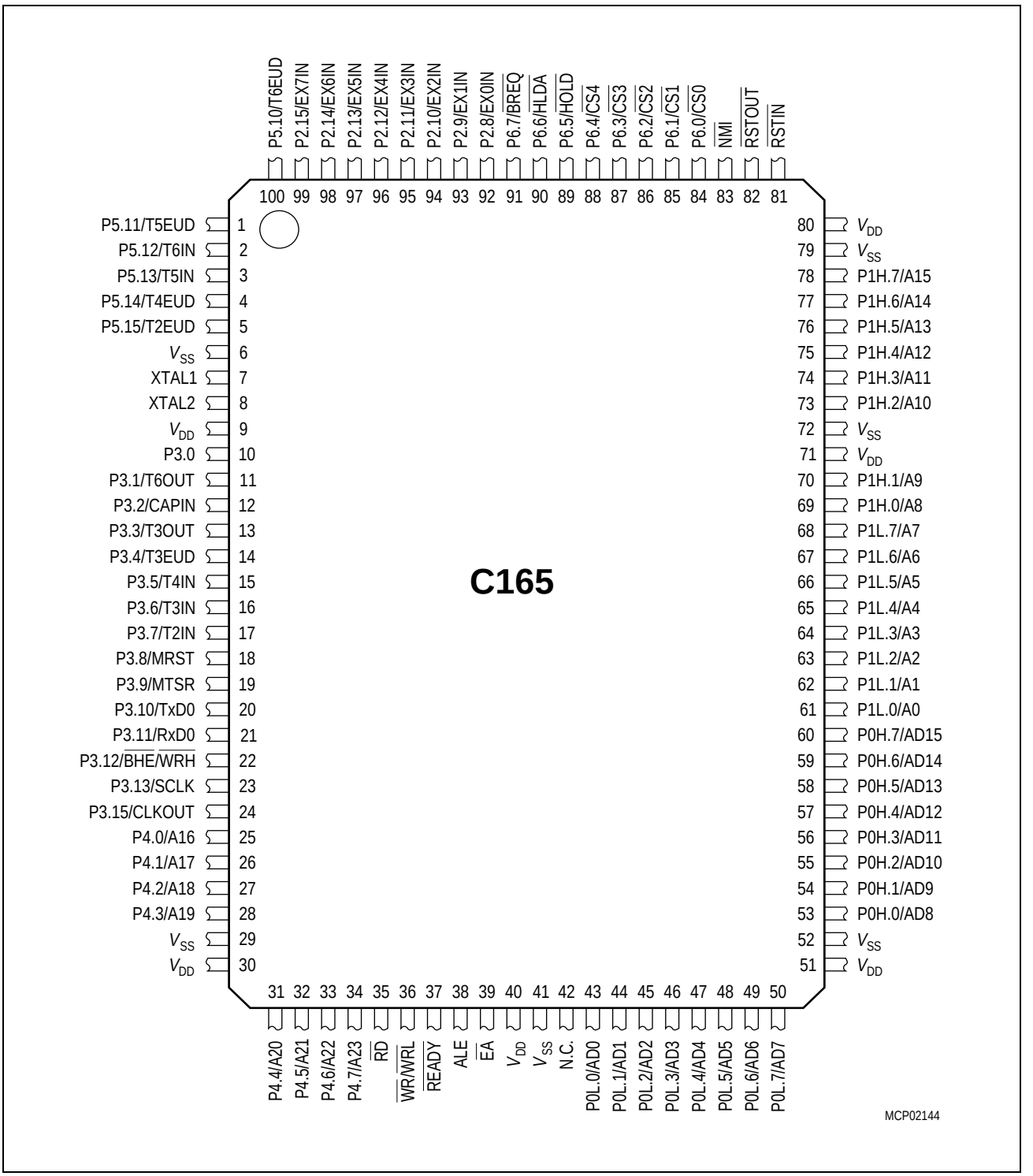

Figure 3

Table 2 Pin Definitions and Functions

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function	
XTAL1	5	7	I	XTAL1:	Input to the oscillator amplifier and input to the internal clock generator
XTAL2	6	8	O	XTAL2:	Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.
P3			IO	Port 3 is a 15-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The Port 3 pins serve for following alternate functions:	
P3.0	8	10			
P3.1	9	11	O	T6OUT	GPT2 Timer T6 Toggle Latch Output
P3.2	10	12	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	11	13	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	12	14	I	T3EUD	GPT1 Timer T3 Ext. Up/Down Ctrl Input
P3.5	13	15	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Input
P3.6	14	16	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	15	17	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Input
P3.8	16	18	I/O	MRST	SSC Master-Receive/Slave-Transmit Input/Output
P3.9	17	19	I/O	MTSR	SSC Master-Transmit/Slave-Receive Output/Input
P3.10	18	20	O	TxD0	ASC0 Clock/Data Output (Asyn./Sync.)
P3.11	19	21	I/O	RxD0	ASC0 Data Inp. (Asyn.) or In/Out (Sync)
P3.12	20	22	O	$\overline{\text{BHE}}$	Ext. Memory High Byte Enable Signal,
			O	$\overline{\text{WRH}}$	Ext. Memory High Byte Write Strobe
P3.13	21	23	I/O	SCLK	SSC Master Cl. Output / Slave Cl. Input
P3.15	22	24	O	CLKOUT	System Clock Output (= CPU Clock)

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

– 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
– 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
– 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
– 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/ output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.
In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. The C165 offers the possibility to switch the $\overline{CS}$ outputs to an unlatched mode. In this mode the internal filter logic is switched off and the $\overline{CS}$ signals are directly generated from the address. The unlatched $\overline{CS}$ mode is enabled by setting CSCFG (SYSCON.6).

Access to very slow memories or memories with varying access times is supported via a particular ‘Ready’ function.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration and allows to share external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7 … P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to ‘1’ the Slave Mode is selected where pin $\overline{HLDA}$ is switched to input. This allows to directly connect the slave controller to another master controller without glue logic.

For applications which require less than 16 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte, or to 64 KByte. In this case Port 4 outputs four, two, or no address lines at all. It outputs all 8 address lines, if an address space of 16 MBytes is used.

Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C165's instructions can be executed in just one machine cycle which requires 80 ns at 25 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16×16 bit multiplication in 5 cycles and a 32-/16 bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

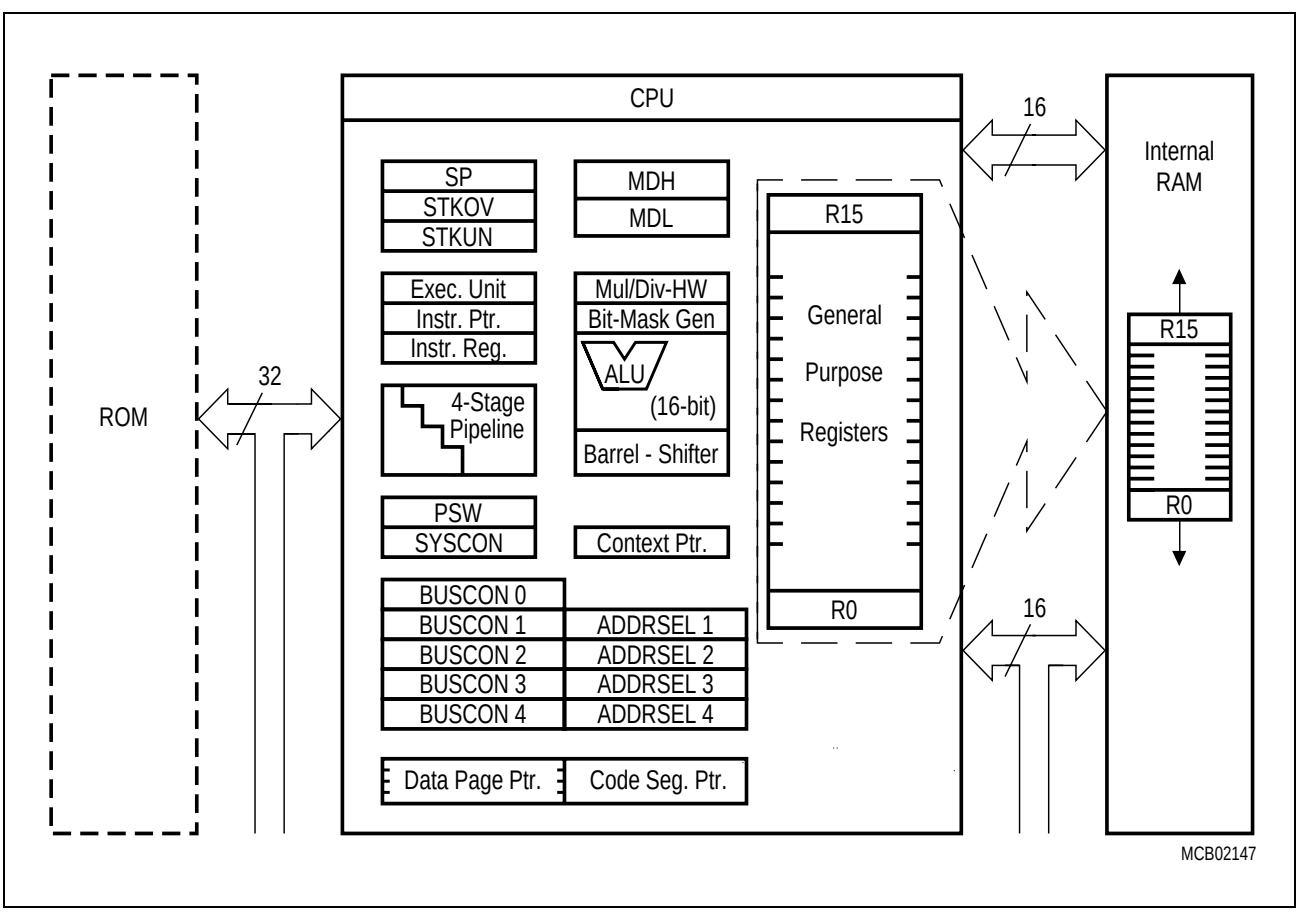

Figure 5 CPU Block Diagram

The CPU has a register context consisting of up to 16 wordwide GPRs at its disposal. These 16 GPRs are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 1024 words is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient C165 instruction set which includes the following instruction classes:

– Arithmetic Instructions
– Logical Instructions
– Boolean Bit Manipulation Instructions
– Compare and Loop Control Instructions
– Shift and Rotate Instructions
– Prioritize Instruction
– Data Movement Instructions
– System Stack Instructions
– Jump and Call Instructions
– Return Instructions
– System Control Instructions
– Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

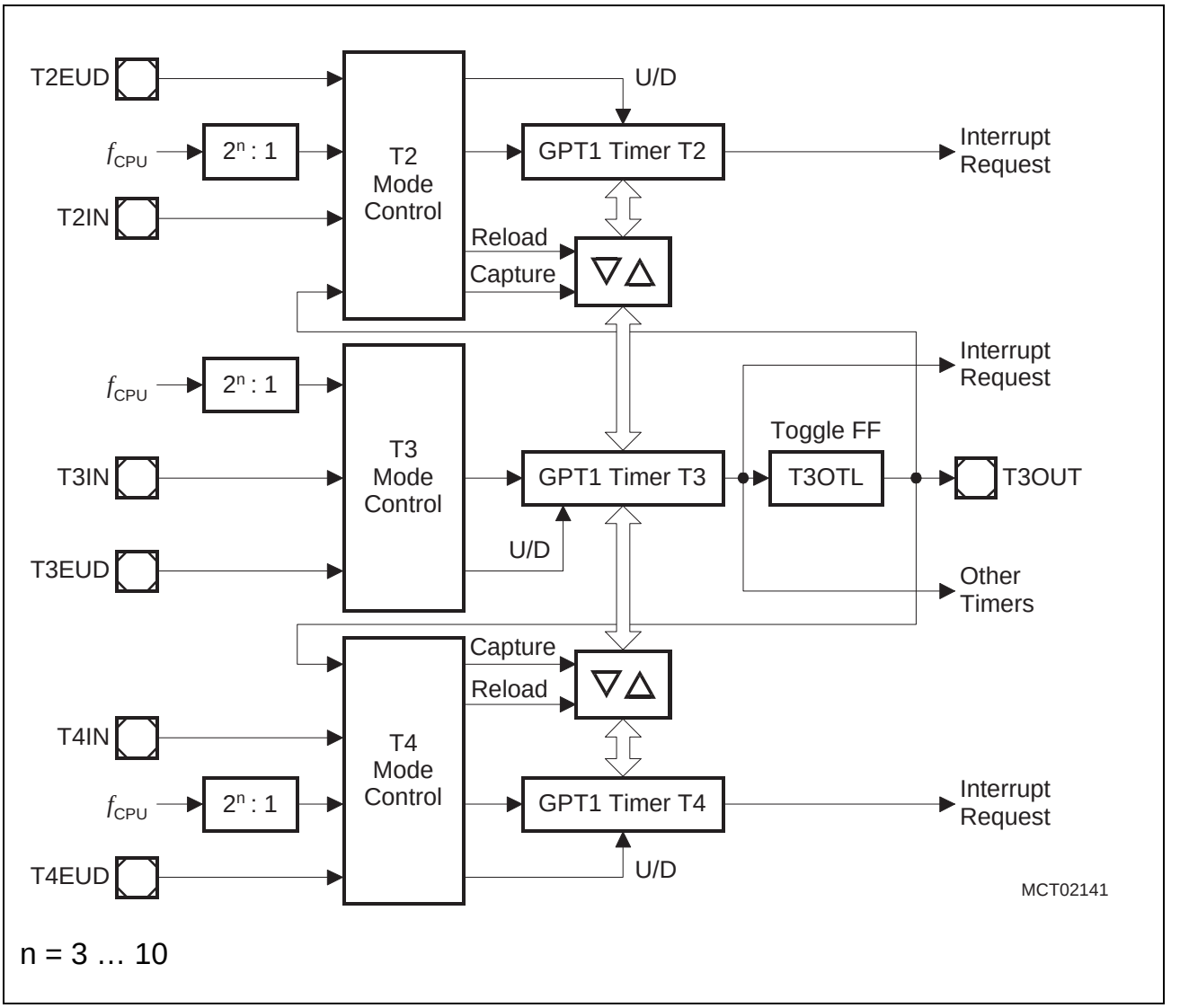

Figure 6 Block Diagram of GPT1

With its maximum resolution of 8 TCL, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock. The count direction (up/down) for each timer is programmable by software. Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5 and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the C165 to measure absolute time differences or to perform pulse multiplication without software overhead.

Table 6 C165 Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
CP		$FE10_H$		08_H	CPU Context Pointer Register	$FC00_H$
CRIC	**b**	$FF6A_H$		$B5_H$	GPT2 CAPREL Interrupt Ctrl. Reg.	0000_H
CSP		$FE08_H$		04_H	CPU Code Seg. Pointer Reg. (read only)	0000_H
DP0H	**b**	$F102_H$	**E**	81_H	P0H Direction Control Register	00_H
DP0L	**b**	$F100_H$	**E**	80_H	P0L Direction Control Register	00_H
DP1H	**b**	$F106_H$	**E**	83_H	P1H Direction Control Register	00_H
DP1L	**b**	$F104_H$	**E**	82_H	P1L Direction Control Register	00_H
DP2	**b**	$FFC2_H$		$E1_H$	Port 2 Direction Control Register	0000_H
DP3	**b**	$FFC6_H$		$E3_H$	Port 3 Direction Control Register	0000_H
DP4	**b**	$FFCA_H$		$E5_H$	Port 4 Direction Control Register	00_H
DP6	**b**	$FFCE_H$		$E7_H$	Port 6 Direction Control Register	00_H
DPP0		$FE00_H$		00_H	CPU Data Page Pointer 0 Reg. (10 bits)	0000_H
DPP1		$FE02_H$		01_H	CPU Data Page Pointer 1 Reg. (10 bits)	0001_H
DPP2		$FE04_H$		02_H	CPU Data Page Pointer 2 Reg. (10 bits)	0002_H
DPP3		$FE06_H$		03_H	CPU Data Page Pointer 3 Reg. (10 bits)	0003_H
EXICON	**b**	$F1C0_H$	**E**	$E0_H$	External Interrupt Control Register	0000_H
IDCHIP		$F07C_H$	**E**	$3E_H$	Identifier	$05XX_H$
IDMANUF		$F07E_H$	**E**	$3F_H$	Identifier	1820_H
IDMEM		$F07A_H$	**E**	$3D_H$	Identifier	0000_H
IDMEM2		$F076_H$	**E**	$3B_H$	Identifier	0000_H
IDPROG		$F078_H$	**E**	$3C_H$	Identifier	0000_H
MDC	**b**	$FF0E_H$		87_H	CPU Multiply Divide Control Register	0000_H
MDH		$FE0C_H$		06_H	CPU Multiply Divide Reg. – High Word	0000_H
MDL		$FE0E_H$		07_H	CPU Multiply Divide Reg. – Low Word	0000_H
ODP2	**b**	$F1C2_H$	**E**	$E1_H$	Port 2 Open Drain Control Register	0000_H
ODP3	**b**	$F1C6_H$	**E**	$E3_H$	Port 3 Open Drain Control Register	0000_H
ODP6	**b**	$F1CE_H$	**E**	$E7_H$	Port 6 Open Drain Control Register	00_H
ONES	**b**	$FF1E_H$		$8F_H$	Constant Value 1's Register (read only)	$FFFF_H$
P0H	**b**	$FF02_H$		81_H	Port 0 High Reg. (Upper half of PORT0)	00_H
P0L	**b**	$FF00_H$		80_H	Port 0 Low Reg. (Lower half of PORT0)	00_H

Table 6 C165 Registers, Ordered by Name (cont'd)

Name		Physical Address		8-Bit Addr.	Description	Reset Value
XP1IC	**b**	$F18E_H$	**E**	$C7_H$	Software Interrupt Control Register	0000_H
XP2IC	**b**	$F196_H$	**E**	CB_H	Software Interrupt Control Register	0000_H
XP3IC	**b**	$F19E_H$	**E**	CF_H	Software Interrupt Control Register	0000_H
ZEROS	**b**	$FF1C_H$		$8E_H$	Constant Value 0's Register (read only)	0000_H

1) The system configuration is selected during reset.

2) The reset value depends on the indicated reset source.

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C165. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 8 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Standard digital supply voltage (5 V versions)	V_{DD}	4.5	5.5	V	Active mode, f_{CPUmax} = 25 MHz
		2.5[1]	5.5	V	PowerDown mode
Reduced digital supply voltage (3 V versions)	V_{DD}	3.0	3.6	V	Active mode, f_{CPUmax} = 20 MHz
		2.5[1]	3.6	V	PowerDown mode
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	–	± 5	mA	Per pin[2)3)]
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	–	50	mA	[3)]
External Load Capacitance	C_L	–	100	pF	–
Ambient temperature	T_A	0	70	°C	SAB-C165 …
		- 40	85	°C	SAF-C165 …
		- 40	125	°C	SAK-C165 …

1) Output voltages and output currents will be reduced when V_{DD} leaves the range defined for active mode.

2) Overload conditions occur if the standard operatings conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$ + 0.5 V or $V_{OV} < V_{SS}$ – 0.5 V). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltage must remain within the specified limits. Proper operation is not guaranteed if overload conditions occur on functional pins such as XTAL1, $\overline{RD}$, $\overline{WR}$, etc.

3) Not 100% tested, guaranteed by design and characterization.

DC Characteristics (Standard Supply Voltage Range) (cont'd)
(Operating Conditions apply)[1]

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
$\overline{\text{RSTIN}}$ active current[4]	I_{RSTL}[6]	- 100	–	µA	$V_{IN} = V_{IL}$
$\overline{\text{READY}}$/$\overline{\text{RD}}$/$\overline{\text{WR}}$ inact. current[7]	I_{RWH}[5]	–	- 40	µA	V_{OUT} = 2.4 V
$\overline{\text{READY}}$/$\overline{\text{RD}}$/$\overline{\text{WR}}$ active current[7]	I_{RWL}[6]	- 500	–	µA	$V_{OUT} = V_{OLmax}$
ALE inactive current[7]	I_{ALEL}[5]	–	40	µA	$V_{OUT} = V_{OLmax}$
ALE active current[7]	I_{ALEH}[6]	500	–	µA	V_{OUT} = 2.4 V
Port 6 inactive current[7]	I_{P6H}[5]	–	- 40	µA	V_{OUT} = 2.4 V
Port 6 active current[7]	I_{P6L}[6]	- 500	–	µA	$V_{OUT} = V_{OL1max}$
PORT0 configuration current[8]	I_{P0H}[5]	–	- 10	µA	$V_{IN} = V_{IHmin}$
	I_{P0L}[6]	- 100	–	µA	$V_{IN} = V_{ILmax}$
XTAL1 input current	I_{IL} CC	–	± 20	µA	0 V < V_{IN} < V_{DD}
Pin capacitance[9] (digital inputs/outputs)	C_{IO} CC	–	10	pF	f = 1 MHz T_A = 25 °C

1) Keeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current I_{OV}.

2) Valid in bidirectional reset mode only.

3) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

4) These parameters describe the $\overline{\text{RSTIN}}$ pullup, which equals a resistance of ca. 50 to 250 kΩ.

5) The maximum current may be drawn while the respective signal line remains inactive.

6) The minimum current must be drawn in order to drive the respective signal line active.

7) This specification is valid during Reset and during Hold-mode or Adapt-mode. During Hold-mode Port 6 pins are only affected, if they are used (configured) for $\overline{\text{CS}}$ output and the open drain function is not enabled. The $\overline{\text{READY}}$-pullup is always active, except for Powerdown mode.

8) This specification is valid during Reset and during Adapt-mode.

9) Not 100% tested, guaranteed by design and characterization.

Table 9 C165 Clock Generation Modes

CLKCFG (P0H.7-5)	CPU Frequency $f_{CPU} = f_{OSC} \times F$	External Clock Input Range[1]	Notes
0 X X	$f_{OSC} \times 1$	1 to 25 MHz	Direct drive[2]
1 X X	$f_{OSC} / 2$	2 to 50 MHz	CPU clock via prescaler

1) The external clock input range refers to a CPU clock range of 10 … 25 MHz (PLL operation).

2) The maximum frequency depends on the duty cycle of the external clock signal.

Prescaler Operation

When prescaler operation is configured (CLKCFG = $1XX_B$) the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{OSC} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{OSC}.

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{OSC} for any TCL.

Direct Drive

When direct drive is configured (CLKCFG = $0XX_B$) the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.
The frequency of f_{CPU} directly follows the frequency of f_{OSC} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{OSC}.
The timings listed below that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated via the following formula:

$$TCL_{min} = 1/f_{OSC} \times DC_{min} \qquad \text{(DC = duty cycle)}$$

For two consecutive TCLs the deviation caused by the duty cycle of f_{OSC} is compensated so the duration of 2TCL is always $1/f_{OSC}$. The minimum value TCL_{min} therefore has to be used only once for timings that require an odd number of TCLs (1, 3, …). Timings that require an even number of TCLs (2, 4, …) may use the formula $2TCL = 1/f_{OSC}$.

AC Characteristics

Table 10 External Clock Drive XTAL1 (Standard Supply Voltage Range)
(Operating Conditions apply)

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		Unit
			min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	40	–	20	–	ns
High time[1]	t_1	SR	20[2]	–	6	–	ns
Low time[1]	t_2	SR	20[2]	–	6	–	ns
Rise time[1]	t_3	SR	–	10	–	6	ns
Fall time[1]	t_4	SR	–	10	–	6	ns

1) The clock input signal must reach the defined levels V_{IL2} and V_{IH2}.

2) The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

Table 11 External Clock Drive XTAL1 (Reduced Supply Voltage Range)
(Operating Conditions apply)

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		Unit
			min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	50	–	25	–	ns
High time[1]	t_1	SR	25[2]	–	8	–	ns
Low time[1]	t_2	SR	25[2]	–	8	–	ns
Rise time[1]	t_3	SR	–	10	–	6	ns
Fall time[1]	t_4	SR	–	10	–	6	ns

1) The clock input signal must reach the defined levels V_{IL2} and V_{IH2}.

2) The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

AC Characteristics

Demultiplexed Bus (Standard Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 4 TCL + 2t_A + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6	CC	4 + t_A	–	TCL - 16 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	- 10 + t_A	–	- 10 + t_A	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	20 + t_C	–	2TCL - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	40 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	50 + 2t_A + t_C	–	4TCL - 30 + 2t_A + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay[1)])	t_{20}	SR	–	26 + 2t_A + t_F[1)]	–	2TCL - 14 + 22t_A + t_F[1)]	ns
Data float after $\overline{RD}$ rising edge (no RW-delay[1)])	t_{21}	SR	–	10 + 2t_A + t_F[1)]	–	TCL - 10 + 22t_A + t_F[1)]	ns

Demultiplexed Bus (Standard Supply Voltage Range) (cont'd)
(Operating Conditions apply)
ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
Data valid to $\overline{WR}$	t_{22}	CC	20 + t_C	–	2TCL - 20 + t_C	–	ns
Data hold after $\overline{WR}$	t_{24}	CC	10 + t_F	–	TCL - 10 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{26}	CC	- 10 + t_F	–	- 10 + t_F	–	ns
Address hold after $\overline{WR}$[2]	t_{28}	CC	0 + t_F	–	0 + t_F	–	ns
ALE falling edge to $\overline{CS}$[3]	t_{38}	CC	- 4 - t_A	10 - t_A	- 4 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In[3]	t_{39}	SR	–	40 + t_C + $2t_A$	–	3TCL - 20 + t_C + $2t_A$	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$[3]	t_{41}	CC	6 + t_F	–	TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	t_{42}	CC	16 + t_A	–	TCL - 4 + t_A	–	ns
ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	t_{43}	CC	- 4 + t_A	–	- 4 + t_A	–	ns
$\overline{RdCS}$ to Valid Data In (with RW-delay)	t_{46}	SR	–	16 + t_C	–	2TCL - 24 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW-delay)	t_{47}	SR	–	36 + t_C	–	3TCL - 24 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW-delay)	t_{48}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW-delay)	t_{49}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	26 + t_C	–	2TCL - 14 + t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51}	SR	0	–	0	–	ns

AC Characteristics

Demultiplexed Bus (Reduced Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 4 TCL + 2t_A + t_C + t_F (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	11 + t_A	–	TCL - 14 + t_A	–	ns
Address setup to ALE	t_6	CC	5 + t_A	–	TCL - 20 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	- 10 + t_A	–	- 10 + t_A	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	34 + t_C	–	2TCL - 16 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	59 + t_C	–	3TCL - 16 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	22 + t_C	–	2TCL - 28 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	47 + t_C	–	3TCL - 28 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	45 + t_A + t_C	–	3TCL - 30 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	57 + 2t_A + t_C	–	4TCL - 43 + 2t_A + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay[1)])	t_{20}	SR	–	36 + 2t_A + t_F[1)]	–	2TCL - 14 + 22t_A + t_F[1)]	ns
Data float after $\overline{RD}$ rising edge (no RW-delay[1)])	t_{21}	SR	–	15 + 2t_A + t_F[1)]	–	TCL - 10 + 22t_A + t_F[1)]	ns

Demultiplexed Bus (Reduced Supply Voltage Range) (cont'd)
(Operating Conditions apply)
ALE cycle time = 4 TCL + $2t_A$ + t_C + t_F (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
Data float after $\overline{\text{RdCS}}$ (with RW-delay)[1]	t_{53}	SR	–	30 + t_F	–	2TCL - 20 + $2t_A$ + t_F [1]	ns
Data float after $\overline{\text{RdCS}}$ (no RW-delay)[1]	t_{68}	SR	–	5 + t_F	–	TCL - 20 + $2t_A$ + t_F [1]	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{55}	CC	- 16 + t_F	–	- 16 + t_F	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{57}	CC	9 + t_F	–	TCL - 16 + t_F	–	ns

1) RW-delay and t_A refer to the next following bus cycle (including an access to an on-chip X-Peripheral).

2) Read data are latched with the same clock edge that triggers the address change and the rising $\overline{\text{RD}}$ edge. Therefore address changes before the end of $\overline{\text{RD}}$ have no impact on read cycles.

3) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

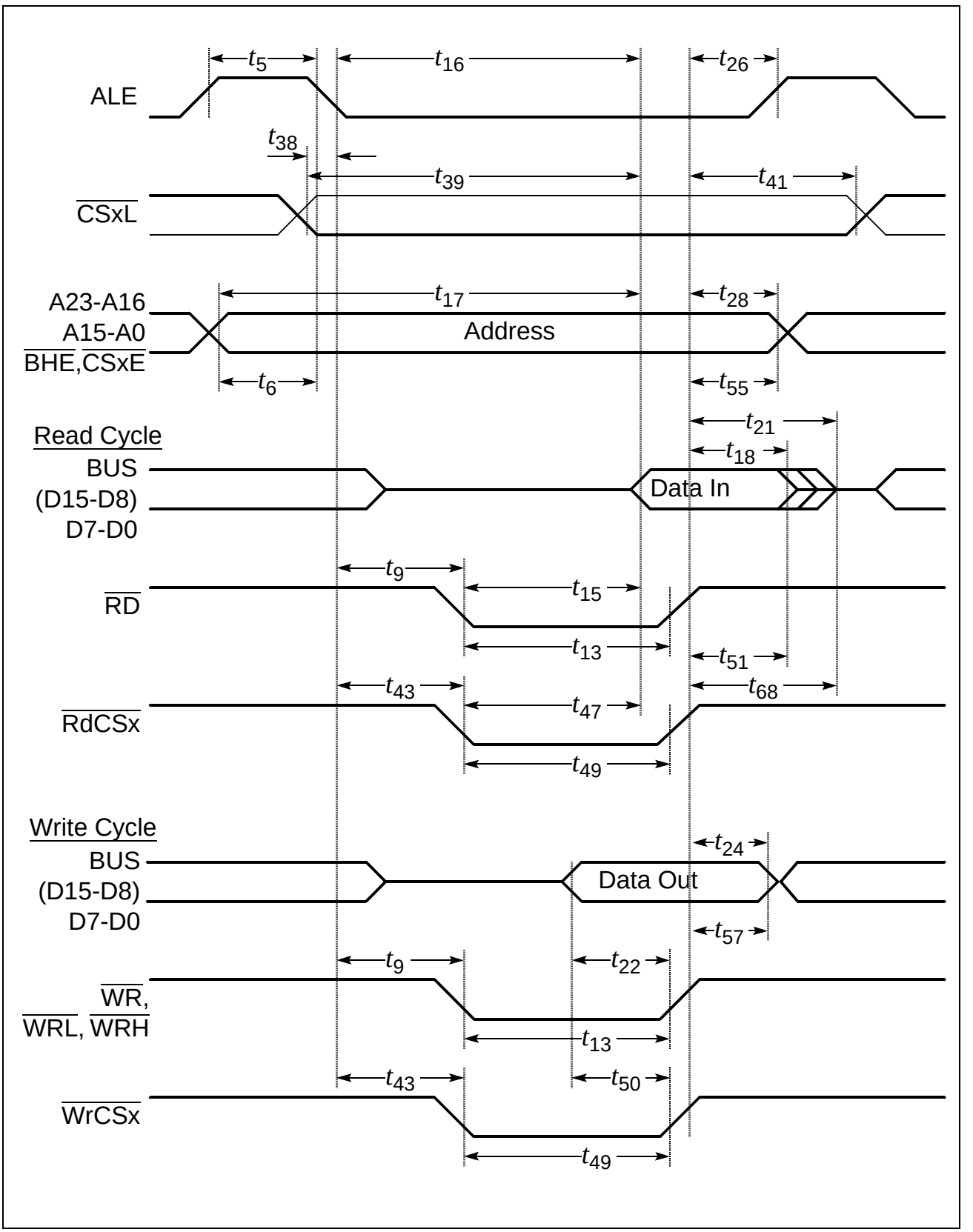

Figure 20 External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Extended ALE

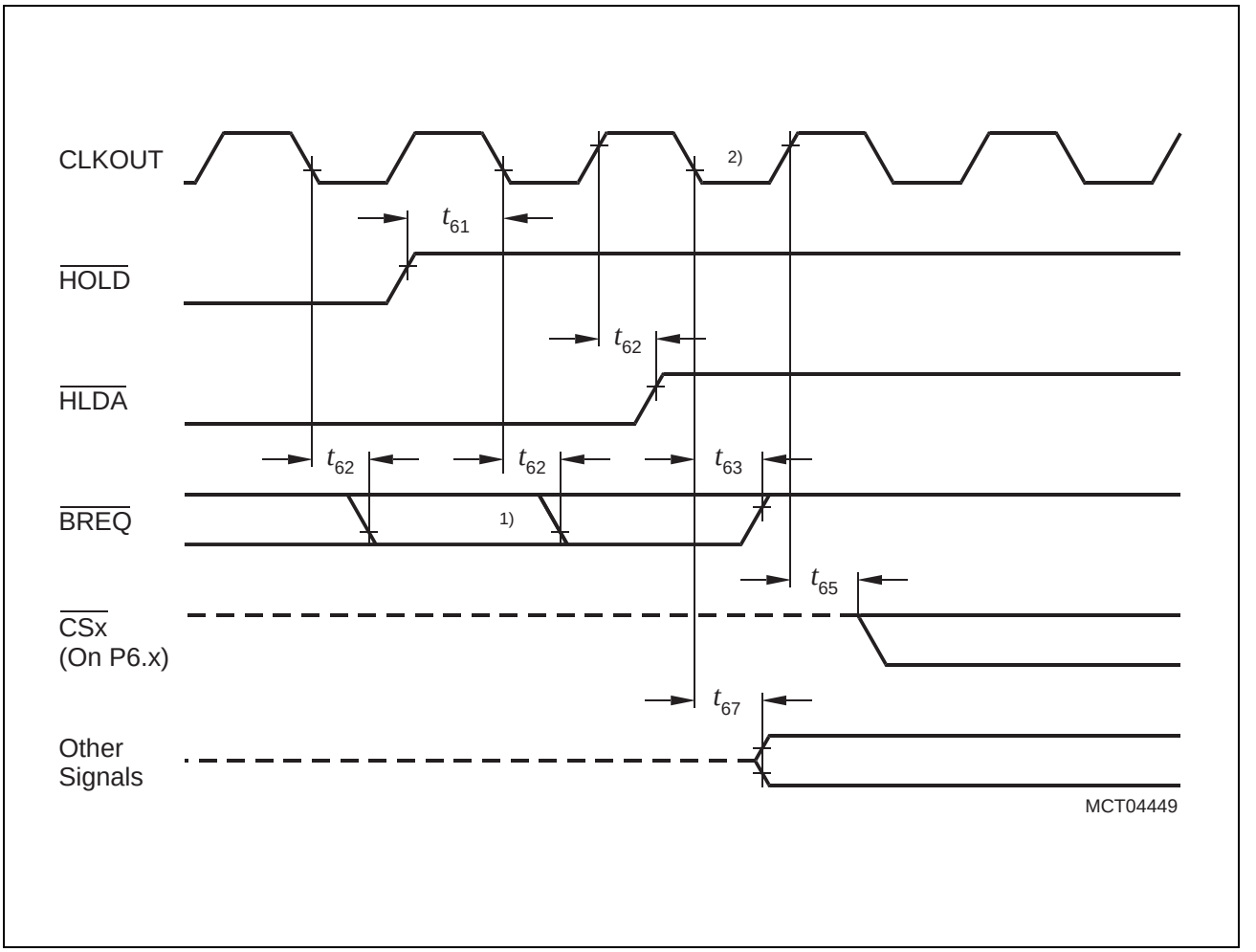

Figure 23 External Bus Arbitration, (Regaining the Bus)

Notes

1) This is the last chance for $\overline{\text{BREQ}}$ to trigger the indicated regain-sequence.
Even if $\overline{\text{BREQ}}$ is activated earlier, the regain-sequence is initiated by $\overline{\text{HOLD}}$ going high.
Please note that $\overline{\text{HOLD}}$ may also be deactivated without the C165 requesting the bus.

2) The next C165 driven bus cycle may start here.