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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x24b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VFQFN Exposed Pad
Supplier Device Package	28-MLP (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f351-gm

1.8. Port Input/Output

C8051F350/1/2/3 devices include 17 I/O pins. Port pins are organized as two byte-wide ports and one 1-bit port. The port pins behave like typical 8051 ports with a few enhancements. Each port pin can be configured as a digital or analog I/O pin. Pins selected as digital I/O can be configured for push-pull or open-drain operation. The “weak pull-ups” that are fixed on typical 8051 devices may be globally disabled to save power.

The Digital Crossbar allows mapping of internal digital system resources to port I/O pins. On-chip counter/timers, serial buses, hardware interrupts, and other digital signals can be configured to appear on the port pins using the Crossbar control registers. This allows the user to select the exact mix of general-purpose port I/O, digital, and analog resources needed for the application.

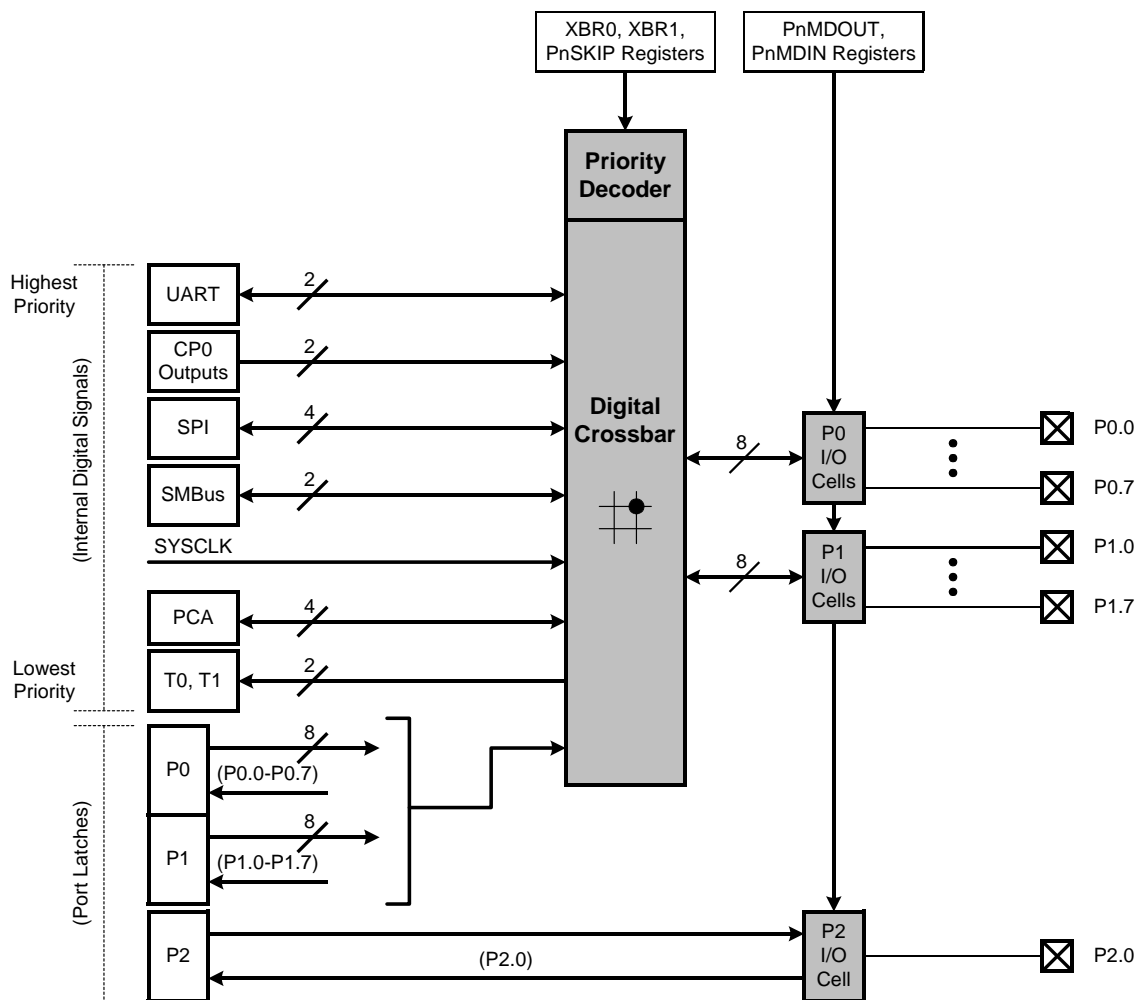


Figure 1.10. Port I/O Functional Block Diagram

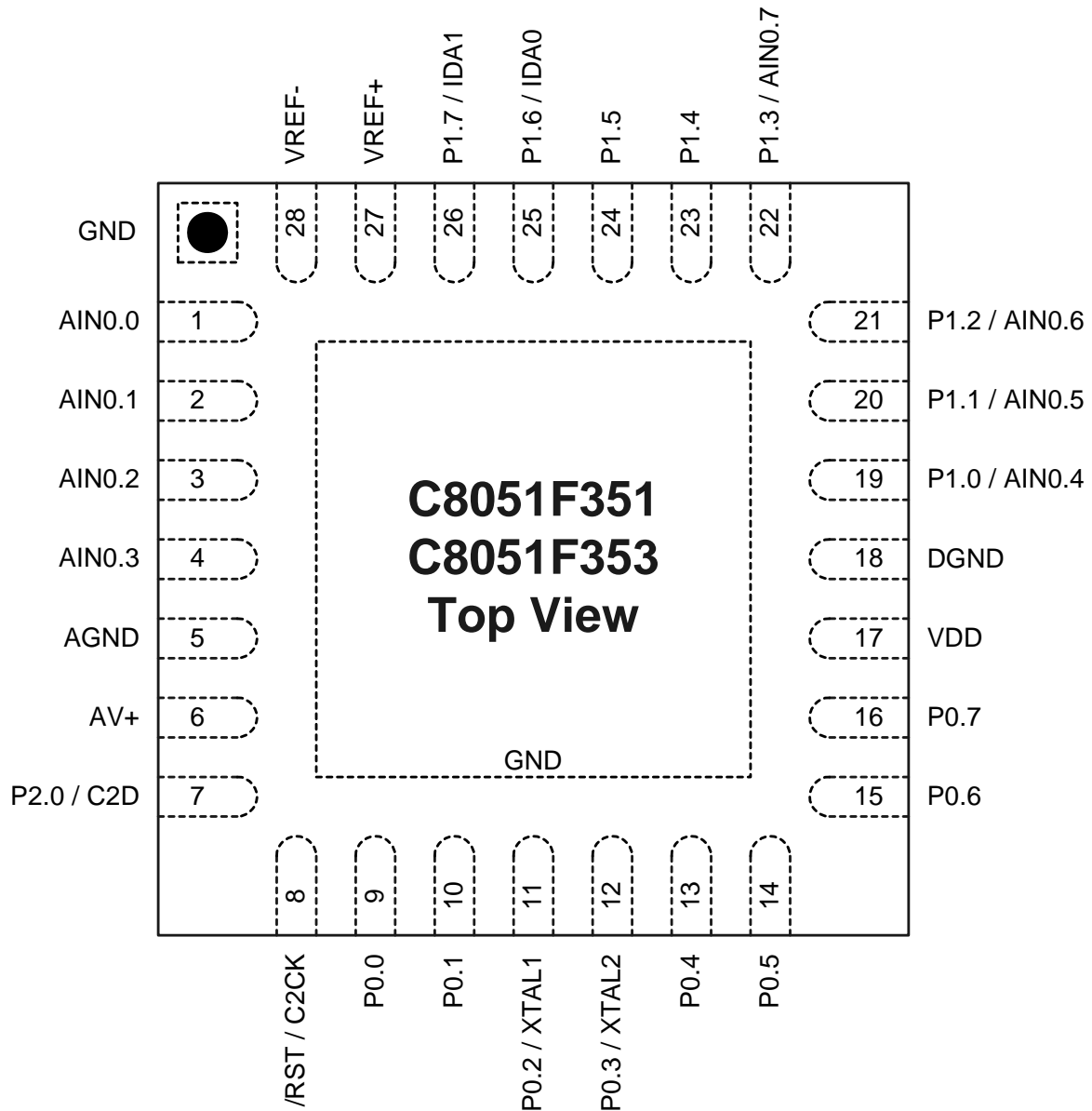


Figure 4.2. QFN-28 Pinout Diagram (Top View)

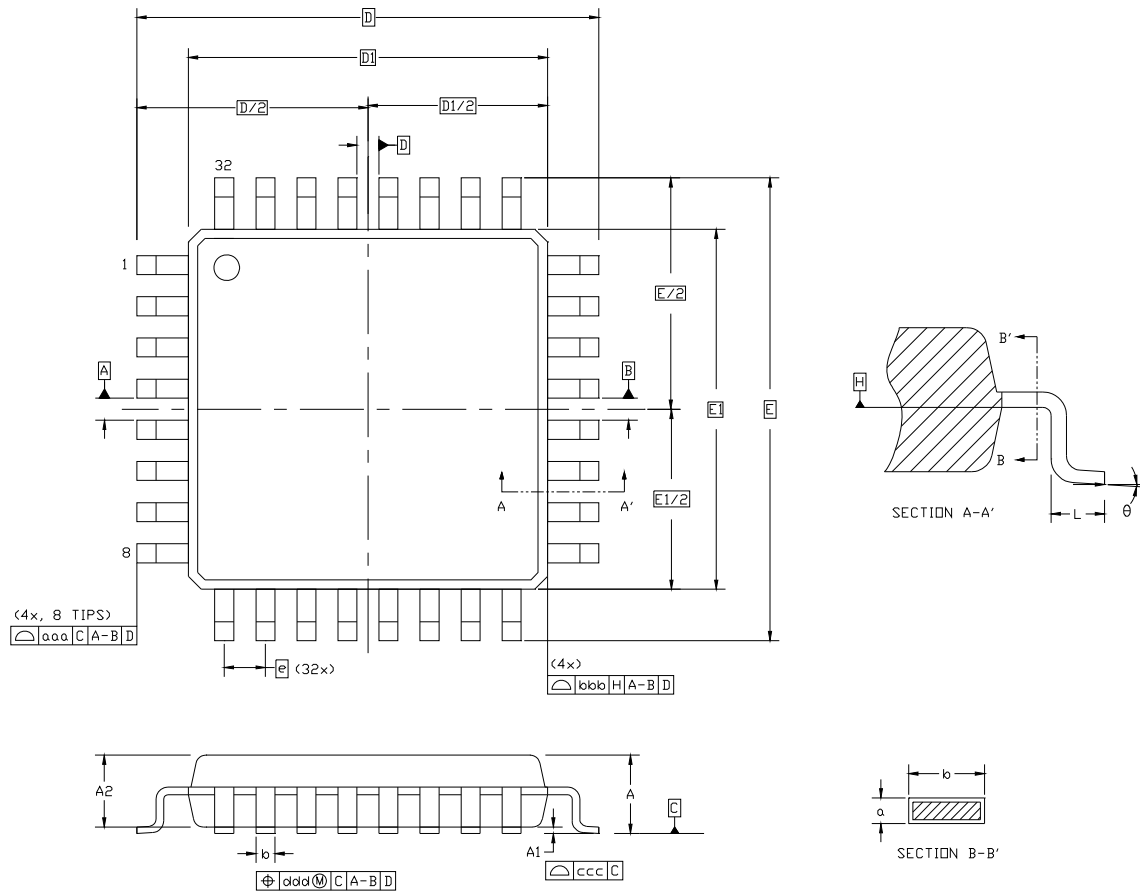


Figure 4.3. LQFP-32 Package Diagram

Table 4.2. LQFP-32 Package Dimensions

	MM		
	MIN	TYP	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	—	0.20
D	—	9.00	—
D1	—	7.00	—
e	—	0.80	—
E	—	9.00	—
E1	—	7.00	—
L	0.45	0.60	0.75

C8051F350/1/2/3

Table 5.3. ADC0 Electrical Characteristics (Continued)

$V_{DD} = AV+ = 3.0$ V, $V_{REF} = 2.5$ V External, PGA Gain = 1, MDCLK = 2.4576 MHz,
Decimation Ratio = 1920, -40 to $+85$ °C unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Power Specifications					
AV+ Supply Current to ADC0		—	230	650	μ A
AV+ Supply Current to Input Buffers (Each Enabled Buffer)		—	90	125	μ A
Power Supply Rejection		80	—	—	dB

Table 5.4. ADC0 SINC3 Filter Typical RMS Noise (μ V)

Decimation Ratio	Output Word Rate*	PGA Gain Setting							
		1	2	4	8	16	32	64	128
1920	10 Hz	2.38	1.23	0.68	0.41	0.24	0.16	0.12	0.11
768	25 Hz	3.90	2.04	1.14	0.68	0.44	0.33	0.28	0.27
640	30 Hz	4.50	2.39	1.31	0.81	0.54	0.42	0.36	0.36
384	50 Hz	6.00	3.21	1.86	1.20	0.86	0.73	0.66	0.66
320	60 Hz	7.26	3.96	2.32	1.51	1.11	0.97	0.89	0.89
192	100 Hz	13.1	7.11	4.24	2.85	2.16	1.91	1.79	1.77
80	240 Hz	93.2	47.7	24.8	13.9	9.34	7.61	6.97	6.67
40	480 Hz	537	267	135	69.5	38.8	25.7	20.9	18.9
20	960 Hz	2974	1586	771	379	196	108	70.0	45.4
*Note: Output Word Rate assuming Modulator Clock frequency = 2.4576 MHz (sampling clock frequency = 19.2 kHz)									

Table 7.1. Voltage Reference Electrical CharacteristicsV_{DD} = 3.0 V; –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Internal Reference					
Output Voltage	25 °C ambient	2.35	2.45	2.50	V
VREF Short-Circuit Current	To AGND	—	9	—	mA
	To AV+	—	20	—	μA
VREF Temperature Coefficient		—	15	—	ppm/°C
Load Regulation	Load = 0 to 200 μA to AGND	—	0.5	—	ppm/μA
VREF Turn-on Time 1 (0.01%)	4.7 μF tantalum, 0.1 μF ceramic bypass capacitors	—	3.9	—	ms
VREF Turn-on Time 2 (0.01%)	0.1 μF ceramic bypass capacitor	—	400	—	μs
VREF Turn-on Time 3 (0.01%)	no bypass capacitor	—	3	—	μs
Power Supply Rejection		—	50	—	dB
External Reference					
Input Voltage Range (VREF+ – VREF–)		1	2.5	AV+	V
Voltage on VREF+ or VREF– pin with respect to AGND		0	—	AV+	V
Input Current	VREF = 2.5 V	—	2	—	μA
Common Mode Rejection Ratio		—	120	—	dB
Power Specifications					
Internal Reference Bias and Band Gap Generator		—	106	135	μA

SFR Definition 9.1. CPT0CN: Comparator0 Control

R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CP0EN	CP0OUT	CP0RIF	CP0FIF	CP0HYP1	CP0HYP0	CP0HYN1	CP0HYN0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SFR Address: 0x9C								
<p>Bit7: CP0EN: Comparator0 Enable Bit. 0: Comparator0 Disabled. 1: Comparator0 Enabled.</p> <p>Bit6: CP0OUT: Comparator0 Output State Flag. 0: Voltage on CP0+ < CP0−. 1: Voltage on CP0+ > CP0−.</p> <p>Bit5: CP0RIF: Comparator0 Rising-Edge Flag. Must be cleared by software. 0: No Comparator0 Rising Edge has occurred since this flag was last cleared. 1: Comparator0 Rising Edge has occurred.</p> <p>Bit4: CP0FIF: Comparator0 Falling-Edge Flag. Must be cleared by software. 0: No Comparator0 Falling-Edge has occurred since this flag was last cleared. 1: Comparator0 Falling-Edge has occurred.</p> <p>Bits3–2: CP0HYP1–0: Comparator0 Positive Hysteresis Control Bits. 00: Positive Hysteresis Disabled. 01: Positive Hysteresis = 5 mV. 10: Positive Hysteresis = 10 mV. 11: Positive Hysteresis = 20 mV.</p> <p>Bits1–0: CP0HYN1–0: Comparator0 Negative Hysteresis Control Bits. 00: Negative Hysteresis Disabled. 01: Negative Hysteresis = 5 mV. 10: Negative Hysteresis = 10 mV. 11: Negative Hysteresis = 20 mV.</p>								

10. CIP-51 Microcontroller

The MCU system controller core is the CIP-51 microcontroller. The CIP-51 is fully compatible with the MCS-51™ instruction set. Standard 803x/805x assemblers and compilers can be used to develop software. The C8051F35x family has a superset of all the peripherals included with a standard 8051. See Section “1. System Overview” on page 17 for more information about the available peripherals. The CIP-51 includes on-chip debug hardware which interfaces directly with the analog and digital subsystems, providing a complete data acquisition or control-system solution in a single integrated circuit.

The CIP-51 Microcontroller core implements the standard 8051 organization and peripherals as well as additional custom peripherals and functions to extend its capability (see Figure 10.1 for a block diagram). The CIP-51 core includes the following features:

- Fully Compatible with MCS-51 Instruction Set
- 50 MIPS Peak Throughput
- 256 Bytes of Internal RAM
- Extended Interrupt Handler
- Reset Input
- Power Management Modes
- Integrated Debug Logic

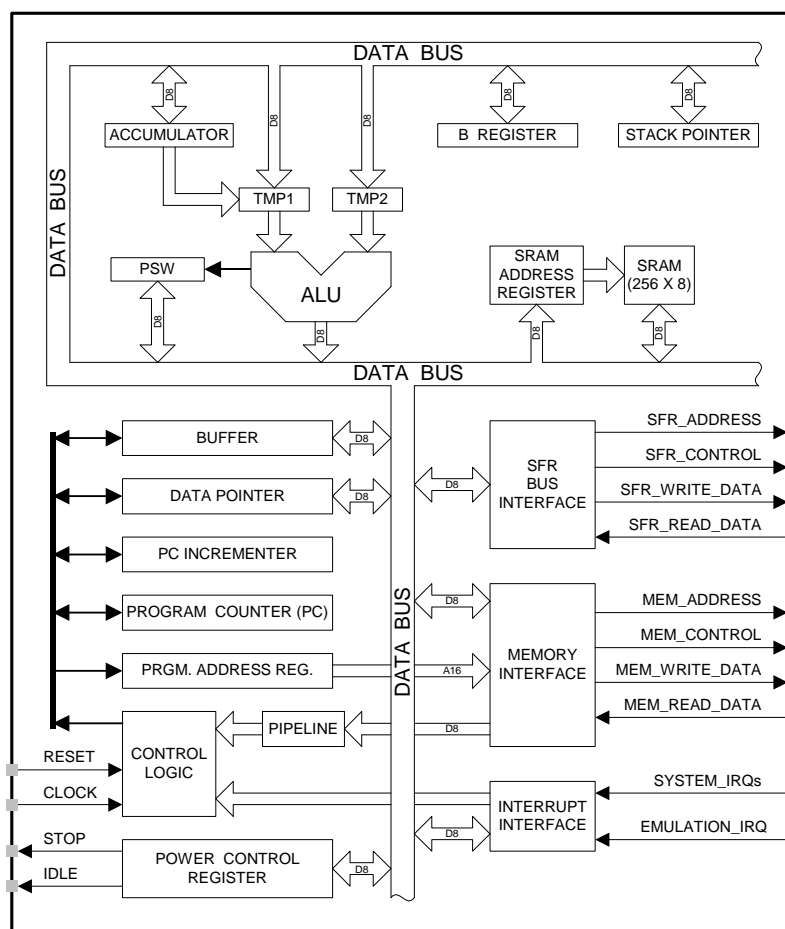


Figure 10.1. CIP-51 Block Diagram

C8051F350/1/2/3

NOTES:

C8051F350/1/2/3

Table 14.1. Reset Electrical Characteristics

–40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
/RST Output Low Voltage	$I_{OL} = 8.5 \text{ mA}$, $V_{DD} = 2.7 \text{ to } 3.6 \text{ V}$	—	—	0.6	V
/RST Input High Voltage		$0.7 \times V_{DD}$	—	—	V
/RST Input Low Voltage		—	—	$0.3 \times V_{DD}$	
/RST Input Pullup Current	/RST = 0.0 V	—	25	40	μA
V_{DD} Monitor Threshold (V_{RST})		2.40	2.55	2.70	V
Missing Clock Detector Timeout	Time from last system clock rising edge to reset initiation	100	220	600	μs
Reset Time Delay	Delay between release of any reset source and code execution at location 0x0000	5.0	—	—	μs
Minimum /RST Low Time to Generate a System Reset		15	—	—	μs
V_{DD} Monitor Turn-on Time		100	—	—	μs
V_{DD} Monitor Supply Current		—	20	50	μA
V_{DD} Ramp Time	$V_{DD} = 0 \text{ V to } V_{RST}$	—	—	1	ms

11. Memory Organization and SFRs

The memory organization of the C8051F350/1/2/3 is similar to that of a standard 8051. There are two separate memory spaces: program memory and data memory. Program and data memory share the same address space but are accessed via different instruction types. The memory map is shown in Figure 11.1.

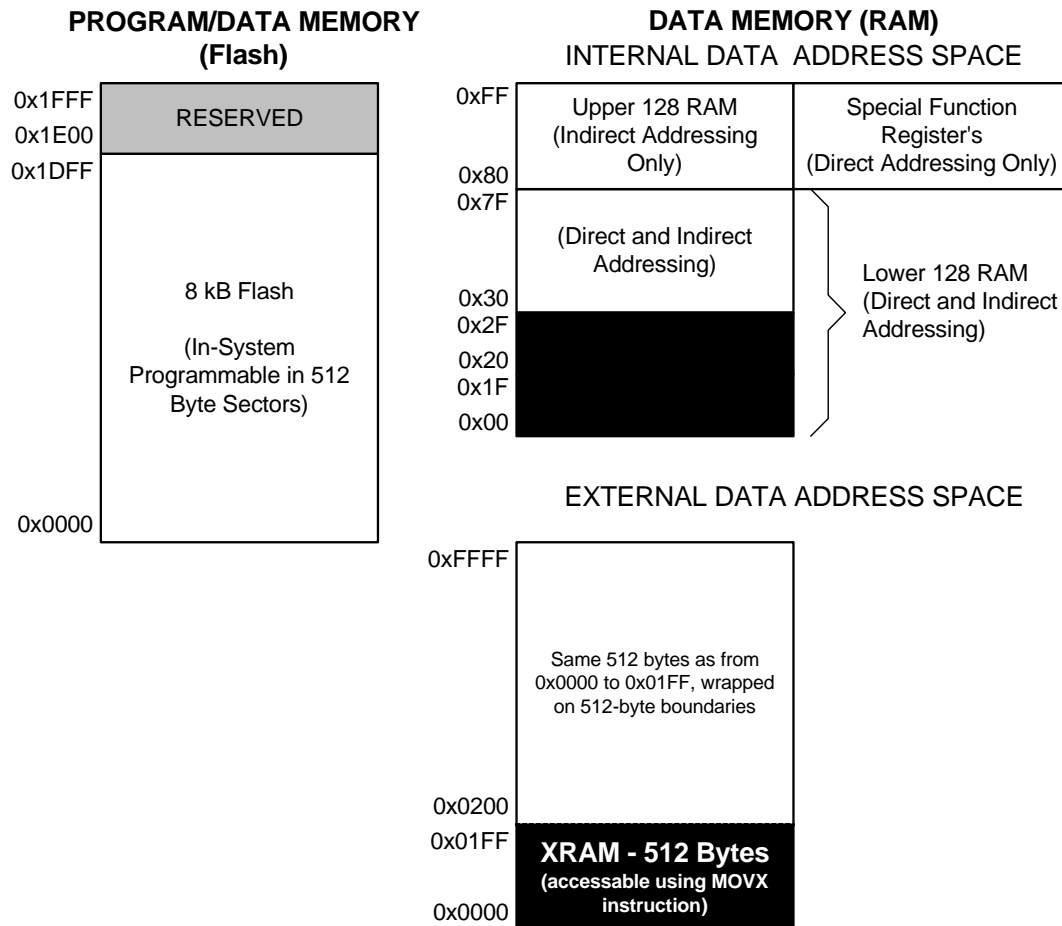


Figure 11.1. Memory Map

11.1. Program Memory

The CIP-51 core has a 64 kB program memory space. The C8051F350/1/2/3 implements 8 kB of this program memory space as in-system, re-programmable Flash memory, organized in a contiguous block from addresses 0x0000 to 0x1DFF. Addresses above 0x1DFF are reserved.

Program memory is normally assumed to be read-only. However, the C8051F350/1/2/3 can write to program memory by setting the Program Store Write Enable bit (PSCTL.0) and using the MOVX write instruction. This feature provides a mechanism for updates to program code and use of the program memory space for non-volatile data storage. Refer to Section “15. Flash Memory” on page 121 for further details.

	P0								P1								P2
PIN I/O	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0
TX0																	
RX0																	
CP0A																	
CP0																	
SCK																	
MISO																	
MOSI																	
NSS*									(*4-Wire SPI Only)								
SDA																	
SCL																	
/SYSCLK																	
CEX0																	
CEX1																	
CEX2																	
ECI																	
T0																	
T1																	
	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	P0SKIP[0:7]								P1SKIP[0:7]								



Port pin potentially assignable to peripheral



Special Function Signals are not assigned by the crossbar.

When these signals are enabled, the CrossBar must be manually configured to skip their corresponding port pins.

Figure 18.4. Crossbar Priority Decoder with Crystal Pins Skipped

Registers XBR0 and XBR1 are used to assign the digital I/O resources to the physical I/O Port pins. Note that when the SMBus is selected, the Crossbar assigns both pins associated with the SMBus (SDA and SCL); when the UART is selected, the Crossbar assigns both pins associated with the UART (TX and RX). UART0 pin assignments are fixed for bootloading purposes: UART TX0 is always assigned to P0.4; UART RX0 is always assigned to P0.5. Comparator outputs are also fixed: CP0A will appear only on P1.4, CP0 will appear only on P1.5. Standard Port I/Os appear contiguously after the prioritized functions have been assigned.

Important Note: The SPI can be operated in either 3-wire or 4-wire modes, pending the state of the NSS-MD1–NSSMD0 bits in register SPI0CN. According to the SPI mode, the NSS signal may or may not be routed to a Port pin.

SFR Definition 18.5. P0MDOUT: Port0 Output Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA4

Bits7–0: Output Configuration Bits for P0.7–P0.0 (respectively): ignored if corresponding bit in register P0MDIN is logic 0.
 0: Corresponding P0.n Output is open-drain.
 1: Corresponding P0.n Output is push-pull.

(Note: When SDA and SCL appear on any of the Port I/O, each are open-drain regardless of the value of P0MDOUT).

SFR Definition 18.6. P0SKIP: Port0 Skip

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD4

Bits7–0: P0SKIP[7:0]: Port0 Crossbar Skip Enable Bits.
 These bits select Port pins to be skipped by the Crossbar Decoder. Port pins used as analog inputs (for ADC or Comparator) or used as special functions (VREF input, external oscillator circuit, CNVSTR input) should be skipped by the Crossbar.
 0: Corresponding P0.n pin is not skipped by the Crossbar.
 1: Corresponding P0.n pin is skipped by the Crossbar.

SFR Definition 18.7. P1: Port1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable
SFR Address: 0x90								

Bits7–0: P1.[7:0]
 Write - Output appears on I/O pins per Crossbar Registers.
 0: Logic Low Output.
 1: Logic High Output (high impedance if corresponding P1MDOUT.n bit = 0).
 Read - Always reads '0' if selected as analog input in register P1MDIN. Directly reads Port pin when configured as digital input.
 0: P1.n pin is logic low.
 1: P1.n pin is logic high.

SFR Definition 18.8. P1MDIN: Port1 Input Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SFR Address: 0xF2								

Bits7–0: Analog Input Configuration Bits for P1.7–P1.0 (respectively).
 Port pins configured as analog inputs have their weak pull-up, digital driver, and digital receiver disabled.
 0: Corresponding P1.n pin is configured as an analog input.
 1: Corresponding P1.n pin is not configured as an analog input.

19.4.2. SMB0CN Control Register

SMB0CN is used to control the interface and to provide status information (see SFR Definition 19.2). The higher four bits of SMB0CN (MASTER, TXMODE, STA, and STO) form a status vector that can be used to jump to service routines. MASTER and TXMODE indicate the master/slave state and transmit/receive modes, respectively.

STA and STO indicate that a START and/or STOP has been detected or generated since the last SMBus interrupt. STA and STO are also used to generate START and STOP conditions when operating as a master. Writing a '1' to STA will cause the SMBus interface to enter Master Mode and generate a START when the bus becomes free (STA is not cleared by hardware after the START is generated). Writing a '1' to STO while in Master Mode will cause the interface to generate a STOP and end the current transfer after the next ACK cycle. If STO and STA are both set (while in Master Mode), a STOP followed by a START will be generated.

As a receiver, writing the ACK bit defines the outgoing ACK value; as a transmitter, reading the ACK bit indicates the value received on the last ACK cycle. ACKRQ is set each time a byte is received, indicating that an outgoing ACK value is needed. When ACKRQ is set, software should write the desired outgoing value to the ACK bit before clearing SI. A NACK will be generated if software does not write the ACK bit before clearing SI. SDA will reflect the defined ACK value immediately following a write to the ACK bit; however SCL will remain low until SI is cleared. If a received slave address is not acknowledged, further slave events will be ignored until the next START is detected.

The ARBLOST bit indicates that the interface has lost an arbitration. This may occur anytime the interface is transmitting (master or slave). A lost arbitration while operating as a slave indicates a bus error condition. ARBLOST is cleared by hardware each time SI is cleared.

The SI bit (SMBus Interrupt Flag) is set at the beginning and end of each transfer, after each byte frame, or when an arbitration is lost; see Table 19.3 for more details.

Important note about the SI bit: The SMBus interface is stalled while SI is set; thus SCL is held low, and the bus is stalled until software clears SI.

Table 19.3 lists all sources for hardware changes to the SMB0CN bits. Refer to Table 19.4 for SMBus status decoding using the SMB0CN register.

19.4.3. Data Register

The SMBus Data register SMB0DAT holds a byte of serial data to be transmitted or one that has just been received. Software may safely read or write to the data register when the SI flag is set. Software should not attempt to access the SMB0DAT register when the SMBus is enabled and the SI flag is cleared to logic 0, as the interface may be in the process of shifting a byte of data into or out of the register.

Data in SMB0DAT is always shifted out MSB first. After a byte has been received, the first bit of received data is located at the MSB of SMB0DAT. While data is being shifted out, data on the bus is simultaneously being shifted in. SMB0DAT always contains the last data byte present on the bus. In the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data or address in SMB0DAT.

SFR Definition 19.3. SMB0DAT: SMBus Data

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC2

Bits7–0: SMB0DAT: SMBus Data.

The SMB0DAT register contains a byte of data to be transmitted on the SMBus serial interface or a byte that has just been received on the SMBus serial interface. The CPU can read from or write to this register whenever the SI serial interrupt flag (SMB0CN.0) is set to logic 1. The serial data in the register remains stable as long as the SI flag is set. When the SI flag is not set, the system may be in the process of shifting data in/out and the CPU should not attempt to access this register.

19.5.3. Slave Receiver Mode

Serial data is received on SDA and the clock is received on SCL. When slave events are enabled (INH = 0), the interface enters Slave Receiver Mode when a START followed by a slave address and direction bit (WRITE in this case) is received. Upon entering Slave Receiver Mode, an interrupt is generated and the ACKRQ bit is set. Software responds to the received slave address with an ACK, or ignores the received slave address with a NACK. If the received slave address is ignored, slave interrupts will be inhibited until the next START is detected. If the received slave address is acknowledged, zero or more data bytes are received. Software must write the ACK bit after each received byte to ACK or NACK the received byte. The interface exits Slave Receiver Mode after receiving a STOP. Note that the interface will switch to Slave Transmitter Mode if SMB0DAT is written while an active Slave Receiver. Figure 19.7 shows a typical Slave Receiver sequence. Two received data bytes are shown, though any number of bytes may be received. Notice that the 'data byte transferred' interrupts occur **before** the ACK cycle in this mode.

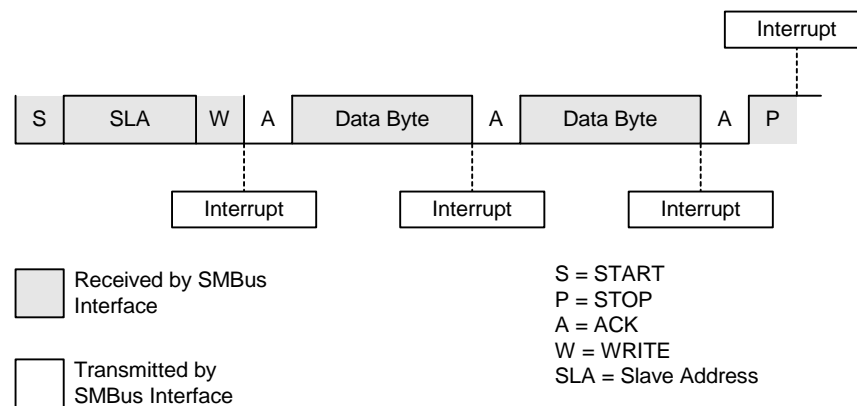


Figure 19.7. Typical Slave Receiver Sequence

22.3. Timer 3

Timer 3 is a 16-bit timer formed by two 8-bit SFRs: TMR3L (low byte) and TMR3H (high byte). Timer 3 may operate in 16-bit auto-reload mode or (split) 8-bit auto-reload mode. The T3SPLIT bit (TMR3CN.3) defines the Timer 3 operation mode.

Timer 3 may be clocked by the system clock, the system clock divided by 12, or the external oscillator source divided by 8. The external clock mode is ideal for real-time clock (RTC) functionality, where the internal oscillator drives the system clock while Timer 3 (and/or the PCA) is clocked by an external precision oscillator. Note that the external oscillator source divided by 8 is synchronized with the system clock.

22.3.1. 16-bit Timer with Auto-Reload

When T3SPLIT (TMR3CN.3) is zero, Timer 3 operates as a 16-bit timer with auto-reload. Timer 3 can be clocked by SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 3 reload registers (TMR3RLH and TMR3RLL) is loaded into the Timer 3 register as shown in Figure 22.6, and the Timer 3 High Byte Overflow Flag (TMR3CN.7) is set. If Timer 3 interrupts are enabled, an interrupt will be generated each Timer 3 overflow. Additionally, if Timer 3 interrupts are enabled and the TF3LEN bit is set (TMR3CN.5), an interrupt will be generated each time the lower 8 bits (TMR3L) overflow from 0xFF to 0x00.

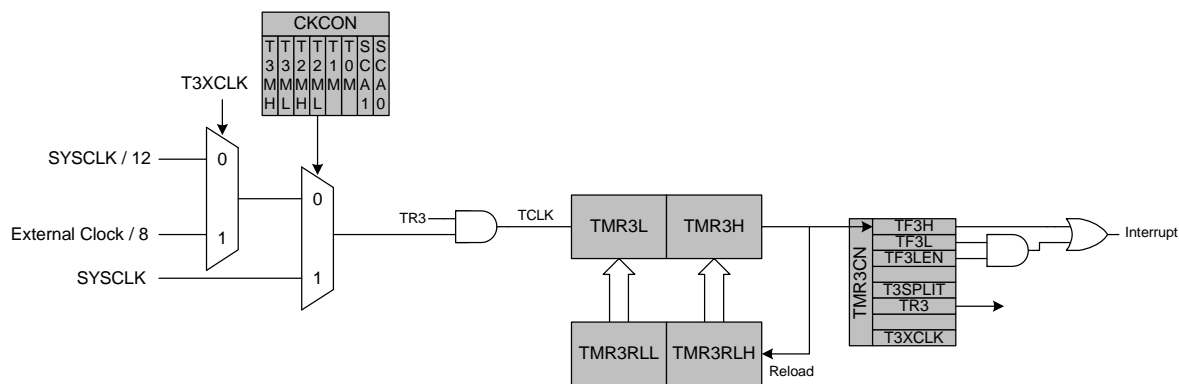


Figure 22.6. Timer 3 16-Bit Mode Block Diagram

SFR Definition 22.13. TMR3CN: Timer 3 Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF3H	TF3L	TF3LEN	—	T3SPLIT	TR3	—	T3XCLK	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x91

- Bit7:** TF3H: Timer 3 High Byte Overflow Flag.
Set by hardware when the Timer 3 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 3 overflows from 0xFFFF to 0x0000. When the Timer 3 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 3 interrupt service routine. TF3H is not automatically cleared by hardware and must be cleared by software.
- Bit6:** TF3L: Timer 3 Low Byte Overflow Flag.
Set by hardware when the Timer 3 low byte overflows from 0xFF to 0x00. When this bit is set, an interrupt will be generated if TF3LEN is set and Timer 3 interrupts are enabled. TF3L will set when the low byte overflows regardless of the Timer 3 mode. This bit is not automatically cleared by hardware.
- Bit5:** TF3LEN: Timer 3 Low Byte Interrupt Enable.
This bit enables/disables Timer 3 Low Byte interrupts. If TF3LEN is set and Timer 3 interrupts are enabled, an interrupt will be generated when the low byte of Timer 3 overflows. This bit should be cleared when operating Timer 3 in 16-bit mode.
0: Timer 3 Low Byte interrupts disabled.
1: Timer 3 Low Byte interrupts enabled.
- Bit4:** UNUSED. Read = 0b. Write = don't care.
- Bit3:** T3SPLIT: Timer 3 Split Mode Enable.
When this bit is set, Timer 3 operates as two 8-bit timers with auto-reload.
0: Timer 3 operates in 16-bit auto-reload mode.
1: Timer 3 operates as two 8-bit auto-reload timers.
- Bit2:** TR3: Timer 3 Run Control.
This bit enables/disables Timer 3. In 8-bit mode, this bit enables/disables TMR3H only; TMR3L is always enabled in this mode.
0: Timer 3 disabled.
1: Timer 3 enabled.
- Bit1:** UNUSED. Read = 0b. Write = don't care.
- Bit0:** T3XCLK: Timer 3 External Clock Select.
This bit selects the external clock source for Timer 3. If Timer 3 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 3 Clock Select bits (T3MH and T3ML in register CKCON) may still be used to select between the external clock and the system clock for either timer.
0: Timer 3 external clock selection is the system clock divided by 12.
1: Timer 3 external clock selection is the external clock divided by 8. Note that the external oscillator source divided by 8 is synchronized with the system clock.

SFR Definition 23.2. PCA0MD: PCA Mode

R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	Reset Value
CIDL	WDTE	WDLCK	—	CPS2	CPS1	CPS0	ECF	01000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xD9

- Bit7: CIDL: PCA Counter/Timer Idle Control.
Specifies PCA behavior when CPU is in Idle Mode.
0: PCA continues to function normally while the system controller is in Idle Mode.
1: PCA operation is suspended while the system controller is in Idle Mode.
- Bit6: WDTE: Watchdog Timer Enable
If this bit is set, PCA Module 2 is used as the watchdog timer.
0: Watchdog Timer disabled.
1: PCA Module 2 enabled as Watchdog Timer.
- Bit5: WDLCK: Watchdog Timer Lock
This bit locks/unlocks the Watchdog Timer Enable. When WDLCK is set, the Watchdog Timer may not be disabled until the next system reset.
0: Watchdog Timer Enable unlocked.
1: Watchdog Timer Enable locked.
- Bit4: UNUSED. Read = 0b, Write = don't care.
- Bits3–1: CPS2–CPS0: PCA Counter/Timer Pulse Select.
These bits select the timebase source for the PCA counter.

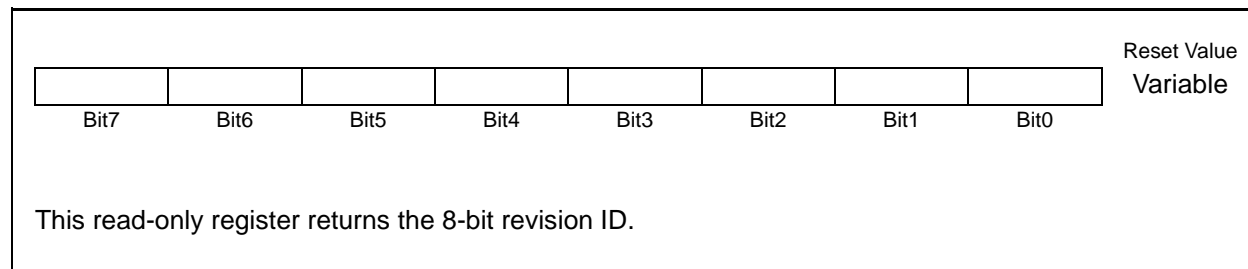
CPS2	CPS1	CPS0	Timebase
0	0	0	System clock divided by 12
0	0	1	System clock divided by 4
0	1	0	Timer 0 overflow
0	1	1	High-to-low transitions on ECI (max rate = system clock divided by 4)
1	0	0	System clock
1	0	1	External clock divided by 8*
1	1	0	Reserved
1	1	1	Reserved

***Note:** External oscillator source divided by 8 is synchronized with the system clock.

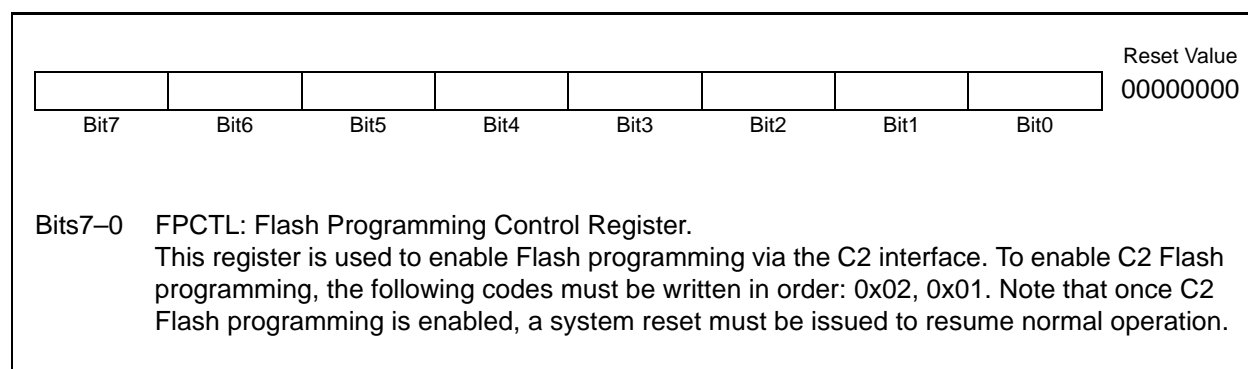
- Bit0: ECF: PCA Counter/Timer Overflow Interrupt Enable.
This bit sets the masking of the PCA Counter/Timer Overflow (CF) interrupt.
0: Disable the CF interrupt.
1: Enable a PCA Counter/Timer Overflow interrupt request when CF (PCA0CN.7) is set.

Note: When the WDTE bit is set to '1', the PCA0MD register cannot be modified. To change the contents of the PCA0MD register, the Watchdog Timer must first be disabled.

C2 Register Definition 25.3. REVID: C2 Revision ID



C2 Register Definition 25.4. FPCTL: C2 Flash Programming Control



C2 Register Definition 25.5. FPDAT: C2 Flash Programming Data

