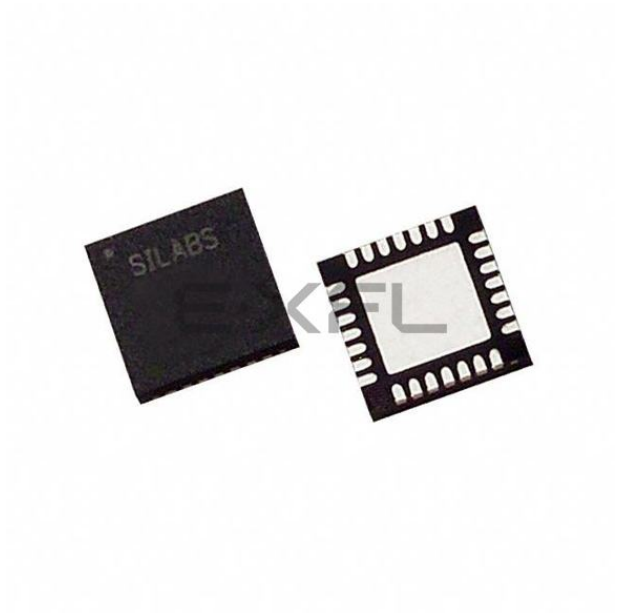

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What is "Embedded - Microcontrollers"?

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x24b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VFQFN Exposed Pad
Supplier Device Package	28-MLP (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f351-gmr

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory	RAM	Calibrated Internal 24.5 MHz Oscillator	Clock Multiplier	SMBus/I2C	SPI	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	24-bit ADC	16-bit ADC	Two 8-bit Current Output DACs	Internal Voltage Reference	Temperature Sensor	Analog Comparator	Lead-free (RoHS Compliant)	Package
C8051F350-GQ	50	8 kB	768	✓	✓	✓	✓	✓	4	✓	17	✓	—	✓	✓	✓	✓	✓	LQFP-32
C8051F351-GM	50	8 kB	768	✓	✓	✓	✓	✓	4	✓	17	✓	—	✓	✓	✓	✓	✓	QFN-28
C8051F352-GQ	50	8 kB	768	✓	✓	✓	✓	✓	4	✓	17	—	✓	✓	✓	✓	✓	✓	LQFP-32
C8051F353-GM	50	8 kB	768	✓	✓	✓	✓	✓	4	✓	17	—	✓	✓	✓	✓	✓	✓	QFN-28

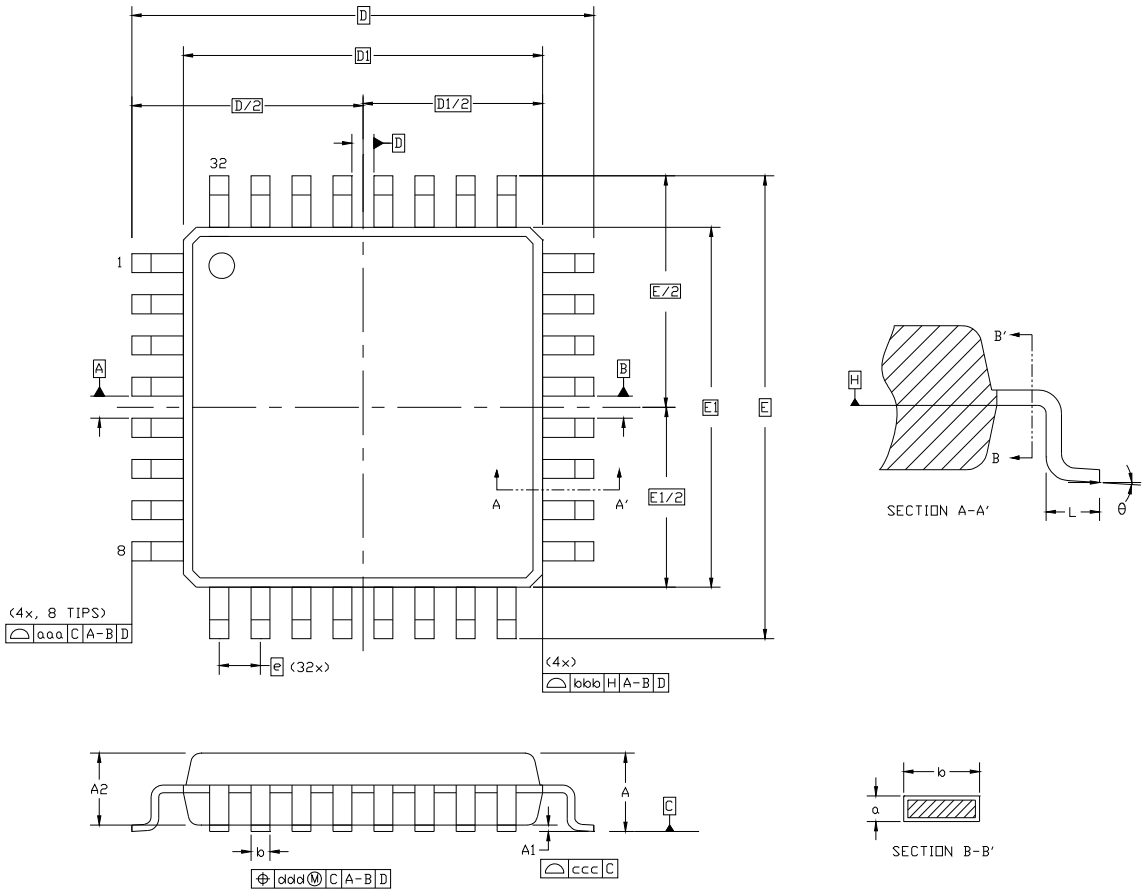


Figure 4.3. LQFP-32 Package Diagram

Table 4.2. LQFP-32 Package Dimensions

	MM		
	MIN	**TYP**	**MAX**
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	—	0.20
D	—	9.00	—
D1	—	7.00	—
e	—	0.80	—
E	—	9.00	—
E1	—	7.00	—
L	0.45	0.60	0.75

5.6. Analog Multiplexer

ADC0 includes analog multiplexer circuitry with independent selection capability for the AIN+ and AIN– inputs. Each input can be connected to one of ten possible input sources: AIN0.0 though AIN0.7, AGND, or the on-chip temperature sensor circuitry (Figure 5.5). The ADC0MUX register (SFR Definition 5.22) controls the input mux selection for both input channels. The multiplexer configuration allows for measurement of single-ended or differential signals. A single-ended measurement can be performed by connecting one of the ADC inputs to AGND. Additionally, the temperature sensor can be measured in single-ended or differential mode. The temperature sensor is automatically enabled when it is selected with the ADC multiplexer. See Section “8. Temperature Sensor’ on page 77 for more details on the temperature sensor.

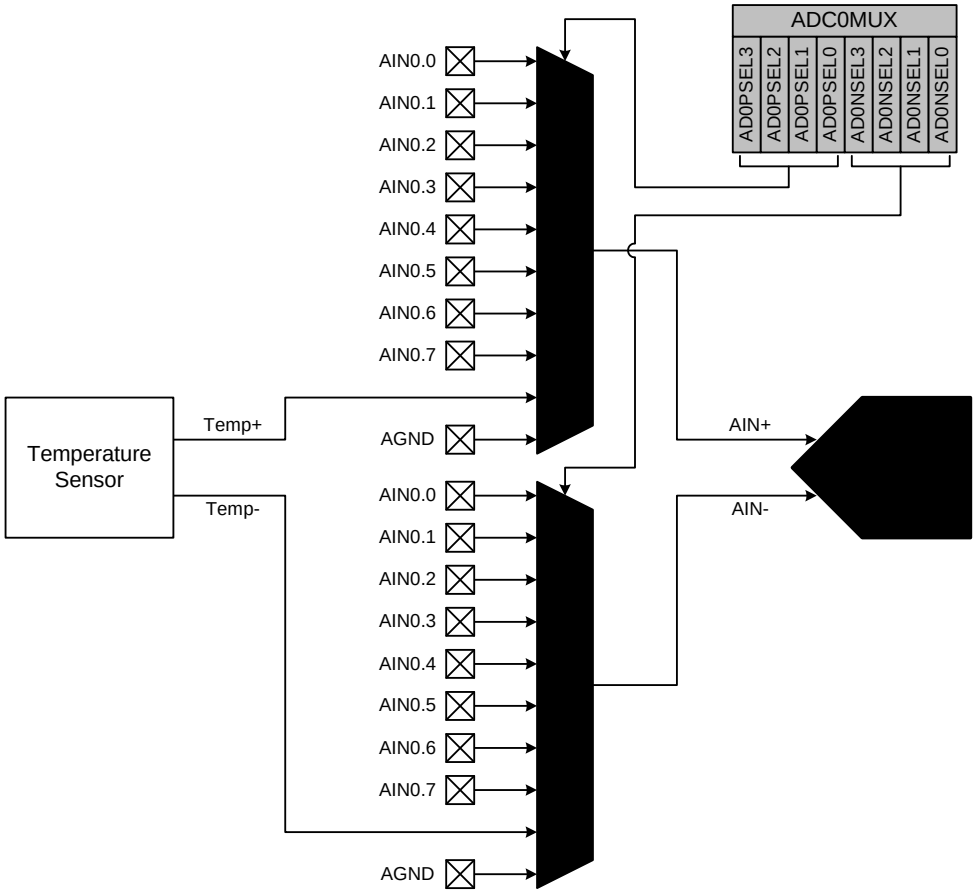


Figure 5.5. ADC0 Multiplexer Connections

Table 5.3. ADC0 Electrical Characteristics (Continued)

V_{DD} = AV+ = 3.0 V, VREF = 2.5 V External, PGA Gain = 1, MDCLK = 2.4576 MHz,
Decimation Ratio = 1920, –40 to +85 °C unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Power Specifications					
AV+ Supply Current to ADC0		—	230	650	µA
AV+ Supply Current to Input Buffers (Each Enabled Buffer)		—	90	125	µA
Power Supply Rejection		80	—	—	dB

Table 5.4. ADC0 SINC3 Filter Typical RMS Noise (µV)

Decimation Ratio	Output Word Rate*	PGA Gain Setting							
		1	2	4	8	16	32	64	128
1920	10 Hz	2.38	1.23	0.68	0.41	0.24	0.16	0.12	0.11
768	25 Hz	3.90	2.04	1.14	0.68	0.44	0.33	0.28	0.27
640	30 Hz	4.50	2.39	1.31	0.81	0.54	0.42	0.36	0.36
384	50 Hz	6.00	3.21	1.86	1.20	0.86	0.73	0.66	0.66
320	60 Hz	7.26	3.96	2.32	1.51	1.11	0.97	0.89	0.89
192	100 Hz	13.1	7.11	4.24	2.85	2.16	1.91	1.79	1.77
80	240 Hz	93.2	47.7	24.8	13.9	9.34	7.61	6.97	6.67
40	480 Hz	537	267	135	69.5	38.8	25.7	20.9	18.9
20	960 Hz	2974	1586	771	379	196	108	70.0	45.4

***Note:** Output Word Rate assuming Modulator Clock frequency = 2.4576 MHz (sampling clock frequency = 19.2 kHz)

SFR Definition 6.3. IDA1CN: IDA1 Control

R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	Reset Value
IDA1EN	IDA1CM			IDA1CSC	—	IDA1OMD		01110000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD7

Bit 7: IDA1EN: IDA1 Enable.
0: IDA1 Disabled.
1: IDA1 Enabled.

Bits 6–4: IDA1CM[2:0]: IDA1 Update Source Select bits.
000: DAC output updates on Timer 0 overflow.
001: DAC output updates on Timer 1 overflow.
010: DAC output updates on Timer 2 overflow.
011: DAC output updates on Timer 3 overflow.
100: DAC output updates on rising edge of CNVSTR.
101: DAC output updates on falling edge of CNVSTR.
110: DAC output updates on any edge of CNVSTR.
111: DAC output updates on write to IDA1.

Bit 3: IDA1CSC: IDA1 Constant Supply Current.
0: Current draw on V_{DD} is dependent on IDA1 Output Word.
1: Current draw on V_{DD} is independent of IDA1 Output Word.

Bit 2: Unused. Read = 0b, Write = Don't Care.

Bits 1:0: IDA1OMD[1:0]: IDA1 Output Mode Select bits.
00: 0.25 mA full-scale output current.
01: 0.5 mA full-scale output current.
10: 1.0 mA full-scale output current.
11: 2.0 mA full-scale output current.

SFR Definition 6.4. IDA1: IDA1 Data Word

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xDD

Bits 7–0: IDA1 Data Word Bits.
Bits 7–0 hold the 8-bit IDA1 Data Word.

Table 10.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
CJNE A, direct, rel	Compare direct byte to A and jump if not equal	3	3/4
CJNE A, #data, rel	Compare immediate to A and jump if not equal	3	3/4
CJNE Rn, #data, rel	Compare immediate to Register and jump if not equal	3	3/4
CJNE @Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	4/5
DJNZ Rn, rel	Decrement Register and jump if not zero	2	2/3
DJNZ direct, rel	Decrement direct byte and jump if not zero	3	3/4
NOP	No operation	1	1

Notes on Registers, Operands and Addressing Modes:

Rn - Register R0–R7 of the currently selected register bank.

@Ri - Data RAM location addressed indirectly through R0 or R1.

rel - 8-bit, signed (two's complement) offset relative to the first byte of the following instruction. Used by SJMP and all conditional jumps.

direct - 8-bit internal data location's address. This could be a direct-access Data RAM location (0x00–0x7F) or an SFR (0x80–0xFF).

#data - 8-bit constant

#data16 - 16-bit constant

bit - Direct-accessed bit in Data RAM or SFR

addr11 - 11-bit destination address used by ACALL and AJMP. The destination must be within the same 2 kB page of program memory as the first byte of the following instruction.

addr16 - 16-bit destination address used by LCALL and LJMP. The destination may be anywhere within the 8 kB program memory space.

There is one unused opcode (0xA5) that performs the same function as NOP.

13. Prefetch Engine

The C8051F350/1/2/3 family of devices incorporate a 2-byte prefetch engine. Because the access time of the Flash memory is 40 ns, and the minimum instruction time is 20 ns, the prefetch engine is necessary for full-speed code execution. Instructions are read from Flash memory two bytes at a time by the prefetch engine, and given to the CIP-51 processor core to execute. When running linear code (code without any jumps or branches), the prefetch engine allows instructions to be executed at full speed. When a code branch occurs, the processor may be stalled for up to two clock cycles while the next set of code bytes is retrieved from Flash memory. The FLRT bit (FLSCL.4) determines how many clock cycles are used to read each set of two code bytes from Flash. When operating from a system clock of 25 MHz or less, the FLRT bit should be set to '0' so that the prefetch engine takes only one clock cycle for each read. When operating with a system clock of greater than 25 MHz (up to 50 MHz), the FLRT bit should be set to '1', so that each prefetch code read lasts for two clock cycles.

SFR Definition 13.1. PFE0CN: Prefetch Engine Control

R	R	R/W	R	R	R	R	R/W	Reset Value
		PFEN					FLBWE	00100000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xE3

Bits 7–6: Unused. Read = 00b; Write = Don't Care
Bit 5: PFEN: Prefetch Enable.
This bit enables the prefetch engine.
0: Prefetch engine is disabled.
1: Prefetch engine is enabled.
Bits 4–1: Unused. Read = 0000b; Write = Don't Care
Bit 0: FLBWE: Flash Block Write Enable.
This bit allows block writes to Flash memory from software.
0: Each byte of a software Flash write is written individually.
1: Flash bytes are written in groups of two.

14.3. External Reset

The external /RST pin provides a means for external circuitry to force the device into a reset state. Asserting an active-low signal on the /RST pin generates a reset; an external pull-up and/or decoupling of the /RST pin may be necessary to avoid erroneous noise-induced resets. See Table 14.1 for complete /RST pin specifications. The PINRSF flag (RSTSRC.0) is set on exit from an external reset.

14.4. Missing Clock Detector Reset

The Missing Clock Detector (MCD) is a one-shot circuit that is triggered by the system clock. If the system clock remains high or low for more than 100 µs, the one-shot will time out and generate a reset. After a MCD reset, the MCDRSF flag (RSTSRC.2) will read ‘1’, signifying the MCD as the reset source; otherwise, this bit reads ‘0’. Writing a ‘1’ to the MCDRSF bit enables the Missing Clock Detector; writing a ‘0’ disables it. The state of the /RST pin is unaffected by this reset.

14.5. Comparator0 Reset

Comparator0 can be configured as a reset source by writing a ‘1’ to the C0RSEF flag (RSTSRC.5). Comparator0 should be enabled and allowed to settle prior to writing to C0RSEF to prevent any turn-on chatter on the output from generating an unwanted reset. The Comparator0 reset is active-low: if the non-inverting input voltage (on CP0+) is less than the inverting input voltage (on CP0–), the device is put into the reset state. After a Comparator0 reset, the C0RSEF flag (RSTSRC.5) will read ‘1’ signifying Comparator0 as the reset source; otherwise, this bit reads ‘0’. The state of the /RST pin is unaffected by this reset.

14.6. PCA Watchdog Timer Reset

The programmable Watchdog Timer (WDT) function of the Programmable Counter Array (PCA) can be used to prevent software from running out of control during a system malfunction. The PCA WDT function can be enabled or disabled by software as described in Section “23.3. Watchdog Timer Mode’ on page 220; the WDT is enabled and clocked by SYSCLK / 12 following any reset. If a system malfunction prevents user software from updating the WDT, a reset is generated and the WDTRSF bit (RSTSRC.5) is set to ‘1’. The state of the /RST pin is unaffected by this reset.

14.7. Flash Error Reset

If a Flash read/write/erase or program read targets an illegal address, a system reset is generated. This may occur due to any of the following:

- A Flash write or erase is attempted above user code space. This occurs when PSWE is set to ‘1’ and a MOVX write operation targets an address above address 0x1DFF.
- A Flash read is attempted above user code space. This occurs when a MOVC operation targets an address above address 0x1DFF.
- A Program read is attempted above user code space. This occurs when user code attempts to branch to an address above 0x1DFF.
- A Flash read, write or erase attempt is restricted due to a Flash security setting (see Section “15.3. Security Options’ on page 123).

The FERROR bit (RSTSRC.6) is set following a Flash error reset. The state of the /RST pin is unaffected by this reset.

14.8. Software Reset

Software may force a reset by writing a ‘1’ to the SWRSF bit (RSTSRC.4). The SWRSF bit will read ‘1’ following a software forced reset. The state of the /RST pin is unaffected by this reset.

15.2. Non-volatile Data Storage

The Flash memory can be used for non-volatile data storage as well as program code. This allows data such as calibration coefficients to be calculated and stored at run time. Data is written using the MOVX write instruction and read using the MOVC instruction. Note: MOVX read instructions always target XRAM.

15.3. Security Options

The CIP-51 provides security options to protect the Flash memory from inadvertent modification by software as well as to prevent the viewing of proprietary program code and constants. The Program Store Write Enable (bit PSWE in register PSCTL) and the Program Store Erase Enable (bit PSEE in register PSCTL) bits protect the Flash memory from accidental modification by software. PSWE must be explicitly set to '1' before software can modify the Flash memory; both PSWE and PSEE must be set to '1' before software can erase Flash memory. Additional security features prevent proprietary program code and data constants from being read or altered across the C2 interface.

A Security Lock Byte located at the last byte of Flash user space offers protection of the Flash program memory from access (reads, writes, or erases) by unprotected code or the C2 interface. The Flash security mechanism allows the user to lock *n* 512-byte Flash pages, starting at page 0 (addresses 0x0000 to 0x01FF), where *n* is the 1's complement number represented by the Security Lock Byte. Note that the page containing the Flash Security Lock Byte is locked when any other Flash pages are locked. See example below.

Security Lock Byte:	11111101b
1's Complement:	00000010b
Flash pages locked:	3 (First two Flash pages + Lock Byte Page)
Addresses locked:	0x0000 to 0x03FF (first two Flash pages) and 0x1C00 to 0x1DFF (Lock Byte Page)

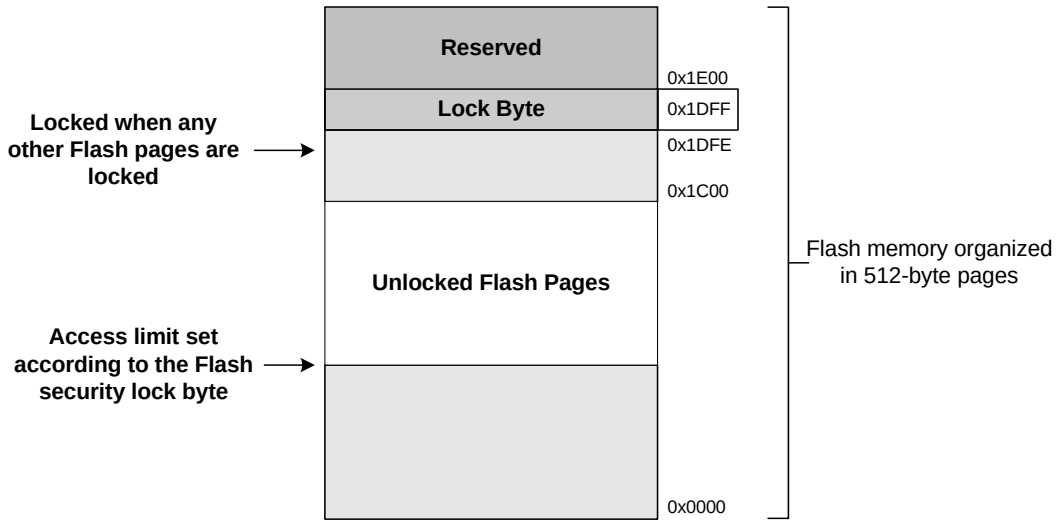


Figure 15.1. Flash Memory Map

NOTES:

Table 11.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
OSCICL	0xB3	Internal Oscillator Calibration	130
OSCICN	0xB2	Internal Oscillator Control	130
OSCXCN	0xB1	External Oscillator Control	134
P0	0x80	Port 0 Latch	145
P0MDIN	0xF1	Port 0 Input Mode Configuration	145
P0MDOUT	0xA4	Port 0 Output Mode Configuration	146
P0SKIP	0xD4	Port 0 Skip	146
P1	0x90	Port 1 Latch	147
P1MDIN	0xF2	Port 1 Input Mode Configuration	147
P1MDOUT	0xA5	Port 1 Output Mode Configuration	148
P1SKIP	0xD5	Port 1 Skip	148
P2	0xA0	Port 2 Latch	149
P2MDOUT	0xA6	Port 2 Output Mode Configuration	149
PCA0CN	0xD8	PCA Control	222
PCA0CPH0	0xEA	PCA Capture 0 High	226
PCA0CPH1	0xEC	PCA Capture 1 High	226
PCA0CPH2	0xEE	PCA Capture 2 High	226
PCA0CPL0	0xE9	PCA Capture 0 Low	226
PCA0CPL1	0xEB	PCA Capture 1 Low	226
PCA0CPL2	0xED	PCA Capture 2 Low	226
PCA0CPM0	0xDA	PCA Module 0 Mode	224
PCA0CPM1	0xDB	PCA Module 1 Mode	224
PCA0CPM2	0xDC	PCA Module 2 Mode	224
PCA0H	0xFA	PCA Counter High	225
PCA0L	0xF9	PCA Counter Low	225
PCA0MD	0xD9	PCA Mode	223
PCON	0x87	Power Control	97
PFE0CN	0xE3	Prefetch Engine Control	113
PSCTL	0x8F	Program Store R/W Control	125
PSW	0xD0	Program Status Word	94
REF0CN	0xD1	Voltage Reference Control	74
RSTSRC	0xEF	Reset Source Configuration/Status	119
SBUF0	0x99	UART0 Data Buffer	177
SCON0	0x98	UART0 Control	176
SMB0CF	0xC1	SMBus Configuration	158
SMB0CN	0xC0	SMBus Control	160
SMB0DAT	0xC2	SMBus Data	162
SP	0x81	Stack Pointer	93
SPI0CFG	0xA1	SPI Configuration	187
SPI0CKR	0xA2	SPI Clock Rate Control	189
SPI0CN	0xF8	SPI Control	188
SPI0DAT	0xA3	SPI Data	190
TCON	0x88	Timer/Counter Control	199
TH0	0x8C	Timer/Counter 0 High	202
TH1	0x8D	Timer/Counter 1 High	202

18.1. Priority Crossbar Decoder

The Priority Crossbar Decoder (Figure 18.3) assigns a priority to each I/O function, starting at the top with UART0. When a digital resource is selected, the least-significant unassigned Port pin is assigned to that resource (excluding UART0, which will be assigned to pins P0.4 and P0.5, and the Comparator0 outputs, which will be assigned to P1.4 and P1.5). If a Port pin is assigned, the Crossbar skips that pin when assigning the next selected resource. Additionally, the Crossbar will skip Port pins whose associated bits in the PnSKIP registers are set. The PnSKIP registers allow software to skip Port pins that are to be used for analog input, dedicated functions, or GPIO.

Important Note on Crossbar Configuration: If a Port pin is claimed by a peripheral without use of the Crossbar, its corresponding PnSKIP bit should be set. This applies to P0.3 and/or P0.2 for the external oscillator, P0.6 for the external CNVSTR signal, P1.6 for IDA0, P1.7 for IDA1, and any selected ADC or comparator inputs. The Crossbar skips selected pins as if they were already assigned, and moves to the next unassigned pin. Figure 18.3 shows the Crossbar Decoder priority with no Port pins skipped (P0SKIP, P1SKIP = 0x00); Figure 18.4 shows the Crossbar Decoder priority with the XTAL1 (P0.2) and XTAL2 (P0.3) pins skipped (P0SKIP = 0x0C).

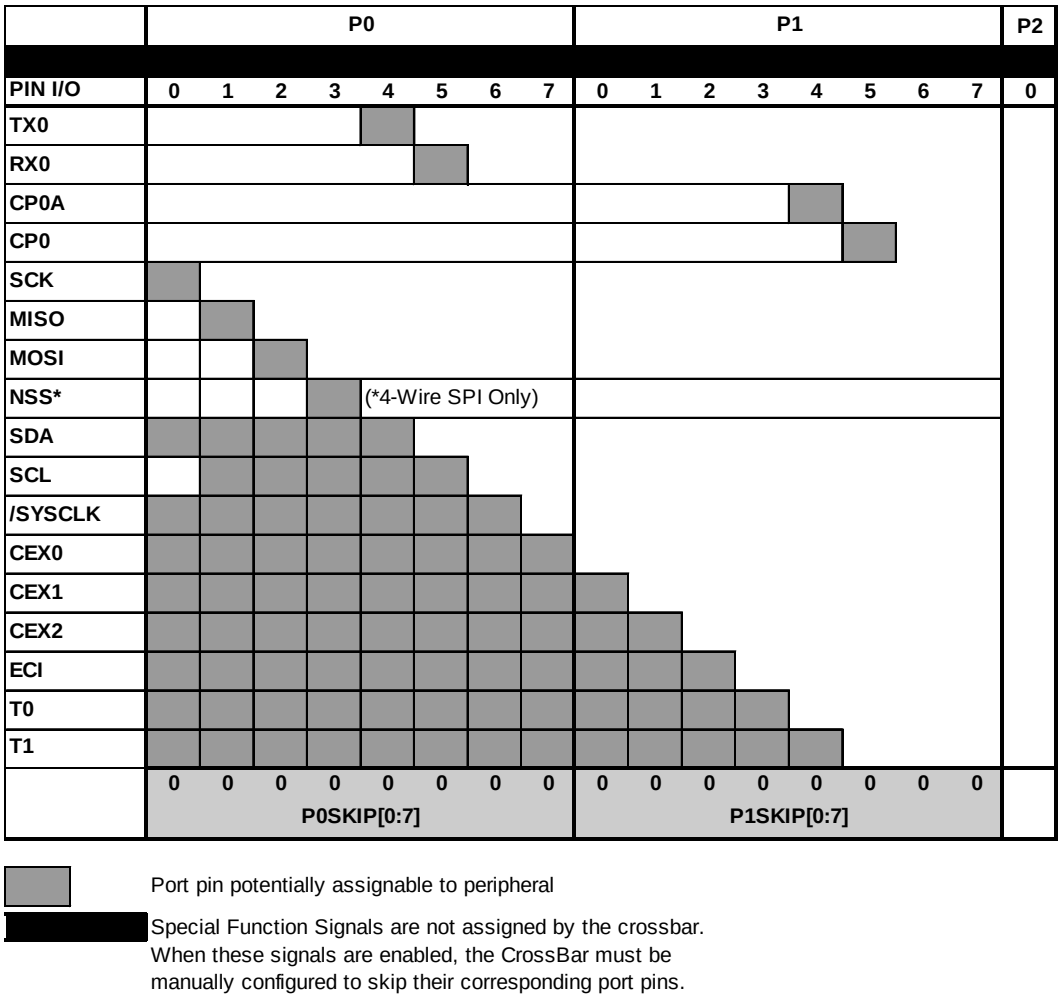
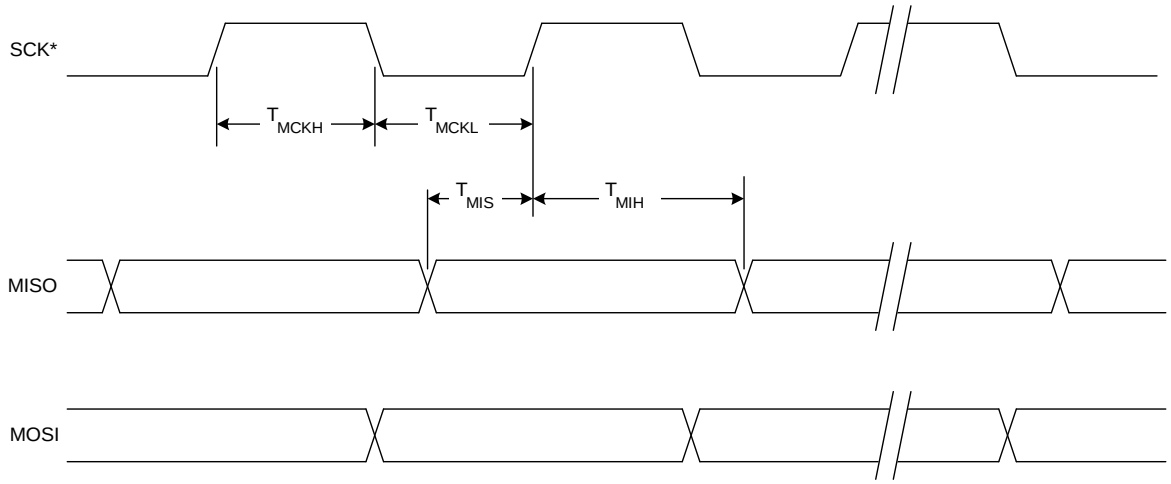
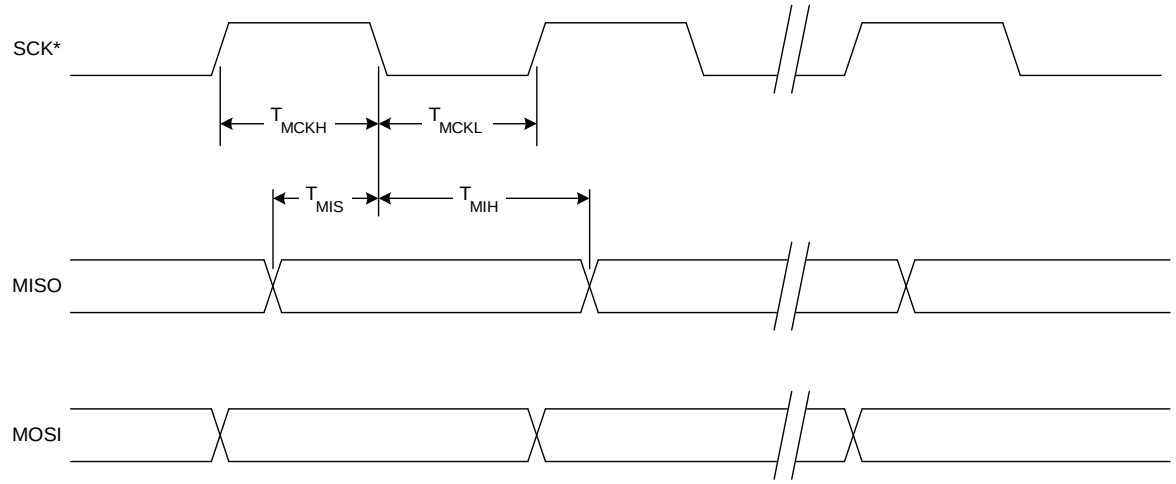


Figure 18.3. Crossbar Priority Decoder with No Pins Skipped



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 21.6. SPI Master Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 21.7. SPI Master Timing (CKPHA = 1)

SFR Definition 22.2. TMOD: Timer Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x89

Bit7: GATE1: Timer 1 Gate Control.
0: Timer 1 enabled when TR1 = 1 irrespective of /INT1 logic level.
1: Timer 1 enabled only when TR1 = 1 AND /INT1 is active as defined by bit IN1PL in register IT01CF (see SFR Definition 12.5).

Bit6: C/T1: Counter/Timer 1 Select.
0: Timer Function: Timer 1 incremented by clock defined by T1M bit (CKCON.4).
1: Counter Function: Timer 1 incremented by high-to-low transitions on external input pin (T1).

Bits5–4: T1M1–T1M0: Timer 1 Mode Select.
These bits select the Timer 1 operation mode.

T1M1	T1M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Timer 1 inactive

Bit3: GATE0: Timer 0 Gate Control.
0: Timer 0 enabled when TR0 = 1 irrespective of /INT0 logic level.
1: Timer 0 enabled only when TR0 = 1 AND /INT0 is active as defined by bit IN0PL in register IT01CF (see SFR Definition 12.5).

Bit2: C/T0: Counter/Timer Select.
0: Timer Function: Timer 0 incremented by clock defined by T0M bit (CKCON.3).
1: Counter Function: Timer 0 incremented by high-to-low transitions on external input pin (T0).

Bits1–0: T0M1–T0M0: Timer 0 Mode Select.
These bits select the Timer 0 operation mode.

T0M1	T0M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Two 8-bit counter/timers

22.2. Timer 2

Timer 2 is a 16-bit timer formed by two 8-bit SFRs: TMR2L (low byte) and TMR2H (high byte). Timer 2 may operate in 16-bit auto-reload mode or (split) 8-bit auto-reload mode. The T2SPLIT bit (TMR2CN.3) defines the Timer 2 operation mode.

Timer 2 may be clocked by the system clock, the system clock divided by 12, or the external oscillator source divided by 8. The external clock mode is ideal for real-time clock (RTC) functionality, where the internal oscillator drives the system clock while Timer 2 (and/or the PCA) is clocked by an external precision oscillator. Note that the external oscillator source divided by 8 is synchronized with the system clock.

22.2.1. 16-bit Timer with Auto-Reload

When T2SPLIT (TMR2CN.3) is zero, Timer 2 operates as a 16-bit timer with auto-reload. Timer 2 can be clocked by SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 2 reload registers (TMR2RLH and TMR2RLL) is loaded into the Timer 2 register as shown in Figure 22.4, and the Timer 2 High Byte Overflow Flag (TMR2CN.7) is set. If Timer 2 interrupts are enabled (if IE.5 is set), an interrupt will be generated on each Timer 2 overflow. Additionally, if Timer 2 interrupts are enabled and the TF2LEN bit is set (TMR2CN.5), an interrupt will be generated each time the lower 8 bits (TMR2L) overflow from 0xFF to 0x00.

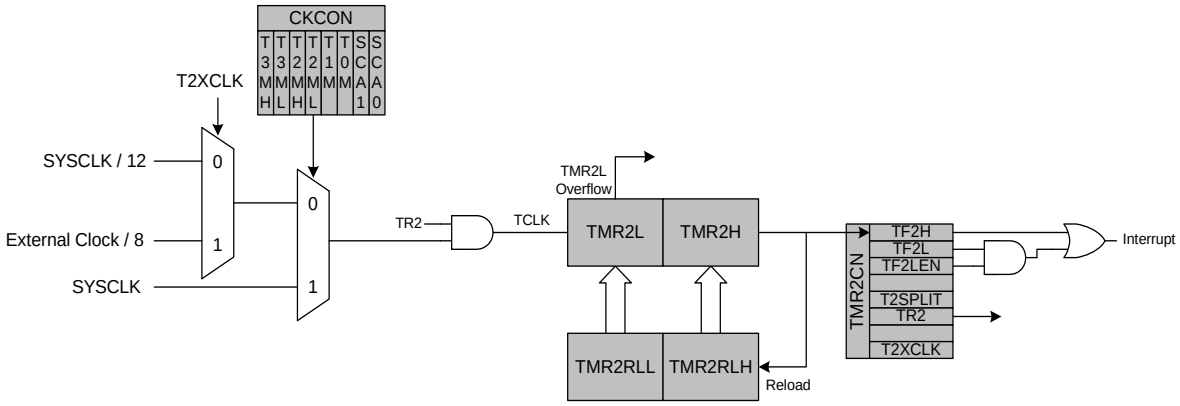


Figure 22.4. Timer 2 16-Bit Mode Block Diagram

23. Programmable Counter Array

The Programmable Counter Array (PCA0) provides enhanced timer functionality while requiring less CPU intervention than the standard 8051 counter/timers. The PCA consists of a dedicated 16-bit counter/timer and three 16-bit capture/compare modules. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the Crossbar to Port I/O when enabled (See Section “18.1. Priority Crossbar Decoder’ on page 139 for details on configuring the Crossbar). The counter/timer is driven by a programmable timebase that can select between six sources: system clock, system clock divided by four, system clock divided by twelve, the external oscillator clock source divided by 8, Timer 0 overflow, or an external clock signal on the ECI input pin. Each capture/compare module may be configured to operate independently in one of six modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, 8-Bit PWM, or 16-Bit PWM (each mode is described in Section “23.2. Capture/Compare Modules’ on page 213). The external oscillator clock option is ideal for real-time clock (RTC) functionality, allowing the PCA to be clocked by a precision external oscillator while the internal oscillator drives the system clock. The PCA is configured and controlled through the system controller's Special Function Registers. The PCA block diagram is shown in Figure 23.1

Important Note: The PCA Module 2 may be used as a watchdog timer (WDT), and is enabled in this mode following a system reset. **Access to certain PCA registers is restricted while WDT mode is enabled**. See Section “23.3. Watchdog Timer Mode’ on page 220 for details.

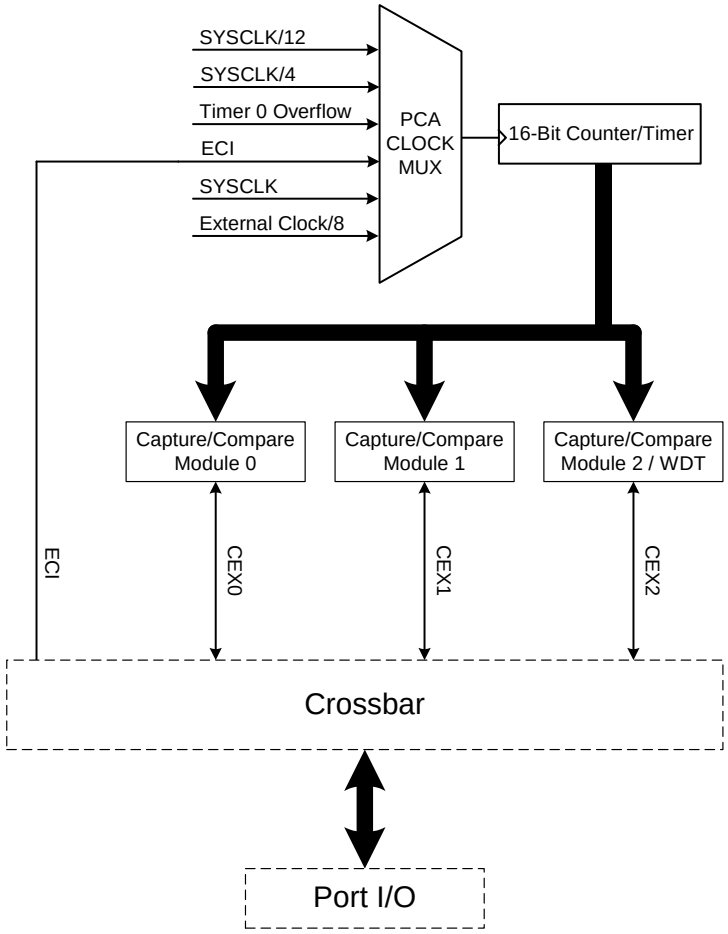


Figure 23.1. PCA Block Diagram

23.2.6. 16-Bit Pulse Width Modulator Mode

A PCA module may also be operated in 16-Bit PWM mode. In this mode, the 16-bit capture/compare module defines the number of PCA clocks for the low time of the PWM signal. When the PCA counter matches the module contents, the output on CEXn is asserted high; when the counter overflows, CEXn is asserted low. To output a varying duty cycle, new value writes should be synchronized with PCA CCFn match interrupts. 16-Bit PWM Mode is enabled by setting the ECOMn, PWMn, and PWM16n bits in the PCA0CPMn register. For a varying duty cycle, match interrupts should be enabled (ECCFn = 1 AND MATn = 1) to help synchronize the capture/compare register writes. The duty cycle for 16-Bit PWM Mode is given by Equation 23.3.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to '0'; writing to PCA0CPHn sets ECOMn to '1'.

$$DutyCycle = \frac{(65536 - PCA0CPn)}{65536}$$

Equation 23.3. 16-Bit PWM Duty Cycle

Using Equation 23.3, the largest duty cycle is 100% (PCA0CPn = 0), and the smallest duty cycle is 0.0015% (PCA0CPn = 0xFFFF). A 0% duty cycle may be generated by clearing the ECOMn bit to '0'.

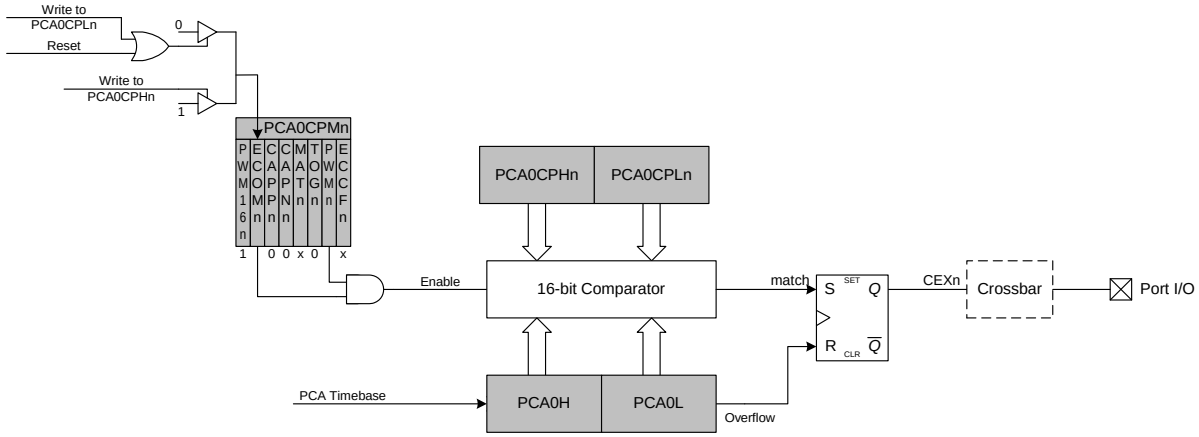


Figure 23.9. PCA 16-Bit PWM Mode

$$Offset = (256 \times PCA0CPL2) + (256 - PCA0L)$$

Equation 23.4. Watchdog Timer Offset in PCA Clocks

The WDT reset is generated when PCA0L overflows while there is a match between PCA0CPH2 and PCA0H. Software may force a WDT reset by writing a '1' to the CCF2 flag (PCA0CN.2) while the WDT is enabled.

23.3.2. Watchdog Timer Usage

To configure the WDT, perform the following tasks:

- Disable the WDT by writing a '0' to the WDTE bit.
- Select the desired PCA clock source (with the CPS2–CPS0 bits).
- Load PCA0CPL2 with the desired WDT update offset value.
- Configure the PCA Idle mode (set CIDL if the WDT should be suspended while the CPU is in Idle mode).
- Enable the WDT by setting the WDTE bit to '1'.
- Write a value to PCA0CPH2 to reload the WDT.

The PCA clock source and Idle mode select cannot be changed while the WDT is enabled. The watchdog timer is enabled by setting the WDTE or WDLCK bits in the PCA0MD register. When WDLCK is set, the WDT cannot be disabled until the next system reset. If WDLCK is not set, the WDT is disabled by clearing the WDTE bit.

The WDT is enabled following any reset. The PCA0 counter clock defaults to the system clock divided by 12, PCA0L defaults to 0x00, and PCA0CPL2 defaults to 0x00. Using Equation 23.4, this results in a WDT timeout interval of 256 PCA clock cycles, or 3072 system clock cycles. Table 23.3 lists some example timeout intervals for typical system clocks.

Table 23.3. Watchdog Timer Timeout Intervals[1]

System Clock (Hz)	PCA0CPL2	Timeout Interval (ms)
24,500,000	255	32.1
24,500,000	128	16.2
24,500,000	32	4.1
18,432,000	255	42.7
18,432,000	128	21.5
18,432,000	32	5.5
11,059,200	255	71.1
11,059,200	128	35.8
11,059,200	32	9.2
3,062,500[2]	255	257
3,062,500[2]	128	129.5
3,062,500[2]	32	33.1
32,000	255	24576
32,000	128	12384
32,000	32	3168

Notes:

1. Assumes SYSCLK / 12 as the PCA clock source, and a PCA0L value of 0x00 at the update time.
2. SYSCLK reset frequency = Internal oscillator frequency divided by 8.

SFR Definition 23.6. PCA0CPLn: PCA Capture Module Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: PCA0CPL0: 0xE9, PCA0CPL1: 0xEB, PCA0CPL2: 0xED

Bits7–0: PCA0CPLn: PCA Capture Module Low Byte.
The PCA0CPLn register holds the low byte (LSB) of the 16-bit capture module n.

SFR Definition 23.7. PCA0CPHn: PCA Capture Module High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: PCA0CPH0: 0xEA, PCA0CPH1: 0xEB, PCA0CPH2: 0xEE

Bits7–0: PCA0CPHn: PCA Capture Module High Byte.
The PCA0CPHn register holds the high byte (MSB) of the 16-bit capture module n.