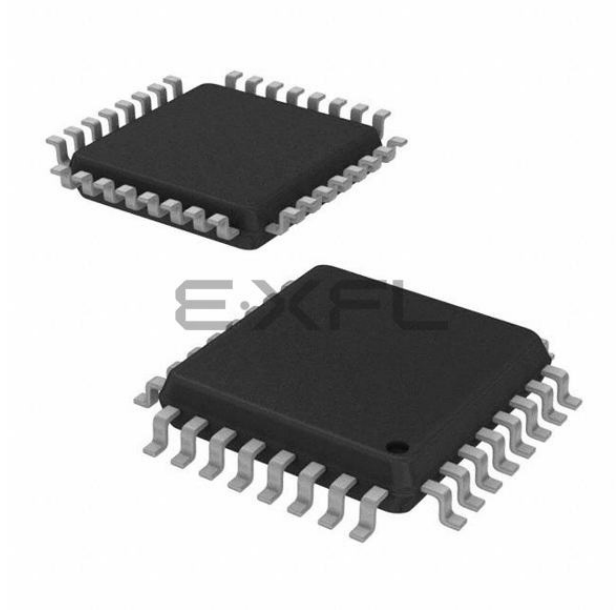

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x16b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f352-gqr

Table of Contents

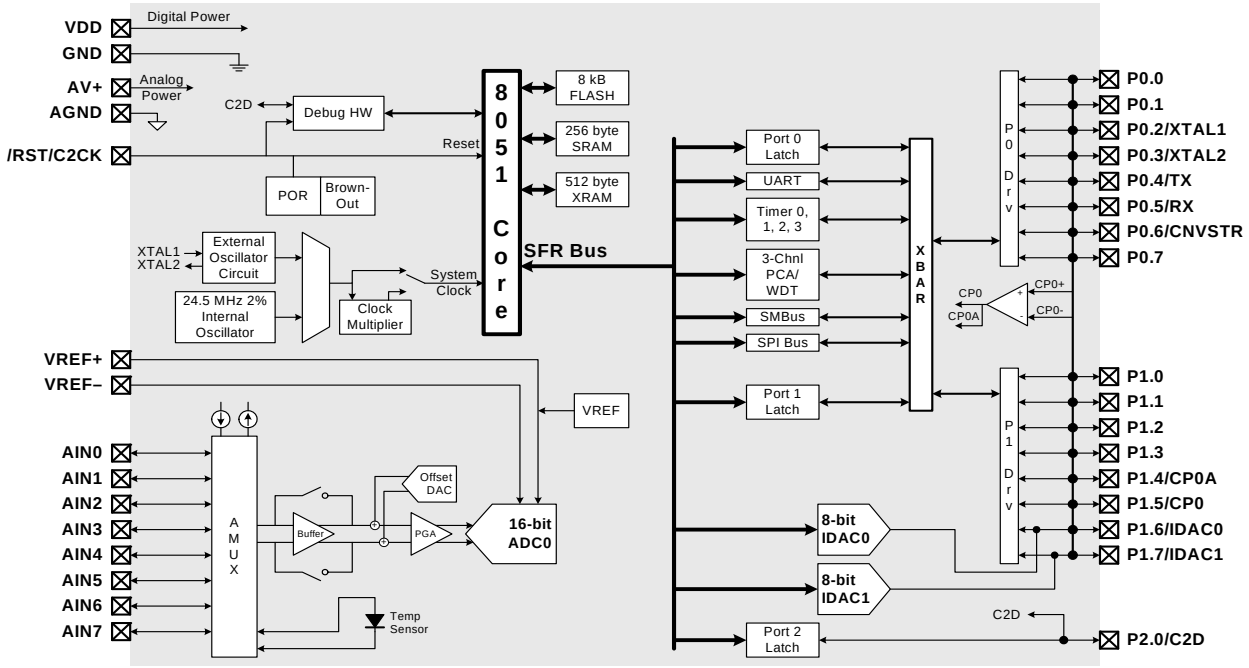


Figure 1.3. C8051F352 Block Diagram

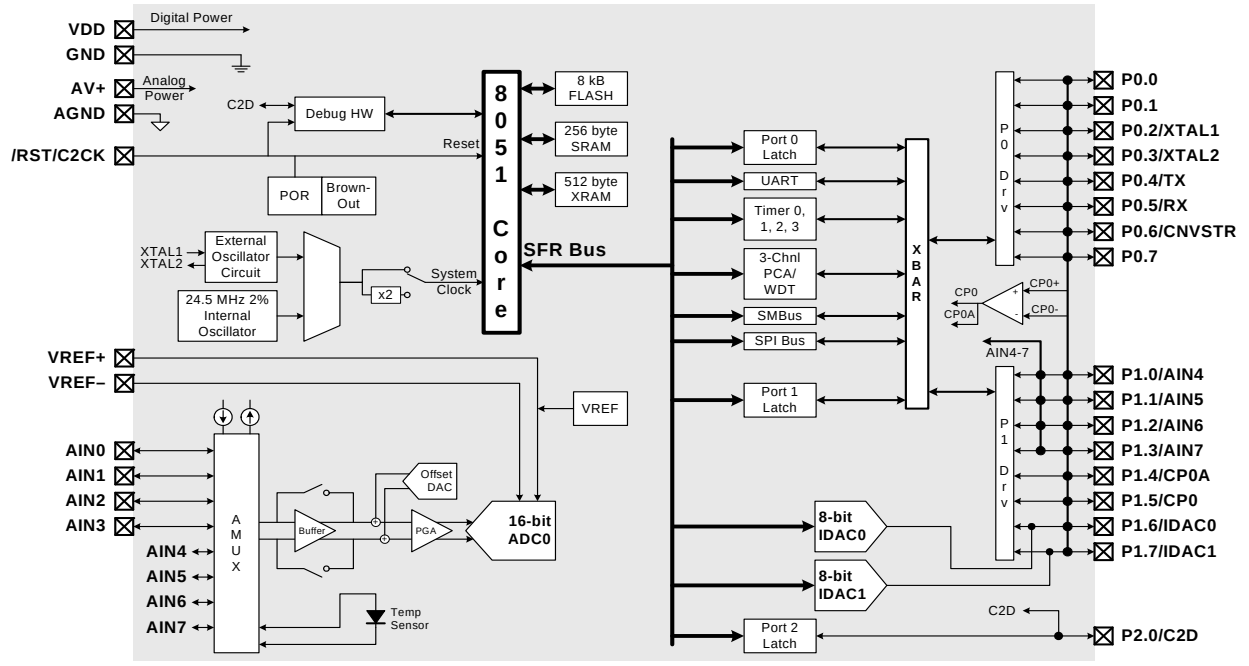


Figure 1.4. C8051F353 Block Diagram

1.6. Programmable Comparator

C8051F350/1/2/3 devices include a software-configurable voltage comparator with an input multiplexer. The Comparator offers programmable response time and hysteresis and two outputs that are optionally available at the Port pins: a synchronous “latched” output (CP0), or an asynchronous “raw” output (CP0A). Comparator interrupts may be generated on rising, falling, or both edges. When in IDLE mode, these interrupts may be used as a “wake-up” source for the processor. Comparator0 may also be configured as a reset source. A block diagram of the Comparator is shown in Figure 1.9.

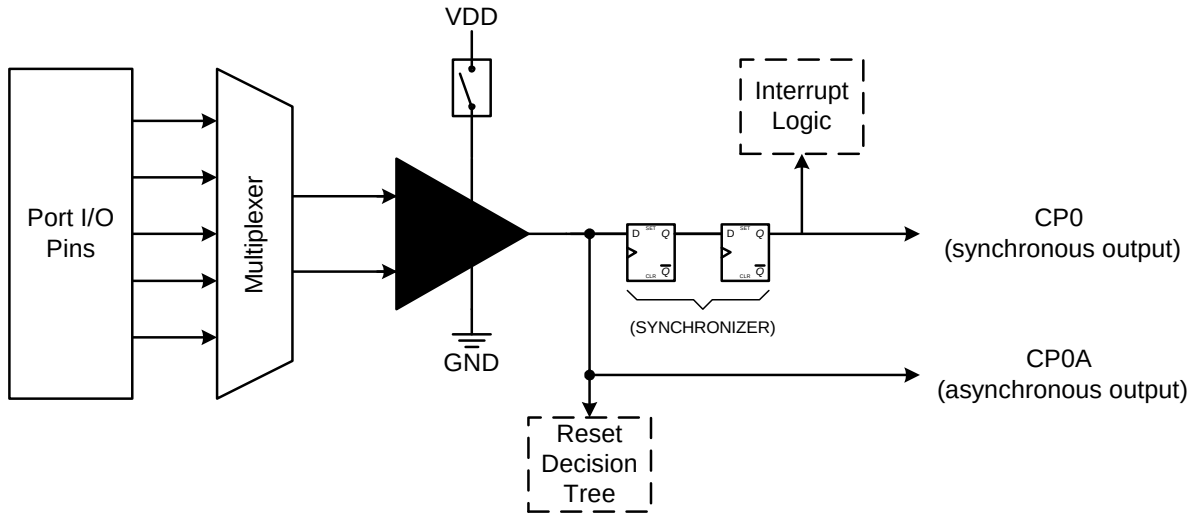


Figure 1.9. Comparator0 Block Diagram

1.7. Serial Ports

The C8051F350/1/2/3 Family includes an SMBus/I2C interface, a full-duplex UART with enhanced baud rate configuration, and an Enhanced SPI interface. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention.

5.3. Performing Conversions

The ADC offers two conversion modes: Single Conversion, and Continuous Conversion. In single conversion mode, a single conversion result is produced for each of the filters (SINC3 and Fast). In continuous conversion mode, the ADC will perform back-to-back conversions until the ADC mode is changed. Procedures for single and continuous conversion modes are detailed in the sections below.

5.3.1. Single Conversions

A single conversion is initiated by writing the ADC System Mode bits (AD0SM) to the “Single Conversion” option. Single conversion mode instructs the ADC to gather enough information to produce a result for the filter that is selected by the AD0ISEL bit. During the conversion, the AD0BUSY flag will be set to ‘1’. The Fast filter results will be available after one period of the ADC’s conversion cycle (determined by the modulator clock and the decimation ratio). The SINC3 filter results will be available after three periods of the ADC’s conversion cycle. The AD0ISEL bit in register ADC0CF determines when the end-of-conversion interrupt will occur, and return the ADC to Idle mode. If the AD0ISEL bit is set to ‘1’, the AD0INT bit will be set to ‘1’ when the Fast filter results are available. If the AD0ISEL bit is cleared to ‘0’, the AD0INT bit will be set to ‘1’ when the SINC3 filter results are available. The AD0SM bits will return to idle mode and the AD0BUSY bit will be cleared to ‘0’ when the selected filter is finished. When using the SINC3 filter, a valid result will also be output by the Fast filter. When using the Fast filter in single-conversion mode, the SINC3 filter results will not be accurate.

5.3.2. Continuous Conversions

Continuous conversions are initiated by writing the ADC System Mode bits (AD0SM) to the “Continuous Conversion” option. In continous conversion mode, the ADC will start a new conversion as soon as each conversion is completed. During the conversions, the AD0BUSY flag will be set to ‘1’. The Fast filter results will be available after one period of the ADC’s conversion cycle, and on every conversion cycle thereafter (determined by the modulator clock and the decimation ratio). The first SINC3 filter result will be available after three periods of the ADC’s conversion cycle, and subsequent SINC3 conversion results will be available at the end of every conversion cycle thereafter. The AD0ISEL bit in register ADC0CF determines when the end-of-conversion interrupts will occur. If the AD0ISEL bit is cleared to ‘0’, the AD0INT bit will be set to ‘1’ when SINC3 filter results are available. If the AD0ISEL bit is set to ‘1’, the AD0INT bit will be set to ‘1’ when Fast filter results are available. Regardless of the setting of the AD0ISEL bit, both filters will update their results registers when new results are available. To stop conversions and exit from continuous conversion mode, the AD0SM bits should be written to Idle mode.

5.3.3. ADC Output

The ADC’s two filters each have their own output data registers. The SINC3 filter results are stored in the ADC0H, ADC0M, and ADC0L registers, while the Fast filter results are stored in the ADC0FH, ADC0FM, and ADC0FL registers. The ADC output can be configured for Unipolar or Bipolar mode using the AD0POL bit in register ADC0CN. Decoding of the ADC output words are shown in Table 5.1 and Table 5.2. The SINC3 filter uses information from the past three conversion cycles to produce an ADC output. The Fast filter uses information from only the current conversion cycle to produce an ADC output. The fast filter reacts more quickly to changes on the analog input, while the SINC3 filter produces lower-noise results.

SFR Definition 5.8. ADC0BUF: ADC0 Input Buffer Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0BPHE	AD0BPLE	AD0BPS		AD0BNHE	AD0BNLE	AD0BNS		00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xBD

Bit 7: AD0BPHE: Positive Channel High Buffer Enable.
0: Positive Channel High Input Buffer Disabled.
1: Positive Channel High Input Buffer Enabled.

Bit 6: AD0BPLE: Positive Channel Low Enable.
0: Positive Channel Low Input Buffer Disabled.
1: Positive Channel Low Input Buffer Enabled.

Bits 5–4: AD0BPS: Positive Channel Input Selection.
00 = Bypass Input Buffer (default).
01 = Select Low Input Buffer Range.
10 = Select High Input Buffer Range.
11 = Reserved.

Bit 3: AD0BNHE: Negative Channel High Buffer Enable.
0: Negative Channel High Input Buffer Disabled.
1: Negative Channel High Input Buffer Enabled.

Bit 2: AD0BNLE: Negative Channel Low Enable.
0: Negative Channel Low Input Buffer Disabled.
1: Negative Channel Low Input Buffer Enabled.

Bits 1–0: AD0BNS: Negative Channel Input Selection.
00 = Bypass Input Buffer (default).
01 = Select Low Input Buffer Range.
10 = Select High Input Buffer Range.
11 = Reserved.

This SFR can only be modified when ADC0 is in IDLE mode.

SFR Definition 7.1. REF0CN: Reference Control

R	R	R	R	R	R	R/W	R/W	Reset Value
—	—	—	—	—	—	BIASE	REFBE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD1

NOTE: Modification of this register is not necessary in most applications. The appropriate circuitry is enabled when it is needed by a peripheral.

Bits7–2: Unused. Read = 000000b; Write = don't care.
Bit1: BIASE: Internal Oscillator Bias Enable.
This bit is ORed with the Internal Oscillator Enable bit to enable the internal oscillator bias generator.
0: Internal Oscillator Bias enable determined by Internal Oscillator Enable bit.
1: Internal Oscillator Bias Generator On.
Bit0: REFBE: Internal Reference Bias Enable Bit.
This bit is ORed with the Enable bits for ADC0, IDAC0, IDAC1, and the Clock Multiplier to enable the internal bandgap generator.
0: Internal Reference Bias enable determined by individual component.
1: Internal Reference Bias enabled.

SFR Definition 9.3. CPT0MX: Comparator0 MUX Selection

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CMX0N3	CMX0N2	CMX0N1	CMX0N0	CMX0P3	CMX0P2	CMX0P1	CMX0P0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x9F

Bits7–4: CMX0N3–CMX0N0: Comparator0 Negative Input MUX Select.
These bits select which Port pin is used as the Comparator0 negative input.

CMX0N3	CMX0N2	CMX0N1	CMX0N0	Negative Input
0	0	0	0	P0.1
0	0	0	1	P0.3
0	0	1	0	P0.5
0	0	1	1	P0.7
0	1	0	0	P1.1
0	1	0	1	P1.3
0	1	1	0	P1.5
0	1	1	1	P1.7
1	x	x	x	None

Bits3–0: CMX0P3–CMX0P0: Comparator0 Positive Input MUX Select.
These bits select which Port pin is used as the Comparator0 positive input.

CMX0P3	CMX0P2	CMX0P1	CMX0P0	Positive Input
0	0	0	0	P0.0
0	0	0	1	P0.2
0	0	1	0	P0.4
0	0	1	1	P0.6
0	1	0	0	P1.0
0	1	0	1	P1.2
0	1	1	0	P1.4
0	1	1	1	P1.6
1	x	x	x	None

Table 10.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
MOV @Ri, A	Move A to indirect RAM	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	2	2
MOV @Ri, #data	Move immediate to indirect RAM	2	2
MOV DPTR, #data16	Load DPTR with 16-bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3
MOVC A, @A+PC	Move code byte relative PC to A	1	3
MOVX A, @Ri	Move external data (8-bit address) to A	1	3
MOVX @Ri, A	Move A to external data (8-bit address)	1	3
MOVX A, @DPTR	Move external data (16-bit address) to A	1	3
MOVX @DPTR, A	Move A to external data (16-bit address)	1	3
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange Register with A	1	1
XCH A, direct	Exchange direct byte with A	2	2
XCH A, @Ri	Exchange indirect RAM with A	1	2
XCHD A, @Ri	Exchange low nibble of indirect RAM with A	1	2
Boolean Manipulation			
CLR C	Clear Carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set Carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement Carry	1	1
CPL bit	Complement direct bit	2	2
ANL C, bit	AND direct bit to Carry	2	2
ANL C, /bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry	2	2
MOV bit, C	Move Carry to direct bit	2	2
JC rel	Jump if Carry is set	2	2/3
JNC rel	Jump if Carry is not set	2	2/3
JB bit, rel	Jump if direct bit is set	3	3/4
JNB bit, rel	Jump if direct bit is not set	3	3/4
JBC bit, rel	Jump if direct bit is set and clear bit	3	3/4
Program Branching			
ACALL addr11	Absolute subroutine call	2	3
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	5
RETI	Return from interrupt	1	5
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
JZ rel	Jump if A equals zero	2	2/3
JNZ rel	Jump if A does not equal zero	2	2/3

Table 11.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
TL0	0x8A	Timer/Counter 0 Low	202
TL1	0x8B	Timer/Counter 1 Low	202
TMOD	0x89	Timer/Counter Mode	200
TMR2CN	0xC8	Timer/Counter 2 Control	205
TMR2H	0xCD	Timer/Counter 2 High	206
TMR2L	0xCC	Timer/Counter 2 Low	206
TMR2RLH	0xCB	Timer/Counter 2 Reload High	206
TMR2RLL	0xCA	Timer/Counter 2 Reload Low	206
TMR3CN	0x91	Timer/Counter 3Control	209
TMR3H	0x95	Timer/Counter 3 High	210
TMR3L	0x94	Timer/Counter 3 Low	210
TMR3RLH	0x93	Timer/Counter 3 Reload High	210
TMR3RLL	0x92	Timer/Counter 3 Reload Low	210
VDM0CN	0xFF	V_{DD} Monitor Control	117
XBR0	0xE1	Port I/O Crossbar Control 0	142
XBR1	0xE2	Port I/O Crossbar Control 1	143

17. Oscillators

C8051F350/1/2/3 devices include a programmable internal oscillator, an external oscillator drive circuit, and a clock multiplier. The internal oscillator can be enabled/disabled and calibrated using the OSCICN and OSCICL registers, as shown in Figure 17.1. The system clock (SYSCLK) can be derived from the internal oscillator, external oscillator circuit, or the clock multiplier. The clock multiplier can produce three possible outputs: Internal Oscillator x 2, External Oscillator x 2, or External Oscillator x 4. Oscillator electrical specifications are given in Table 17.1 on page 136.

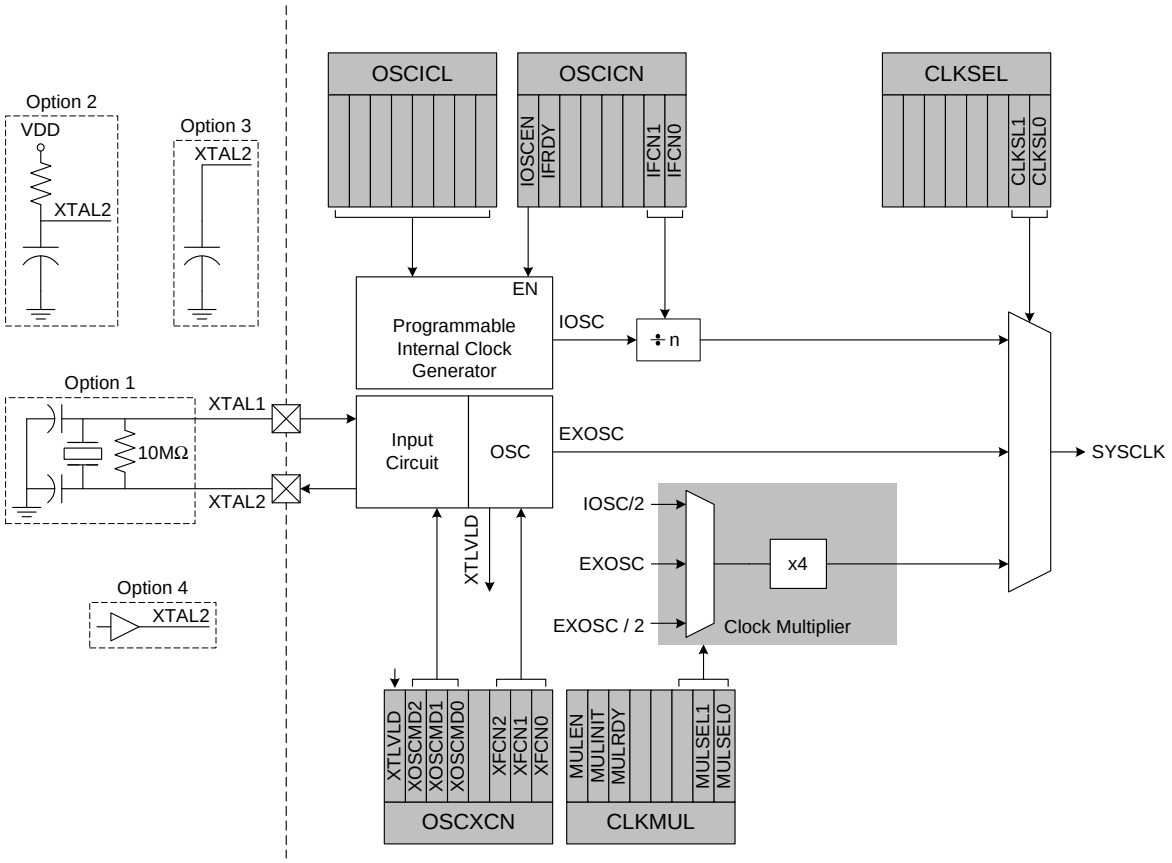


Figure 17.1. Oscillator Diagram

17.1. Programmable Internal Oscillator

All C8051F350/1/2/3 devices include a programmable internal oscillator that defaults as the system clock after a system reset. The internal oscillator period can be programmed via the OSCICL register, shown in SFR Definition 17.2. On C8051F350/1/2/3 devices, OSCICL is factory calibrated to obtain a 24.5 MHz frequency.

Electrical specifications for the precision internal oscillator are given in Table 17.1 on page 136. Note that the system clock may be derived from the programmed internal oscillator divided by 1, 2, 4, or 8, as defined by the IFCN bits in register OSCICN. The divide value defaults to 8 following a reset.

SFR Definition 17.1. OSCICN: Internal Oscillator Control

R/W	R	R	R	R	R	R/W	R/W	Reset Value
IOSCEN	IFRDY	—	—	—	—	IFCN1	IFCN0	11000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xB2

Bit7: IOSCEN: Internal Oscillator Enable Bit.
0: Internal Oscillator Disabled.
1: Internal Oscillator Enabled.
Bit6: IFRDY: Internal Oscillator Frequency Ready Flag.
0: Internal Oscillator is not running at programmed frequency.
1: Internal Oscillator is running at programmed frequency.
Bits5–2: UNUSED. Read = 0000b, Write = don't care.
Bits1–0: IFCN1–0: Internal Oscillator Frequency Control Bits.
00: SYSCLK derived from Internal Oscillator divided by 8.
01: SYSCLK derived from Internal Oscillator divided by 4.
10: SYSCLK derived from Internal Oscillator divided by 2.
11: SYSCLK derived from Internal Oscillator divided by 1.

SFR Definition 17.2. OSCICL: Internal Oscillator Calibration

R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								Variable
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xB3

Bit7: UNUSED. Read = 0. Write = don’t care.
Bits 6–0: OSCICL: Internal Oscillator Calibration Register.
This register determines the internal oscillator period. On C8051F350/1/2/3 devices, the reset value is factory calibrated to generate an internal oscillator frequency of 24.5 MHz.

The capacitors shown in the external crystal configuration provide the load capacitance required by the crystal for correct oscillation. These capacitors are “in series” as seen by the crystal and “in parallel” with the stray capacitance of the XTAL1 and XTAL2 pins.

Note: The load capacitance depends upon the crystal and the manufacturer. Please refer to the crystal datasheet when completing these calculations.

For example, a tuning-fork crystal of 32.768 kHz with a recommended load capacitance of 12.5 pF should use the configuration shown in Figure 17.1, Option 1. The total value of the capacitors and the stray capacitance of the XTAL pins should equal 25 pF. With a stray capacitance of 3 pF per pin, the 22 pF capacitors yield an equivalent capacitance of 12.5 pF across the crystal, as shown in Figure 17.2.

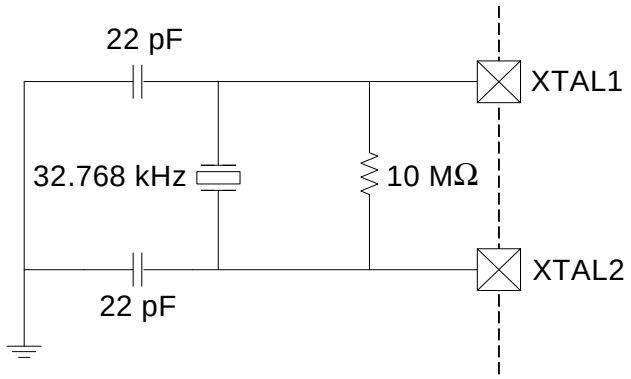


Figure 17.2. 32.768 kHz External Crystal Example

Important note on external crystals: Crystal oscillator circuits are quite sensitive to PCB layout. The crystal should be placed as close as possible to the XTAL pins on the device. The traces should be as short as possible and shielded with ground plane from any other traces which could introduce noise or interference.

19.1. Supporting Documents

It is assumed the reader is familiar with or has access to the following supporting documents:

1. The I2C-Bus and How to Use It (including specifications), Philips Semiconductor.
2. The I2C-Bus Specification -- Version 2.0, Philips Semiconductor.
3. System Management Bus Specification -- Version 1.1, SBS Implementers Forum.

19.2. SMBus Configuration

Figure 19.2 shows a typical SMBus configuration. The SMBus specification allows any recessive voltage between 3.0 V and 5.0 V; different devices on the bus may operate at different voltage levels. The bi-directional SCL (serial clock) and SDA (serial data) lines must be connected to a positive power supply voltage through a pull-up resistor or similar circuit. Every device connected to the bus must have an open-drain or open-collector output for both the SCL and SDA lines, so that both are pulled high (recessive state) when the bus is free. The maximum number of devices on the bus is limited only by the requirement that the rise and fall times on the bus not exceed 300 ns and 1000 ns, respectively.

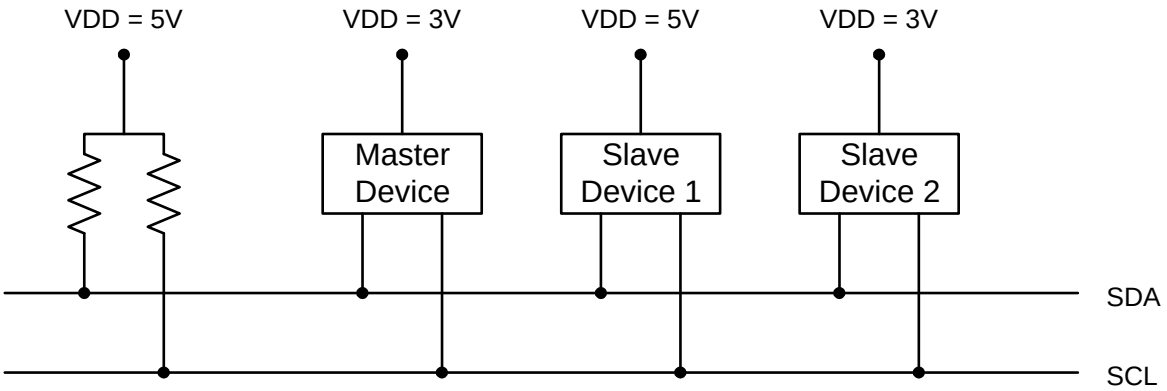


Figure 19.2. Typical SMBus Configuration

19.3. SMBus Operation

Two types of data transfers are possible: data transfers from a master transmitter to an addressed slave receiver (WRITE), and data transfers from an addressed slave transmitter to a master receiver (READ). The master device initiates both types of data transfers and provides the serial clock pulses on SCL. The SMBus interface may operate as a master or a slave, and multiple master devices on the same bus are supported. If two or more masters attempt to initiate a data transfer simultaneously, an arbitration scheme is employed with a single master always winning the arbitration. Note that it is not necessary to specify one device as the Master in a system; any device who transmits a START and a slave address becomes the master for the duration of that transfer.

A typical SMBus transaction consists of a START condition followed by an address byte (Bits7–1: 7-bit slave address; Bit0: R/W direction bit), one or more bytes of data, and a STOP condition. Each byte that is received (by a master or slave) must be acknowledged (ACK) with a low SDA during a high SCL (see Figure 19.3). If the receiving device does not ACK, the transmitting device will read a NACK (not acknowledge), which is a high SDA during a high SCL.

SFR Definition 19.1. SMB0CF: SMBus Clock/Configuration

R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	Reset Value
ENSMB	INH	BUSY	EXTHOLD	SMBTOE	SMBFTE	SMBCS1	SMBCS0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC1

Bit7: ENSMB: SMBus Enable.
This bit enables/disables the SMBus interface. When enabled, the interface constantly monitors the SDA and SCL pins.
0: SMBus interface disabled.
1: SMBus interface enabled.

Bit6: INH: SMBus Slave Inhibit.
When this bit is set to logic 1, the SMBus does not generate an interrupt when slave events occur. This effectively removes the SMBus slave from the bus. Master Mode interrupts are not affected.
0: SMBus Slave Mode enabled.
1: SMBus Slave Mode inhibited.

Bit5: BUSY: SMBus Busy Indicator.
This bit is set to logic 1 by hardware when a transfer is in progress. It is cleared to logic 0 when a STOP or free-timeout is sensed.

Bit4: EXTHOLD: SMBus Setup and Hold Time Extension Enable.
This bit controls the SDA setup and hold times according to Table 19.2.
0: SDA Extended Setup and Hold Times disabled.
1: SDA Extended Setup and Hold Times enabled.

Bit3: SMBTOE: SMBus SCL Timeout Detection Enable.
This bit enables SCL low timeout detection. If set to logic 1, the SMBus forces Timer 3 to reload while SCL is high and allows Timer 3 to count when SCL goes low. If Timer 3 is configured in split mode (T3SPLIT is set), only the high byte of Timer 3 is held in reload while SCL is high. Timer 3 should be programmed to generate interrupts at 25 ms, and the Timer 3 interrupt service routine should reset SMBus communication.

Bit2: SMBFTE: SMBus Free Timeout Detection Enable.
When this bit is set to logic 1, the bus will be considered free if SCL and SDA remain high for more than 10 SMBus clock source periods.

Bits1–0: SMBCS1–SMBCS0: SMBus Clock Source Selection.
These two bits select the SMBus clock source, which is used to generate the SMBus bit rate. The selected device should be configured according to Equation 19.1.

SMBCS1	SMBCS0	SMBus Clock Source
0	0	Timer 0 Overflow
0	1	Timer 1 Overflow
1	0	Timer 2 High Byte Overflow
1	1	Timer 2 Low Byte Overflow

21.5. Serial Clock Timing

Four combinations of serial clock phase and polarity can be selected using the clock control bits in the SPI0 Configuration Register (SPI0CFG). The CKPHA bit (SPI0CFG.5) selects one of two clock phases (edge used to latch the data). The CKPOL bit (SPI0CFG.4) selects between an active-high or active-low clock. Both master and slave devices must be configured to use the same clock phase and polarity. SPI0 should be disabled (by clearing the SPIEN bit, SPI0CN.0) when changing the clock phase or polarity. The clock and data line relationships are shown in Figure 21.5.

The SPI0 Clock Rate Register (SPI0CKR) as shown in SFR Definition 21.3 controls the master mode serial clock frequency. This register is ignored when operating in slave mode. When the SPI is configured as a master, the maximum data transfer rate (bits/sec) is one-half the system clock frequency or 12.5 MHz, whichever is slower. When the SPI is configured as a slave, the maximum data transfer rate (bits/sec) for full-duplex operation is 1/10 the system clock frequency, provided that the master issues SCK, NSS (in 4-wire slave mode), and the serial input data synchronously with the slave's system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less than 1/10 the system clock frequency. In the special case where the master only wants to transmit data to the slave and does not need to receive data from the slave (i.e. half-duplex operation), the SPI slave can receive data at a maximum data transfer rate (bits/sec) of 1/4 the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the slave's system clock.

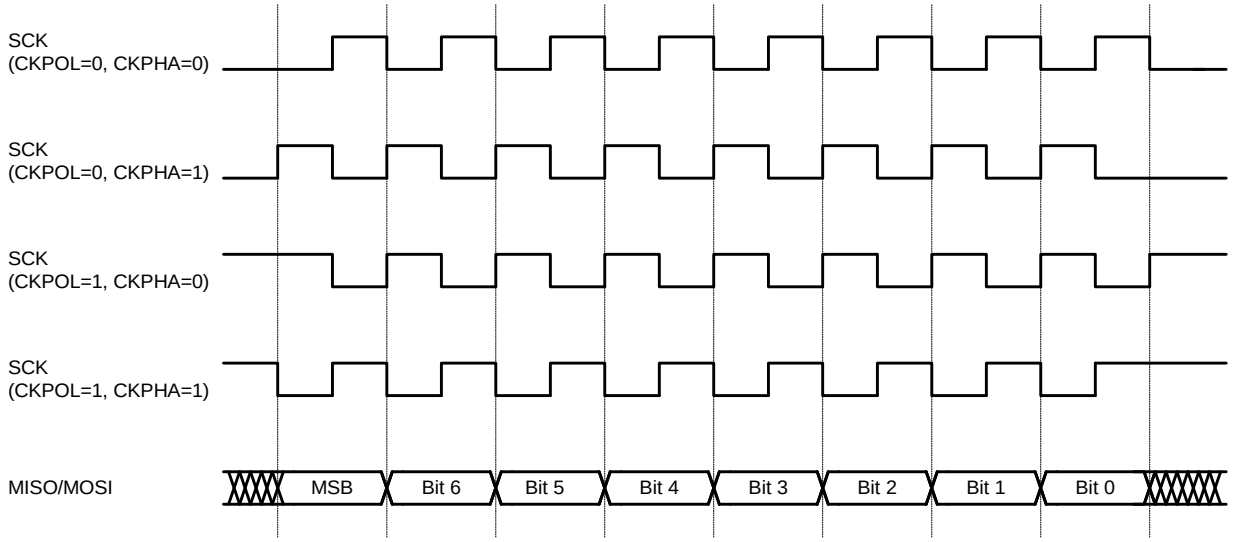


Figure 21.5. Data/Clock Timing Relationship

21.6. SPI Special Function Registers

SPI0 is accessed and controlled through four special function registers in the system controller: SPI0CN Control Register, SPI0DAT Data Register, SPI0CFG Configuration Register, and SPI0CKR Clock Rate Register. The four special function registers related to the operation of the SPI0 Bus are described in the following figures.

SFR Definition 21.1. SPI0CFG: SPI0 Configuration

R	R/W	R/W	R/W	R	R	R	R	Reset Value
SPIBSY	MSTEN	CKPHA	CKPOL	SLVSEL	NSSIN	SRMT	RXBMT	00000111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA1

Bit 7: SPIBSY: SPI Busy (read only).
This bit is set to logic 1 when a SPI transfer is in progress (Master or Slave Mode).

Bit 6: MSTEN: Master Mode Enable.
0: Disable master mode. Operate in slave mode.
1: Enable master mode. Operate as a master.

Bit 5: CKPHA: SPI0 Clock Phase.
This bit controls the SPI0 clock phase.
0: Data centered on first edge of SCK period.*
1: Data centered on second edge of SCK period.*

Bit 4: CKPOL: SPI0 Clock Polarity.
This bit controls the SPI0 clock polarity.
0: SCK line low in idle state.
1: SCK line high in idle state.

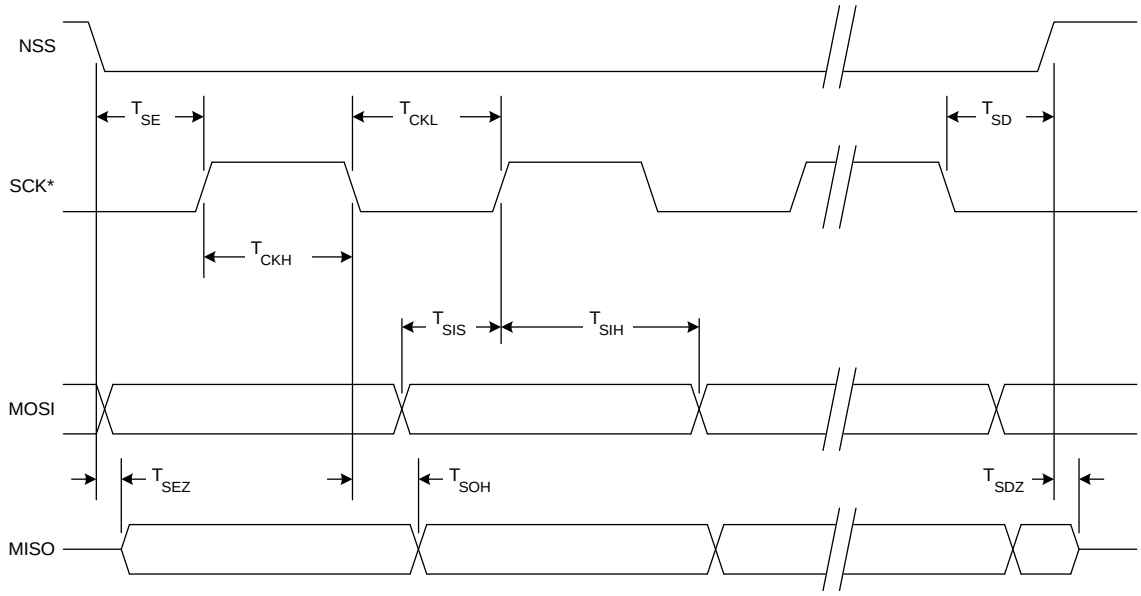
Bit 3: SLVSEL: Slave Selected Flag (read only).
This bit is set to logic 1 whenever the NSS pin is low indicating SPI0 is the selected slave. It is cleared to logic 0 when NSS is high (slave not selected). This bit does not indicate the instantaneous value at the NSS pin, but rather a de-glitched version of the pin input.

Bit 2: NSSIN: NSS Instantaneous Pin Input (read only).
This bit mimics the instantaneous value that is present on the NSS port pin at the time that the register is read. This input is not de-glitched.

Bit 1: SRMT: Shift Register Empty (Valid in Slave Mode, read only).
This bit will be set to logic 1 when all data has been transferred in/out of the shift register, and there is no new information available to read from the transmit buffer or write to the receive buffer. It returns to logic 0 when a data byte is transferred to the shift register from the transmit buffer or by a transition on SCK.
NOTE: SRMT = 1 when in Master Mode.

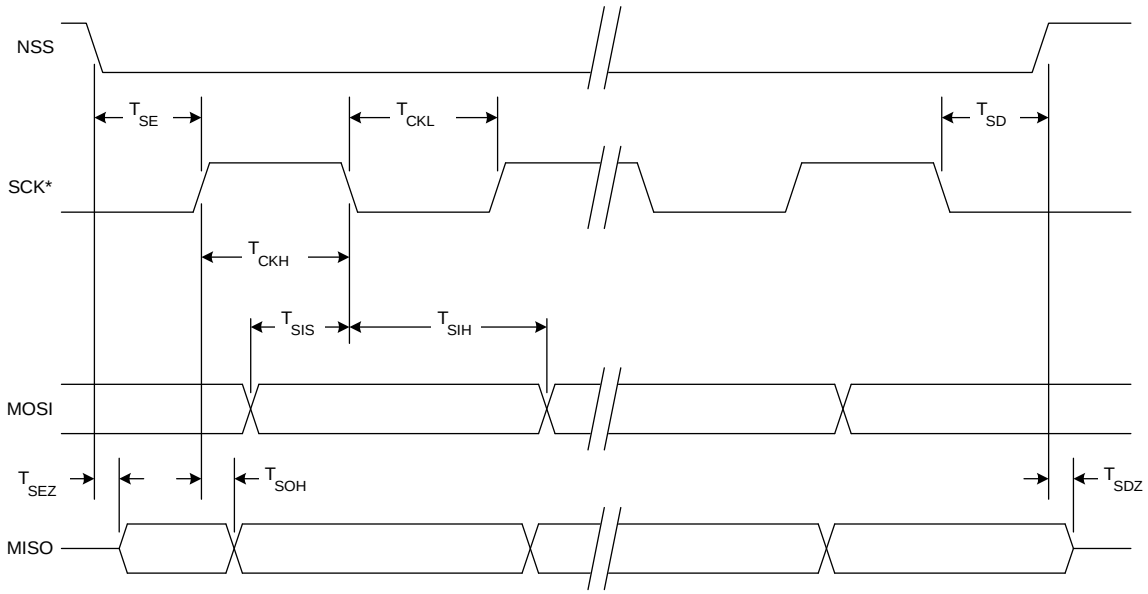
Bit 0: RXBMT: Receive Buffer Empty (Valid in Slave Mode, read only).
This bit will be set to logic 1 when the receive buffer has been read and contains no new information. If there is new information available in the receive buffer that has not been read, this bit will return to logic 0.
NOTE: RXBMT = 1 when in Master Mode.

***Note:** See Table 21.1 for timing parameters.



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 21.8. SPI Slave Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 21.9. SPI Slave Timing (CKPHA = 1)

23.2.5. 8-Bit Pulse Width Modulator Mode

Each module can be used independently to generate a pulse width modulated (PWM) output on its associated CEXn pin. The frequency of the output is dependent on the timebase for the PCA counter/timer. The duty cycle of the PWM output signal is varied using the module's PCA0CPLn capture/compare register. When the value in the low byte of the PCA counter/timer (PCA0L) is equal to the value in PCA0CPLn, the output on the CEXn pin will be set. When the count value in PCA0L overflows, the CEXn output will be reset (see Figure 23.8). Also, when the counter/timer low byte (PCA0L) overflows from 0xFF to 0x00, PCA0CPLn is reloaded automatically with the value stored in the module's capture/compare high byte (PCA0CPHn) without software intervention. Setting the ECOMn and PWMn bits in the PCA0CPMn register enables 8-Bit Pulse Width Modulator mode. The duty cycle for 8-Bit PWM Mode is given by Equation 23.2.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to '0'; writing to PCA0CPHn sets ECOMn to '1'.

$$DutyCycle = \frac{(256 - PCA0CPHn)}{256}$$

Equation 23.2. 8-Bit PWM Duty Cycle

Using Equation 23.2, the largest duty cycle is 100% (PCA0CPHn = 0), and the smallest duty cycle is 0.39% (PCA0CPHn = 0xFF). A 0% duty cycle may be generated by clearing the ECOMn bit to '0'.

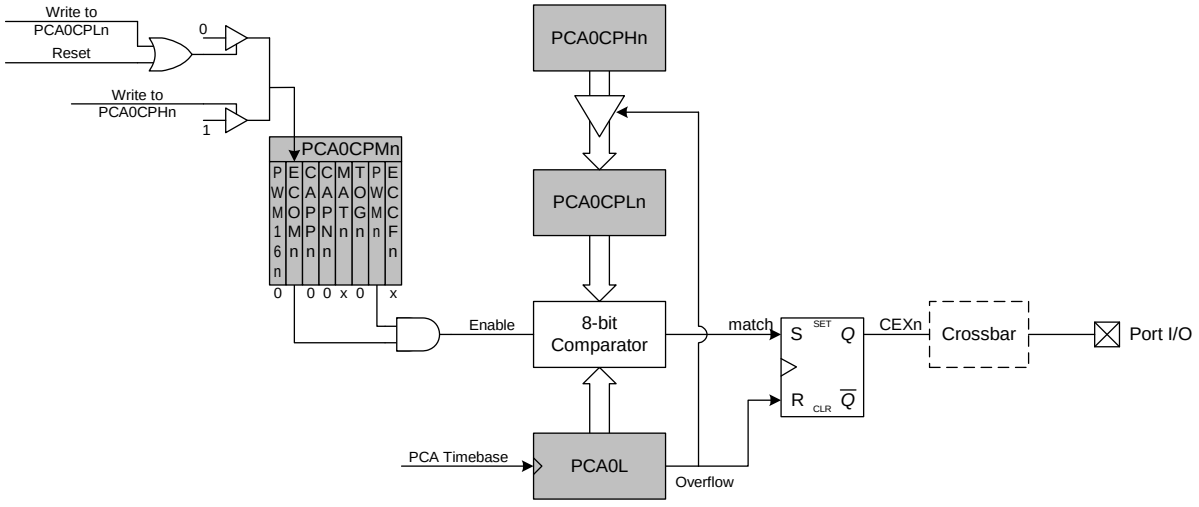


Figure 23.8. PCA 8-Bit PWM Mode Diagram

SFR Definition 23.4. PCA0L: PCA Counter/Timer Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xF9

Bits 7–0: PCA0L: PCA Counter/Timer Low Byte.
The PCA0L register holds the low byte (LSB) of the 16-bit PCA Counter/Timer.

SFR Definition 23.5. PCA0H: PCA Counter/Timer High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:

SFR Address: 0xFA

Bits 7–0: PCA0H: PCA Counter/Timer High Byte.
The PCA0H register holds the high byte (MSB) of the 16-bit PCA Counter/Timer.

C2 Register Definition 25.3. REVID: C2 Revision ID

Reset Value
Variable

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

This read-only register returns the 8-bit revision ID.

C2 Register Definition 25.4. FPCTL: C2 Flash Programming Control

Reset Value
00000000

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Bits7–0 FPCTL: Flash Programming Control Register.
This register is used to enable Flash programming via the C2 interface. To enable C2 Flash programming, the following codes must be written in order: 0x02, 0x01. Note that once C2 Flash programming is enabled, a system reset must be issued to resume normal operation.

C2 Register Definition 25.5. FPDAT: C2 Flash Programming Data

Reset Value
00000000

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Bits7–0: FPDAT: C2 Flash Programming Data Register.
This register is used to pass Flash commands, addresses, and data during C2 Flash accesses. Valid commands are listed below.

Code	Command
0x06	Flash Block Read
0x07	Flash Block Write
0x08	Flash Page Erase
0x03	Device Erase