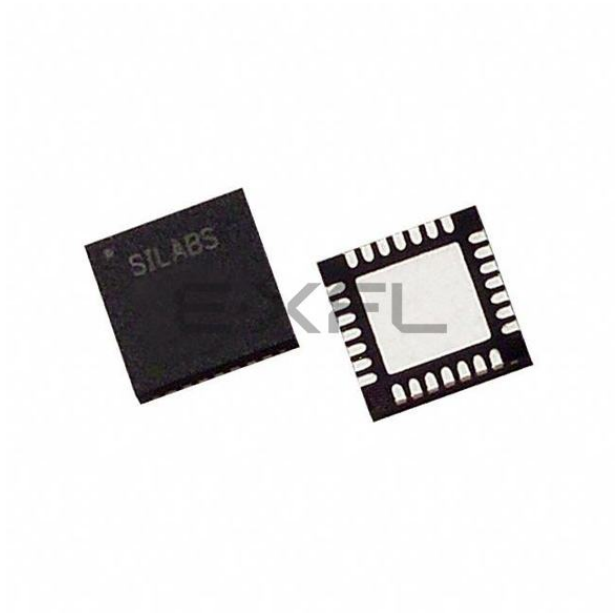

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x16b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VFQFN Exposed Pad
Supplier Device Package	28-MLP (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f353-gm

NOTES:

SFR Definition 22.14. TMR3RLL: Timer 3 Reload Register Low Byte 210
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SFR Definition 23.1. PCA0CN: PCA Control 222
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3. Global DC Electrical Characteristics

Table 3.1. Global DC Electrical Characteristics

–40 to +85 °C, 25 MHz System Clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Analog Supply Voltage[1]		2.7	3.0	3.6	V
Analog Supply Current	Internal REF, ADC, IDACs, Comparators all active	—	0.75	1.3	mA
Analog Supply Current with analog sub-systems inactive	Internal REF, ADC, IDACs, Comparators all disabled, oscillator disabled	—	< 1	—	µA
Analog-to-Digital Supply Delta ($\|V_{DD} – AV+\|$)		—	—	0.5	V
Digital Supply Voltage		2.7	3.0	3.6	V
Digital Supply Current with CPU active	V_{DD} = 2.7 V; SYSCLK = 25 MHz V_{DD} = 2.7 V; SYSCLK = 50 MHz V_{DD} = 3.3 V; SYSCLK = 25 MHz V_{DD} = 3.3 V; SYSCLK = 50 MHz	— — — —	9.9 17.8 13.6 24.9	11.3 20.0 15.5 27.1	mA mA mA mA
Digital Supply Current with CPU inactive (not accessing Flash)	V_{DD} = 2.7 V; SYSCLK = 25 MHz V_{DD} = 2.7 V; SYSCLK = 50 MHz V_{DD} = 3.3 V; SYSCLK = 25 MHz V_{DD} = 3.3 V; SYSCLK = 50 MHz	— — — —	5.7 11.1 7.5 15.0	6.6 12.7 8.5 16.5	mA mA mA mA
Digital Supply Current (shutdown)	Oscillator not running	—	< 0.1	—	µA
Digital Supply RAM Data Retention Voltage		—	1.5	—	V
SYSCLK (System Clock) [2,3]		0	—	50	MHz
Specified Operating Temperature Range		–40	—	+85	°C

Notes:

1. Analog Supply AV+ must be greater than 1 V for V_{DD} monitor to operate.
2. SYSCLK is the internal device clock. For operational speeds in excess of 25 MHz, SYSCLK must be derived from the internal clock multiplier.
3. SYSCLK must be at least 32 kHz to enable debugging.

SFR Definition 5.1. ADC0CN: ADC0 Control

R	R	R	R/W	R/W	R/W	R/W	R/W	Reset Value
—	—	—	AD0POL	AD0BCE	AD0GN			00010000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xF4

Bits 7–5: Unused: Read = 000b, Write = don't care.
Bit 4: AD0POL: ADC0 Polarity.
0: ADC operates in Unipolar mode (straight binary result).
1: ADC operates in Bipolar mode (2's compliment result).
Bit 3: AD0BCE: ADC0 Burnout Current Source Enable.
0: ADC Burnout current sources disabled.
1: ADC Burnout current sources enabled.
Bits 2:0 AD0GN: ADC0 Programmable Gain Setting.
000: PGA Gain = 1.
001: PGA Gain = 2.
010: PGA Gain = 4.
011: PGA Gain = 8.
100: PGA Gain = 16.
101: PGA Gain = 32.
110: PGA Gain = 64.
111: PGA Gain = 128.

This SFR can only be modified when ADC0 is in IDLE mode.

SFR Definition 5.19. ADC0FH: ADC0 Conversion Register (Fast Filter) High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ADC0FH								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xFE

Bits 7–0: ADC0FH: ADC0 Conversion Register (Fast Filter) High Byte.
C8051F350/1: This register contains bits 23–16 of the 24-bit ADC fast filter conversion result.
C8051F352/3: This register contains bits 15–8 of the 16-bit ADC fast filter conversion result.

SFR Definition 5.20. ADC0FM: ADC0 Conversion Register (Fast Filter) Middle Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ADC0FM								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xFD

Bits 7–0: ADC0FM: ADC0 Conversion Register (Fast Filter) Middle Byte.
C8051F350/1: This register contains bits 15–8 of the 24-bit ADC fast filter conversion result.
C8051F352/3: This register contains bits 7–0 of the 16-bit ADC fast filter conversion result.

SFR Definition 5.21. ADC0FL: ADC0 Conversion Register (Fast Filter) Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ADC0FL								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xFC

Bits 7–0: ADC0FL: ADC0 Conversion Register (Fast Filter) Low Byte.
C8051F350/1: This register contains bits 7–0 of the 24-bit ADC fast filter conversion result.
C8051F352/3: This register contains all zeros (00000000b).

Table 5.9. ADC0 Fast Filter Flicker-Free (Noise-Free) Resolution[1] in Unipolar Mode (bits)

Decimation Ratio	Output Word Rate[2]	PGA Gain Setting							
		1	2	4	8	16	32	64	128
1920	10 Hz	16.26	16.11	15.90	15.49	14.95	14.24	13.37	12.32
768	25 Hz	14.37	14.24	13.98	13.64	13.05	12.24	11.34	10.39
640	30 Hz	13.63	13.64	13.57	13.10	12.57	11.82	10.86	9.93
384	50 Hz	11.83	11.93	11.85	11.72	11.32	10.69	9.84	8.93
320	60 Hz	11.11	11.04	11.11	11.00	10.74	10.16	9.36	8.44
192	100 Hz	9.43	9.28	9.40	9.34	9.17	8.86	8.21	7.39

Notes:

1. *Flicker-free (Noise-free) Resolution* = $\log_2\left(\frac{FullInputRange(V)}{6.6 \times RMS\ Noise(V)}\right)$

where *Full Input Range* = $\frac{V_{REF}}{PGA\ Gain}$ in Unipolar mode and *RMS Noise* is obtained from Table 5.7.

2. Output Word Rate assuming Modular Clock frequency = 2.4576 MHz (sampling clock frequency = 19.2 kHz)

NOTES:

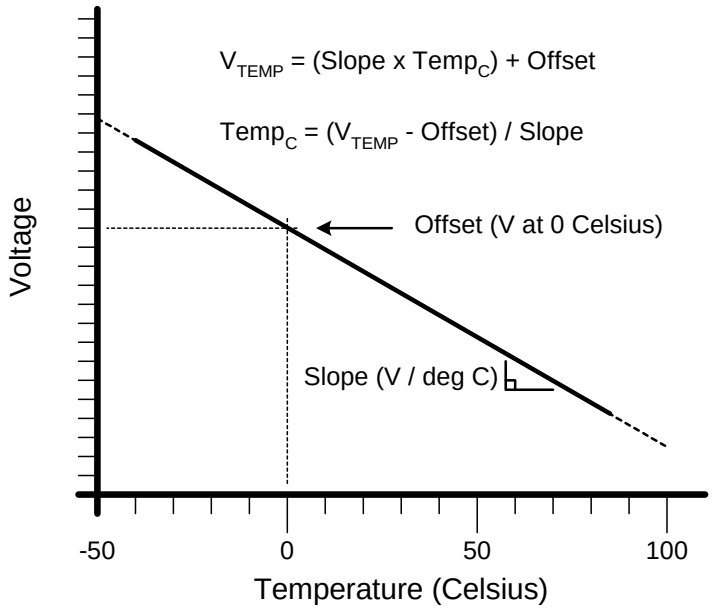

Figure 8.2. Single Channel Transfer Function

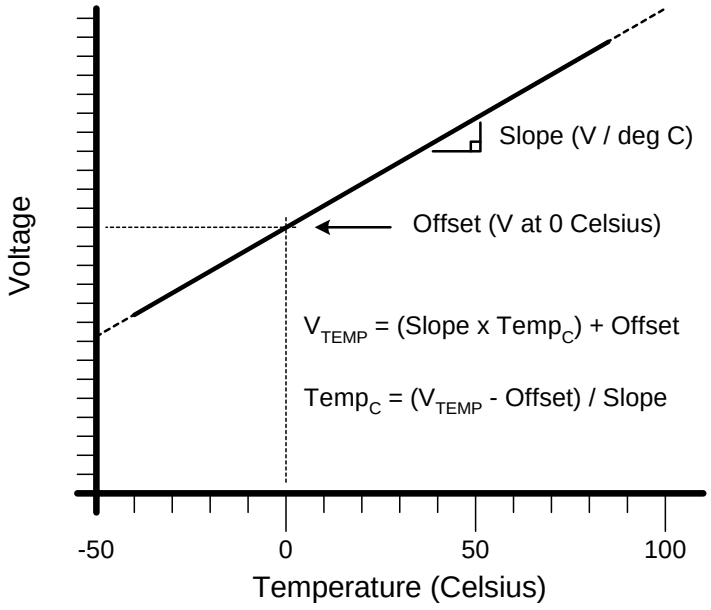

Figure 8.3. Differential Transfer Function

13. Prefetch Engine

The C8051F350/1/2/3 family of devices incorporate a 2-byte prefetch engine. Because the access time of the Flash memory is 40 ns, and the minimum instruction time is 20 ns, the prefetch engine is necessary for full-speed code execution. Instructions are read from Flash memory two bytes at a time by the prefetch engine, and given to the CIP-51 processor core to execute. When running linear code (code without any jumps or branches), the prefetch engine allows instructions to be executed at full speed. When a code branch occurs, the processor may be stalled for up to two clock cycles while the next set of code bytes is retrieved from Flash memory. The FLRT bit (FLSCL.4) determines how many clock cycles are used to read each set of two code bytes from Flash. When operating from a system clock of 25 MHz or less, the FLRT bit should be set to '0' so that the prefetch engine takes only one clock cycle for each read. When operating with a system clock of greater than 25 MHz (up to 50 MHz), the FLRT bit should be set to '1', so that each prefetch code read lasts for two clock cycles.

SFR Definition 13.1. PFE0CN: Prefetch Engine Control

R	R	R/W	R	R	R	R	R/W	Reset Value
		PFEN					FLBWE	00100000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xE3

Bits 7–6: Unused. Read = 00b; Write = Don't Care
Bit 5: PFEN: Prefetch Enable.
This bit enables the prefetch engine.
0: Prefetch engine is disabled.
1: Prefetch engine is enabled.
Bits 4–1: Unused. Read = 0000b; Write = Don't Care
Bit 0: FLBWE: Flash Block Write Enable.
This bit allows block writes to Flash memory from software.
0: Each byte of a software Flash write is written individually.
1: Flash bytes are written in groups of two.

SFR Definition 14.2. RSTSRC: Reset Source

R	R	R/W	R/W	R	R/W	R/W	R	Reset Value
—	FERROR	C0RSEF	SWRSF	WDTRSF	MCDRSF	PORSF	PINRSF	Variable
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xEF

Bit7: UNUSED. Read = 0. Write = don't care.

Bit6: FERROR: Flash Error Indicator.
0: Source of last reset was not a Flash read/write/erase error.
1: Source of last reset was a Flash read/write/erase error.

Bit5: C0RSEF: Comparator0 Reset Enable and Flag.
0: **Read:** Source of last reset was not Comparator0. **Write:** Comparator0 is not a reset source.
1: **Read:** Source of last reset was Comparator0. **Write:** Comparator0 is a reset source (active-low).

Bit4: SWRSF: Software Reset Force and Flag.
0: **Read:** Source of last reset was not a write to the SWRSF bit. **Write:** No Effect.
1: **Read:** Source of last was a write to the SWRSF bit. **Write:** Forces a system reset.

Bit3: WDTRSF: Watchdog Timer Reset Flag.
0: Source of last reset was not a WDT timeout.
1: Source of last reset was a WDT timeout.

Bit2: MCDRSF: Missing Clock Detector Flag.
0: **Read:** Source of last reset was not a Missing Clock Detector timeout. **Write:** Missing Clock Detector disabled.
1: **Read:** Source of last reset was a Missing Clock Detector timeout. **Write:** Missing Clock Detector enabled; triggers a reset if a missing clock condition is detected.

Bit1: PORSF: Power-On Reset Force and Flag.
This bit is set anytime a power-on reset occurs. Writing this bit enables/disables the V_{DD} monitor as a reset source. **Note: writing '1' to this bit before the V_{DD} monitor is enabled and stabilized may cause a system reset.** See register VDM0CN (SFR Definition 14.1)
0: **Read:** Last reset was not a power-on or V_{DD} monitor reset. **Write:** V_{DD} monitor is not a reset source.
1: **Read:** Last reset was a power-on or V_{DD} monitor reset; all other reset flags indeterminate. **Write:** V_{DD} monitor is a reset source.

Bit0: PINRSF: HW Pin Reset Flag.
0: Source of last reset was not /RST pin.
1: Source of last reset was /RST pin.

11.2. Data Memory

The C8051F350/1/2/3 includes 256 bytes of internal RAM mapped into the data memory space from 0x00 through 0xFF. The lower 128 bytes of data memory are used for general purpose registers and scratch pad memory. Either direct or indirect addressing may be used to access the lower 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode.

The upper 128 bytes of data memory are accessible only by indirect addressing. This region occupies the same address space as the Special Function Registers (SFRs) but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the CPU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory. Figure 11.1 illustrates the data memory organization of the C8051F350/1/2/3.

The C8051F35x family also includes 512 bytes of on-chip RAM mapped into the external memory (XDATA) space. This RAM can be accessed using the CIP-51 core's MOVX instruction. More information on the XRAM memory can be found in Section "16. External RAM' on page 127.

11.3. General Purpose Registers

The lower 32 bytes of data memory (locations 0x00 through 0x1F) may be addressed as four banks of general-purpose registers. Each bank consists of eight byte-wide registers designated R0 through R7. Only one of these banks may be enabled at a time. Two bits in the program status word, RS0 (PSW.3) and RS1 (PSW.4), select the active register bank (see description of the PSW in SFR Definition 10.4). This allows fast context switching when entering subroutines and interrupt service routines. Indirect addressing modes use registers R0 and R1 as index registers.

11.4. Bit Addressable Locations

In addition to direct access to data memory organized as bytes, the sixteen data memory locations at 0x20 through 0x2F are also accessible as 128 individually addressable bits. Each bit has a bit address from 0x00 to 0x7F. Bit 0 of the byte at 0x20 has bit address 0x00 while bit 7 of the byte at 0x20 has bit address 0x07. Bit 7 of the byte at 0x2F has bit address 0x7F. A bit access is distinguished from a full byte access by the type of instruction used (bit source or destination operands as opposed to a byte source or destination).

The MCS-51™ assembly language allows an alternate notation for bit addressing of the form XX.B where XX is the byte address and B is the bit position within the byte. For example, the instruction:

```
MOV    C, 22.3h
```

moves the Boolean value at 0x13 (bit 3 of the byte at location 0x22) into the Carry flag.

11.5. Stack

A programmer's stack can be located anywhere in the 256-byte data memory. The stack area is designated using the Stack Pointer (SP, 0x81) SFR. The SP will point to the last location used. The next value pushed on the stack is placed at SP+1 and then SP is incremented. A reset initializes the stack pointer to location 0x07. Therefore, the first value pushed on the stack is placed at location 0x08, which is also the first register (R0) of register bank 1. Thus, if more than one register bank is to be used, the SP should be initialized to a location in the data memory not being used for data storage. The stack depth can extend up to 256 bytes.

The capacitors shown in the external crystal configuration provide the load capacitance required by the crystal for correct oscillation. These capacitors are “in series” as seen by the crystal and “in parallel” with the stray capacitance of the XTAL1 and XTAL2 pins.

Note: The load capacitance depends upon the crystal and the manufacturer. Please refer to the crystal datasheet when completing these calculations.

For example, a tuning-fork crystal of 32.768 kHz with a recommended load capacitance of 12.5 pF should use the configuration shown in Figure 17.1, Option 1. The total value of the capacitors and the stray capacitance of the XTAL pins should equal 25 pF. With a stray capacitance of 3 pF per pin, the 22 pF capacitors yield an equivalent capacitance of 12.5 pF across the crystal, as shown in Figure 17.2.

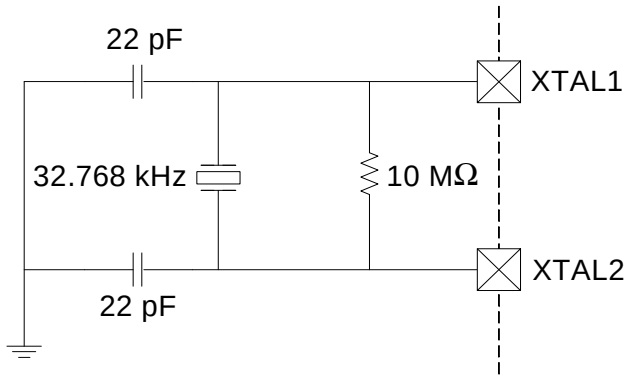

Figure 17.2. 32.768 kHz External Crystal Example

Important note on external crystals: Crystal oscillator circuits are quite sensitive to PCB layout. The crystal should be placed as close as possible to the XTAL pins on the device. The traces should be as short as possible and shielded with ground plane from any other traces which could introduce noise or interference.

SFR Definition 18.1. XBR0: Port I/O Crossbar Register 0

R	R	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
—	—	CP0AE	CP0E	SYSCKE	SMB0E	SPI0E	URT0E	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xE1

Bits7–6: UNUSED. Read = 00b, Write = don't care.
Bit5: CP0AE: Comparator0 Asynchronous Output Enable
0: Asynchronous CP0 unavailable at Port pin.
1: Asynchronous CP0 routed to Port pin P1.4.
Bit4: CP0E: Comparator0 Output Enable
0: CP0 unavailable at Port pin.
1: CP0 routed to Port pin P1.5.
Bit3: SYSCKE: /SYSCLK Output Enable
0: /SYSCLK unavailable at Port pin.
1: /SYSCLK output routed to Port pin.
Bit2: SMB0E: SMBus I/O Enable
0: SMBus I/O unavailable at Port pins.
1: SMBus I/O routed to Port pins.
Bit1: SPI0E: SPI I/O Enable
0: SPI I/O unavailable at Port pins.
1: SPI I/O routed to Port pins. Note that the SPI can be assigned either 3 or 4 GPIO pins.
Bit0: URT0E: UART I/O Output Enable
0: UART I/O unavailable at Port pin.
1: UART TX0, RX0 routed to Port pins P0.4 and P0.5.

19.4. Using the SMBus

The SMBus can operate in both Master and Slave modes. The interface provides timing and shifting control for serial transfers; higher level protocol is determined by user software. The SMBus interface provides the following application-independent features:

- Byte-wise serial data transfers
- Clock signal generation on SCL (Master Mode only) and SDA data synchronization
- Timeout/bus error recognition, as defined by the SMB0CF configuration register
- START/STOP timing, detection, and generation
- Bus arbitration
- Interrupt generation
- Status information

SMBus interrupts are generated for each data byte or slave address that is transferred. When transmitting, this interrupt is generated after the ACK cycle so that software may read the received ACK value; when receiving data, this interrupt is generated before the ACK cycle so that software may define the outgoing ACK value. See Section “19.5. SMBus Transfer Modes’ on page 163 for more details on transmission sequences.

Interrupts are also generated to indicate the beginning of a transfer when a master (START generated), or the end of a transfer when a slave (STOP detected). Software should read the SMB0CN (SMBus Control register) to find the cause of the SMBus interrupt. The SMB0CN register is described in Section “19.4.2. SMB0CN Control Register’ on page 159; Table 19.4 provides a quick SMB0CN decoding reference.

SMBus configuration options include:

- Timeout detection (SCL Low Timeout and/or Bus Free Timeout)
- SDA setup and hold time extensions
- Slave event enable/disable
- Clock source selection

These options are selected in the SMB0CF register, as described in Section “19.4.1. SMBus Configuration Register’ on page 156.

Figure 19.4 shows the typical SCL generation described by Equation 19.2. Notice that T_{HIGH} is typically twice as large as T_{LOW}. The actual SCL output may vary due to other devices on the bus (SCL may be extended low by slower slave devices, or driven low by contending master devices). The bit rate when operating as a master will never exceed the limits defined by equation Equation 19.1.

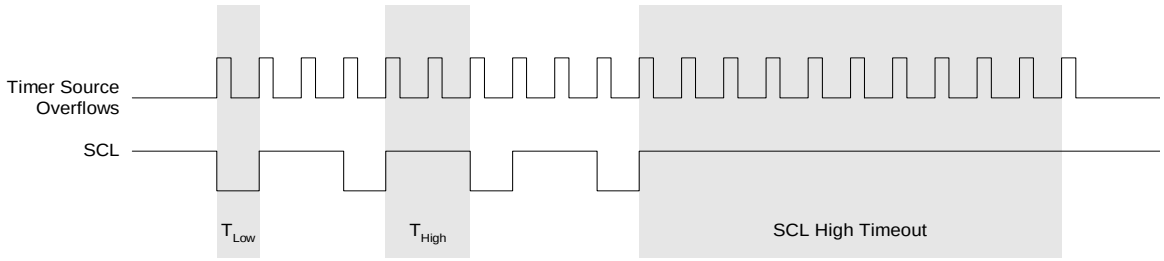

Figure 19.4. Typical SMBus SCL Generation

Setting the EXTHOLD bit extends the minimum setup and hold times for the SDA line. The minimum SDA setup time defines the absolute minimum time that SDA is stable before SCL transitions from low-to-high. The minimum SDA hold time defines the absolute minimum time that the current SDA value remains stable after SCL transitions from high-to-low. EXTHOLD should be set so that the minimum setup and hold times meet the SMBus Specification requirements of 250 ns and 300 ns, respectively. Table 19.2 shows the minimum setup and hold times for the two EXTHOLD settings. Setup and hold time extensions are typically necessary when SYSCLK is above 10 MHz.

Table 19.2. Minimum SDA Setup and Hold Times

EXTHOLD	Minimum SDA Setup Time	Minimum SDA Hold Time
0	T_{low} – 4 system clocks OR 1 system clock + s/w delay*	3 system clocks
1	11 system clocks	12 system clocks

***Note:** Setup Time for ACK bit transmissions and the MSB of all data transfers. The s/w delay occurs between the time SMB0DAT or ACK is written and when SI is cleared. Note that if SI is cleared in the same write that defines the outgoing ACK value, s/w delay is zero.

With the SMBTOE bit set, Timer 3 should be configured to overflow after 25 ms in order to detect SCL low timeouts (see Section “19.3.3. SCL Low Timeout’ on page 154). The SMBus interface will force Timer 3 to reload while SCL is high, and allow Timer 3 to count when SCL is low. The Timer 3 interrupt service routine should be used to reset SMBus communication by disabling and re-enabling the SMBus.

SMBus Free Timeout detection can be enabled by setting the SMBFTE bit. When this bit is set, the bus will be considered free if SDA and SCL remain high for more than 10 SMBus clock source periods (see Figure 19.4). When a Free Timeout is detected, the interface will respond as if a STOP was detected (an interrupt will be generated, and STO will be set).

Table 20.1. Timer Settings for Standard Baud Rates Using the Internal Oscillator

	Frequency: 24.5 MHz						
	Target Baud Rate (bps)	Baud Rate % Error	Oscillator Divide Factor	Timer Clock Source	SCA1–SCA0 (pre-scale select)*	T1M*	Timer 1 Reload Value (hex)
SYSCLK from Internal Osc.	230400	–0.32%	106	SYSCLK	XX	1	0xCB
	115200	–0.32%	212	SYSCLK	XX	1	0x96
	57600	0.15%	426	SYSCLK	XX	1	0x2B
	28800	–0.32%	848	SYSCLK / 4	01	0	0x96
	14400	0.15%	1704	SYSCLK / 12	00	0	0xB9
	9600	–0.32%	2544	SYSCLK / 12	00	0	0x96
	2400	–0.32%	10176	SYSCLK / 48	10	0	0x96
	1200	0.15%	20448	SYSCLK / 48	10	0	0x2B

X = Don't care

***Note:** SCA1–SCA0 and T1M bit definitions can be found in Section 22.1.

Table 20.2. Timer Settings for Standard Baud Rates Using an External 25.0 MHz Oscillator

	Frequency: 25.0 MHz						
	Target Baud Rate (bps)	Baud Rate % Error	Oscillator Divide Factor	Timer Clock Source	SCA1–SCA0 (pre-scale select)*	T1M*	Timer 1 Reload Value (hex)
SYSCLK from External Osc.	230400	–0.47%	108	SYSCLK	XX	1	0xCA
	115200	0.45%	218	SYSCLK	XX	1	0x93
	57600	–0.01%	434	SYSCLK	XX	1	0x27
	28800	0.45%	872	SYSCLK / 4	01	0	0x93
	14400	–0.01%	1736	SYSCLK / 4	01	0	0x27
	9600	0.15%	2608	EXTCLK / 8	11	0	0x5D
	2400	0.45%	10464	SYSCLK / 48	10	0	0x93
	1200	–0.01%	20832	SYSCLK / 48	10	0	0x27
SYSCLK from Internal Osc.	57600	–0.47%	432	EXTCLK / 8	11	0	0xE5
	28800	–0.47%	864	EXTCLK / 8	11	0	0xCA
	14400	0.45%	1744	EXTCLK / 8	11	0	0x93
	9600	0.15%	2608	EXTCLK / 8	11	0	0x5D

X = Don't care

***Note:** SCA1–SCA0 and T1M bit definitions can be found in Section 22.1.

21.5. Serial Clock Timing

Four combinations of serial clock phase and polarity can be selected using the clock control bits in the SPI0 Configuration Register (SPI0CFG). The CKPHA bit (SPI0CFG.5) selects one of two clock phases (edge used to latch the data). The CKPOL bit (SPI0CFG.4) selects between an active-high or active-low clock. Both master and slave devices must be configured to use the same clock phase and polarity. SPI0 should be disabled (by clearing the SPIEN bit, SPI0CN.0) when changing the clock phase or polarity. The clock and data line relationships are shown in Figure 21.5.

The SPI0 Clock Rate Register (SPI0CKR) as shown in SFR Definition 21.3 controls the master mode serial clock frequency. This register is ignored when operating in slave mode. When the SPI is configured as a master, the maximum data transfer rate (bits/sec) is one-half the system clock frequency or 12.5 MHz, whichever is slower. When the SPI is configured as a slave, the maximum data transfer rate (bits/sec) for full-duplex operation is 1/10 the system clock frequency, provided that the master issues SCK, NSS (in 4-wire slave mode), and the serial input data synchronously with the slave's system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less than 1/10 the system clock frequency. In the special case where the master only wants to transmit data to the slave and does not need to receive data from the slave (i.e. half-duplex operation), the SPI slave can receive data at a maximum data transfer rate (bits/sec) of 1/4 the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the slave's system clock.

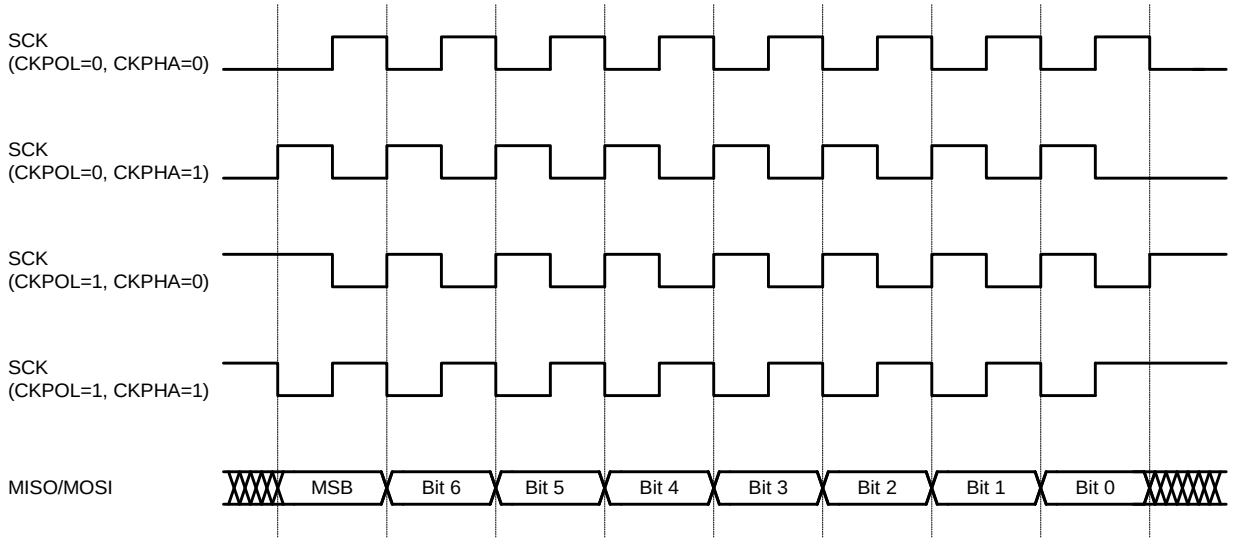

Figure 21.5. Data/Clock Timing Relationship

21.6. SPI Special Function Registers

SPI0 is accessed and controlled through four special function registers in the system controller: SPI0CN Control Register, SPI0DAT Data Register, SPI0CFG Configuration Register, and SPI0CKR Clock Rate Register. The four special function registers related to the operation of the SPI0 Bus are described in the following figures.

SFR Definition 21.1. SPI0CFG: SPI0 Configuration

R	R/W	R/W	R/W	R	R	R	R	Reset Value
SPIBSY	MSTEN	CKPHA	CKPOL	SLVSEL	NSSIN	SRMT	RXBMT	00000111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA1

Bit 7: SPIBSY: SPI Busy (read only).
This bit is set to logic 1 when a SPI transfer is in progress (Master or Slave Mode).

Bit 6: MSTEN: Master Mode Enable.
0: Disable master mode. Operate in slave mode.
1: Enable master mode. Operate as a master.

Bit 5: CKPHA: SPI0 Clock Phase.
This bit controls the SPI0 clock phase.
0: Data centered on first edge of SCK period.*
1: Data centered on second edge of SCK period.*

Bit 4: CKPOL: SPI0 Clock Polarity.
This bit controls the SPI0 clock polarity.
0: SCK line low in idle state.
1: SCK line high in idle state.

Bit 3: SLVSEL: Slave Selected Flag (read only).
This bit is set to logic 1 whenever the NSS pin is low indicating SPI0 is the selected slave. It is cleared to logic 0 when NSS is high (slave not selected). This bit does not indicate the instantaneous value at the NSS pin, but rather a de-glitched version of the pin input.

Bit 2: NSSIN: NSS Instantaneous Pin Input (read only).
This bit mimics the instantaneous value that is present on the NSS port pin at the time that the register is read. This input is not de-glitched.

Bit 1: SRMT: Shift Register Empty (Valid in Slave Mode, read only).
This bit will be set to logic 1 when all data has been transferred in/out of the shift register, and there is no new information available to read from the transmit buffer or write to the receive buffer. It returns to logic 0 when a data byte is transferred to the shift register from the transmit buffer or by a transition on SCK.
NOTE: SRMT = 1 when in Master Mode.

Bit 0: RXBMT: Receive Buffer Empty (Valid in Slave Mode, read only).
This bit will be set to logic 1 when the receive buffer has been read and contains no new information. If there is new information available in the receive buffer that has not been read, this bit will return to logic 0.
NOTE: RXBMT = 1 when in Master Mode.

***Note:** See Table 21.1 for timing parameters.

SFR Definition 22.8. TMR2CN: Timer 2 Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF2H	TF2L	TF2LEN	—	T2SPLIT	TR2	—	T2XCLK	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xC8

Bit7: TF2H: Timer 2 High Byte Overflow Flag.
Set by hardware when the Timer 2 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 2 overflows from 0xFFFF to 0x0000. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 2 interrupt service routine. TF2H is not automatically cleared by hardware and must be cleared by software.

Bit6: TF2L: Timer 2 Low Byte Overflow Flag.
Set by hardware when the Timer 2 low byte overflows from 0xFF to 0x00. When this bit is set, an interrupt will be generated if TF2LEN is set and Timer 2 interrupts are enabled. TF2L will set when the low byte overflows regardless of the Timer 2 mode. This bit is not automatically cleared by hardware.

Bit5: TF2LEN: Timer 2 Low Byte Interrupt Enable.
This bit enables/disables Timer 2 Low Byte interrupts. If TF2LEN is set and Timer 2 interrupts are enabled, an interrupt will be generated when the low byte of Timer 2 overflows. This bit should be cleared when operating Timer 2 in 16-bit mode.
0: Timer 2 Low Byte interrupts disabled.
1: Timer 2 Low Byte interrupts enabled.

Bit4: UNUSED. Read = 0b. Write = don't care.

Bit3: T2SPLIT: Timer 2 Split Mode Enable.
When this bit is set, Timer 2 operates as two 8-bit timers with auto-reload.
0: Timer 2 operates in 16-bit auto-reload mode.
1: Timer 2 operates as two 8-bit auto-reload timers.

Bit2: TR2: Timer 2 Run Control.
This bit enables/disables Timer 2. In 8-bit mode, this bit enables/disables TMR2H only; TMR2L is always enabled in this mode.
0: Timer 2 disabled.
1: Timer 2 enabled.

Bit1: UNUSED. Read = 0b. Write = don't care.

Bit0: T2XCLK: Timer 2 External Clock Select.
This bit selects the external clock source for Timer 2. If Timer 2 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 2 Clock Select bits (T2MH and T2ML in register CKCON) may still be used to select between the external clock and the system clock for either timer.
0: Timer 2 external clock selection is the system clock divided by 12.
1: Timer 2 external clock selection is the external clock divided by 8. Note that the external oscillator source divided by 8 is synchronized with the system clock.

24. Revision Specific Behavior

This chapter describes a functional difference between C8051F35x “REV B” and “REV C” or later devices. The functionality of the VREF- pin differs between these revisions.

24.1. Revision Identification

The Lot ID Code on the top side of the device package can be used for decoding device revision information. On C8051F350/2 devices, the revision letter is the first letter of the Lot ID Code. On C8051F351/3 devices, the revision letter is the first of the Lot ID Code. Figure 24.1 shows how to find the revision on the top side of the device package.

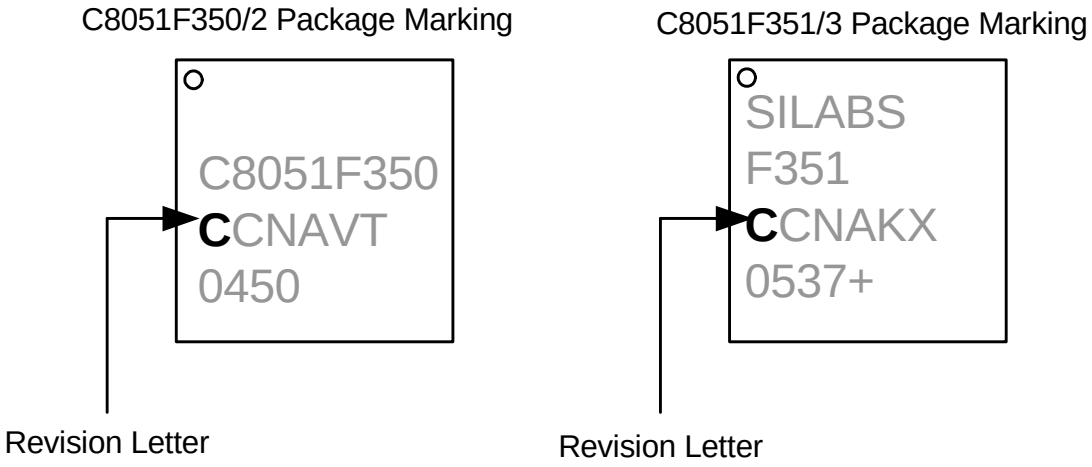

Figure 24.1. Reading Package Marking

24.1. VREF- pin

The required connection for the VREF- pin differs between the "REV B" and "REV C" and later devices. On "REV B" devices, when the internal voltage reference is enabled, the VREF- pin is internally connected to GND so the VREF- pin can be left unconnected externally.

On "REV C" and later devices, when the internal voltage reference is enabled, the VREF- pin is not internally connected to GND. The VREF- pin must be connected to GND externally for the voltage reference to operate properly.