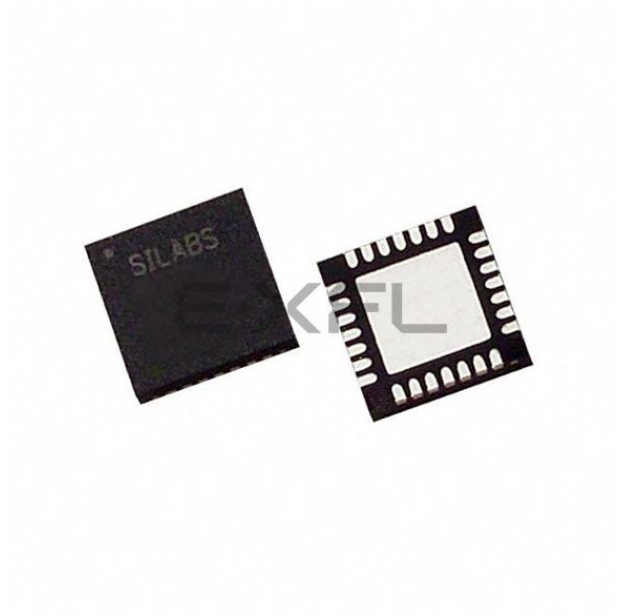

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x16b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VFQFN Exposed Pad
Supplier Device Package	28-MLP (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f353-gmr

1. System Overview

C8051F350/1/2/3 devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 1.1 for specific product feature selection.

- High-speed pipelined 8051-compatible microcontroller core (up to 50 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- 24 or 16-bit single-ended/differential ADC with analog multiplexer
- Two 8-bit Current Output DACs
- Precision programmable 24.5 MHz internal oscillator
- 8 kB of on-chip Flash memory
- 768 bytes of on-chip RAM
- SMBus/I2C, Enhanced UART, and SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable counter/timer array (PCA) with three capture/compare modules and watchdog timer function
- On-chip power-on reset, V_{DD} monitor, and temperature sensor
- On-chip voltage comparator
- 17 Port I/O (5 V tolerant)

With on-chip power-on reset, V_{DD} monitor, watchdog timer, and clock oscillator, the C8051F350/1/2/3 devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 2.7 to 3.6 V operation over the industrial temperature range (–45 to +85 °C). The Port I/O and /RST pins are tolerant of input signals up to 5 V. The C8051F350/1/2/3 are available in 28-pin QFN (also referred to as MLP or MLF) or 32-pin LQFP packaging, as shown in Figure 1.1 through Figure 1.4.

2. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Ambient temperature under bias	–55	—	125	°C
Storage Temperature	–65	—	150	°C
Voltage on AIN0.0–AIN0.7, VREF+, and VREF– with respect to DGND	–0.3	—	V_{DD} + 0.3	V
Voltage on any Port 0, 1, or 2 Pin or /RST with respect to DGND	–0.3	—	5.8	V
Voltage on V_{DD} with respect to DGND	–0.3	—	4.2	V
Voltage on AV+ with respect to AGND	–0.3	—	4.2	V
Maximum output current sunk by any Port 0, 1, or 2 pin	—	—	100	mA
Maximum output current sunk by any other I/O pin	—	—	50	mA
Maximum output current sourced by any Port 0, 1, or 2 pin	—	—	100	mA
Maximum output current sourced by any other I/O pin	—	—	50	mA
Maximum Total current through V_{DD}, AV+, DGND, and AGND	—	—	500	mA

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4.1. Pin Definitions for the C8051F350/1/2/3 (Continued)

Name	Pin Numbers		Type	Description
	'F350 'F352	'F351 'F353		
P0.6/	19	15	D I/O or A In	Port 0.6. See Port I/O Section for a complete description.
CNVSTR			D In	External Convert Start Input for IDACs (See IDAC Section for complete description).
P0.7	20	16	D I/O or A In	Port 0.7. See Port I/O Section for a complete description.
P1.0/	23	19	D I/O or A In	Port 1.0. See Port I/O Section for a complete description.
AIN0.4			A In	ADC0 Input Channel 4 (C8051F351/3 - See ADC0 Section for complete description).
P1.1/	24	20	D I/O or A In	Port 1.1. See Port I/O Section for a complete description.
AIN0.5			A In	ADC0 Input Channel 5 (C8051F351/3 - See ADC0 Section for complete description).
P1.2/	25	21	D I/O or A In	Port 1.2. See Port I/O Section for a complete description.
AIN0.6			A In	ADC0 Input Channel 6 (C8051F351/3 - See ADC0 Section for complete description).
P1.3/	26	22	D I/O or A In	Port 1.3. See Port I/O Section for a complete description.
AIN0.7			A In	ADC0 Input Channel 7 (C8051F351/3 - See ADC0 Section for complete description).
P1.4	27	23	D I/O or A In	Port 1.4. See Port I/O Section for a complete description.
P1.5	28	24	D I/O or A In	Port 1.5. See Port I/O Section for a complete description.
P1.6/	29	25	D I/O or A In	Port 1.6. See Port I/O Section for a complete description.
IDA0			A Out	IDAC0 Output (See IDAC Section for complete description).
P1.7/	30	26	D I/O or A In	Port 1.7. See Port I/O Section for a complete description.
IDA1			A Out	IDAC1 Output (See IDAC Section for complete description).

Table 5.1. ADC0 Unipolar Output Word Coding (AD0POL = 0)

Input Voltage* (AIN+ – AIN–)	24-bit Output Word (C8051F350/1)	16-bit Output Word (C8051F352/3)
VREF – 1 LSB	0xFFFFFF	0xFFFF
VREF / 2	0x800000	0x8000
+1 LSB	0x000001	0x0001
0	0x000000	0x0000
***Note:** Input Voltage is voltage at ADC inputs after amplification by the PGA.		

Table 5.2. ADC0 Bipolar Output Word Coding (AD0POL = 1)

Input Voltage* (AIN+ – AIN–)	24-bit Output Word (C8051F350/1)	16-bit Output Word (C8051F352/3)
VREF – 1 LSB	0x7FFFFF	0x7FFF
VREF / 2	0x400000	0x4000
+1 LSB	0x000001	0x0001
0	0x000000	0x0000
–1 LSB	0xFFFFFF	0xFFFF
–VREF / 2	0xC00000	0xC000
–VREF	0x800000	0x8000
***Note:** Input Voltage is voltage at ADC inputs after amplification by the PGA.		

5.3.1. Error Conditions

Any errors during a conversion or calibration are indicated using bits in the ADC0STA register. The AD0S3C flag will be set to ‘1’ if there is a SINC3 filter clip during the conversion. Likewise, the AD0FFC flag will be set to ‘1’ if there is a Fast filter clip during the conversion. A filter clip occurs whenever an internal filter register overflows during a conversion. The AD0OVR flag will be set to ‘1’ if an ADC overrun condition occurs. An overrun occurs if the end of a conversion is reached while the AD0INT flag is still set to ‘1’ from the previous conversion. If the data registers have not been read, the new data values will be updated, and the previous conversion will be lost. The general AD0ERR flag indicates that an AD0S3C, AD0FFC, or AD0OVR error condition has occurred, or that a calibration resulted in a value that was beyond the limits of the offset or gain register. The data output registers are updated at the end of every conversion regardless of whether or not an error occurs.

5.4. Offset DAC

An 8-bit offset DAC is included, which can be used for offset correction up to approximately ±1/2 of the ADC’s input range on any PGA gain setting. The ADC0DAC register (SFR Definition 5.7) controls the offset DAC voltage. The register is decoded as a signed binary word. The MSB (bit 7) determines the sign of the DAC magnitude (0 = positive, 1 = negative), and the remaining seven bits (bits 6–0) determine the magnitude. Each LSB of the offset DAC is equivalent to approximately 0.4% of the ADC’s input span. A write to the ADC0DAC register initiates a change on the offset DAC output.

5.5. Burnout Current Sources

The burnout current sources can be used to detect an open circuit or short circuit at the ADC inputs. The burnout current sources are enabled by setting the AD0BCE bit in register ADC0CN to ‘1’ (SFR Definition 5.1). The positive-channel burnout current source sources approximately 2 µA on AIN+, and the negative-channel burnout current sinks approximately 2 µA on AIN–. If an open circuit exists between AIN+ and AIN– when the burnout current sources are enabled, the ADC will read a full scale positive value. If a short-circuit exists between AIN+ and AIN– when the burnout current sources are enabled, the ADC will read a value near zero. The burnout current sources should be disabled during normal ADC measurements.

SFR Definition 5.2. ADC0CF: ADC0 Configuration

R	R	R	R/W	R	R/W	R	R	Reset Value
—	—	—	AD0ISEL	—	AD0VREF	—	—	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xFB

Bits 7–5: Unused: Read = 000b, Write = don't care.
Bit 4: AD0ISEL: ADC0 Interrupt Source Select.
This bit selects which filter completion will set the AD0INT interrupt flag.
0: SINC3 filter.
1: FAST filter.
Bit 3: Unused: Read = 0b, Write = don't care.
Bit 2: AD0VREF: ADC0 VREF Source Select.
0: ADC0 uses the internal VREF (2.5 V). Setting this bit to '0' enables the internal Voltage Reference.
1: ADC0 uses an external VREF.
Bits 1–0: Unused: Read = 00b, Write = don't care.

This SFR can only be modified when ADC0 is in IDLE mode.

SFR Definition 5.4. ADC0CLK: ADC0 Modulator Clock Divisor

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ADC0CLK								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xF7

Bits 7–0: ADC0CLK: ADC0 Modulator Clock Divisor.
This register establishes the Modulator Clock (MDCLK), by dividing down the system clock (SYSCLK). The input signal is sampled by the modulator at a frequency of MDCLK / 128. For optimal performance, the divider should be chosen such that the modulator clock is equal to 2.4576 MHz (modulator sampling rate = 19.2 kHz).

The system clock is divided according to the equation:

MDCLK = SYSCLK / (ADC0CLK + 1)

Note: The Modulator Sampling Rate is not the ADC Output Word Rate. See Section 5.1.4 for details.

SFR Definition 5.5. ADC0DECH: ADC0 Decimation Ratio Register High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
—	—	—	—	—	DECI10	DECI9	DECI8	00000111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x9B

Bits 7–3: Unused: Read = 00000b, Write = don't care.
Bits 2–0: DECI[10:8]: ADC0 Decimation Ratio Register, Bits 10–8.
This register contains the high bits of the 11-bit ADC Decimation Ratio. The decimation ratio determines the output word rate of ADC0, based on the Modulator Clock (MDCLK). See the ADC0DECL register description for more information.

This SFR can only be modified when ADC0 is in IDLE mode.

10.2. Register Descriptions

Following are descriptions of SFRs related to the operation of the CIP-51 System Controller. Reserved bits should not be set to logic l. Future product versions may use these bits to implement new features in which case the reset value of the bit will be logic 0, selecting the feature's default state. Detailed descriptions of the remaining SFRs are included in the sections of the datasheet associated with their corresponding system function.

SFR Definition 10.1. SP: Stack Pointer

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x81

Bits7–0: SP: Stack Pointer.
The Stack Pointer holds the location of the top of the stack. The stack pointer is incremented before every PUSH operation. The SP register defaults to 0x07 after reset.

SFR Definition 10.2. DPL: Data Pointer Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x82

Bits7–0: DPL: Data Pointer Low.
The DPL register is the low byte of the 16-bit DPTR. DPTR is used to access indirectly addressed XRAM and Flash memory.

SFR Definition 10.3. DPH: Data Pointer High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x83

Bits7–0: DPH: Data Pointer High.
The DPH register is the high byte of the 16-bit DPTR. DPTR is used to access indirectly addressed XRAM and Flash memory.

11.2. Data Memory

The C8051F350/1/2/3 includes 256 bytes of internal RAM mapped into the data memory space from 0x00 through 0xFF. The lower 128 bytes of data memory are used for general purpose registers and scratch pad memory. Either direct or indirect addressing may be used to access the lower 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode.

The upper 128 bytes of data memory are accessible only by indirect addressing. This region occupies the same address space as the Special Function Registers (SFRs) but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the CPU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory. Figure 11.1 illustrates the data memory organization of the C8051F350/1/2/3.

The C8051F35x family also includes 512 bytes of on-chip RAM mapped into the external memory (XDATA) space. This RAM can be accessed using the CIP-51 core's MOVX instruction. More information on the XRAM memory can be found in Section "16. External RAM' on page 127.

11.3. General Purpose Registers

The lower 32 bytes of data memory (locations 0x00 through 0x1F) may be addressed as four banks of general-purpose registers. Each bank consists of eight byte-wide registers designated R0 through R7. Only one of these banks may be enabled at a time. Two bits in the program status word, RS0 (PSW.3) and RS1 (PSW.4), select the active register bank (see description of the PSW in SFR Definition 10.4). This allows fast context switching when entering subroutines and interrupt service routines. Indirect addressing modes use registers R0 and R1 as index registers.

11.4. Bit Addressable Locations

In addition to direct access to data memory organized as bytes, the sixteen data memory locations at 0x20 through 0x2F are also accessible as 128 individually addressable bits. Each bit has a bit address from 0x00 to 0x7F. Bit 0 of the byte at 0x20 has bit address 0x00 while bit 7 of the byte at 0x20 has bit address 0x07. Bit 7 of the byte at 0x2F has bit address 0x7F. A bit access is distinguished from a full byte access by the type of instruction used (bit source or destination operands as opposed to a byte source or destination).

The MCS-51™ assembly language allows an alternate notation for bit addressing of the form XX.B where XX is the byte address and B is the bit position within the byte. For example, the instruction:

```
MOV    C, 22.3h
```

moves the Boolean value at 0x13 (bit 3 of the byte at location 0x22) into the Carry flag.

11.5. Stack

A programmer's stack can be located anywhere in the 256-byte data memory. The stack area is designated using the Stack Pointer (SP, 0x81) SFR. The SP will point to the last location used. The next value pushed on the stack is placed at SP+1 and then SP is incremented. A reset initializes the stack pointer to location 0x07. Therefore, the first value pushed on the stack is placed at location 0x08, which is also the first register (R0) of register bank 1. Thus, if more than one register bank is to be used, the SP should be initialized to a location in the data memory not being used for data storage. The stack depth can extend up to 256 bytes.

SFR Definition 12.2. IP: Interrupt Priority

R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
—	PSPI0	PT2	PS0	PT1	PX1	PT0	PX0	10000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xB8

Bit 7: UNUSED. Read = 1, Write = don't care.
Bit 6: PSPI0: Serial Peripheral Interface (SPI0) Interrupt Priority Control.
This bit sets the priority of the SPI0 interrupt.
0: SPI0 interrupt set to low priority level.
1: SPI0 interrupt set to high priority level.
Bit 5: PT2: Timer 2 Interrupt Priority Control.
This bit sets the priority of the Timer 2 interrupt.
0: Timer 2 interrupt set to low priority level.
1: Timer 2 interrupt set to high priority level.
Bit 4: PS0: UART0 Interrupt Priority Control.
This bit sets the priority of the UART0 interrupt.
0: UART0 interrupt set to low priority level.
1: UART0 interrupt set to high priority level.
Bit 3: PT1: Timer 1 Interrupt Priority Control.
This bit sets the priority of the Timer 1 interrupt.
0: Timer 1 interrupt set to low priority level.
1: Timer 1 interrupt set to high priority level.
Bit 2: PX1: External Interrupt 1 Priority Control.
This bit sets the priority of the External Interrupt 1 interrupt.
0: External Interrupt 1 set to low priority level.
1: External Interrupt 1 set to high priority level.
Bit 1: PT0: Timer 0 Interrupt Priority Control.
This bit sets the priority of the Timer 0 interrupt.
0: Timer 0 interrupt set to low priority level.
1: Timer 0 interrupt set to high priority level.
Bit 0: PX0: External Interrupt 0 Priority Control.
This bit sets the priority of the External Interrupt 0 interrupt.
0: External Interrupt 0 set to low priority level.
1: External Interrupt 0 set to high priority level.

SFR Definition 12.5. IT01CF: INT0/INT1 Configuration

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
IN1PL	IN1SL2	IN1SL1	IN1SL0	IN0PL	IN0SL2	IN0SL1	IN0SL0	00000001
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xE4

Note: Refer to SFR Definition 22.1 for INT0/1 edge- or level-sensitive interrupt selection.

Bit 7: IN1PL: /INT1 Polarity
0: /INT1 input is active low.
1: /INT1 input is active high.

Bits 6–4: IN1SL2–0: /INT1 Port Pin Selection Bits
These bits select which Port pin is assigned to /INT1. Note that this pin assignment is independent of the Crossbar; /INT1 will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin (accomplished by setting to '1' the corresponding bit in register P0SKIP).

IN1SL2–0	/INT1 Port Pin
000	P0.0
001	P0.1
010	P0.2
011	P0.3
100	P0.4
101	P0.5
110	P0.6
111	P0.7

Bit 3: IN0PL: /INT0 Polarity
0: /INT0 interrupt is active low.
1: /INT0 interrupt is active high.

Bits 2–0: INT0SL2–0: /INT0 Port Pin Selection Bits
These bits select which Port pin is assigned to /INT0. Note that this pin assignment is independent of the Crossbar. /INT0 will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin (accomplished by setting to '1' the corresponding bit in register P0SKIP).

IN0SL2–0	/INT0 Port Pin
000	P0.0
001	P0.1
010	P0.2
011	P0.3
100	P0.4
101	P0.5
110	P0.6
111	P0.7

Table 18.1. Port I/O DC Electrical Characteristics

V_{DD} = 2.7 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameters	Conditions	Min	Typ	Max	Units
Output High Voltage	I_{OH} = –3 mA, Port I/O push-pull I_{OH} = –10 µA, Port I/O push-pull I_{OH} = –10 mA, Port I/O push-pull	V_{DD} – 0.7 V_{DD} – 0.1 —	— — V_{DD} – 0.8	— — —	V
Output Low Voltage	I_{OL} = 8.5 mA I_{OL} = 10 µA I_{OL} = 25 mA	— — —	— — 1.0	0.6 0.1 —	V
Input High Voltage		2.0	—	—	V
Input Low Voltage		—	—	0.8	V
Input Leakage Current	Weak Pull-up Off Weak Pull-up On, V_{IN} = 0 V	— —	 25	±1 50	µA

20.1. Enhanced Baud Rate Generation

The UART0 baud rate is generated by Timer 1 in 8-bit auto-reload mode. The TX clock is generated by TL1; the RX clock is generated by a copy of TL1 (shown as RX Timer in Figure 20.2), which is not user-accessible. Both TX and RX Timer overflows are divided by two to generate the TX and RX baud rates. The RX Timer runs when Timer 1 is enabled, and uses the same reload value (TH1). However, an RX Timer reload is forced when a START condition is detected on the RX pin. This allows a receive to begin any time a START is detected, independent of the TX Timer state.

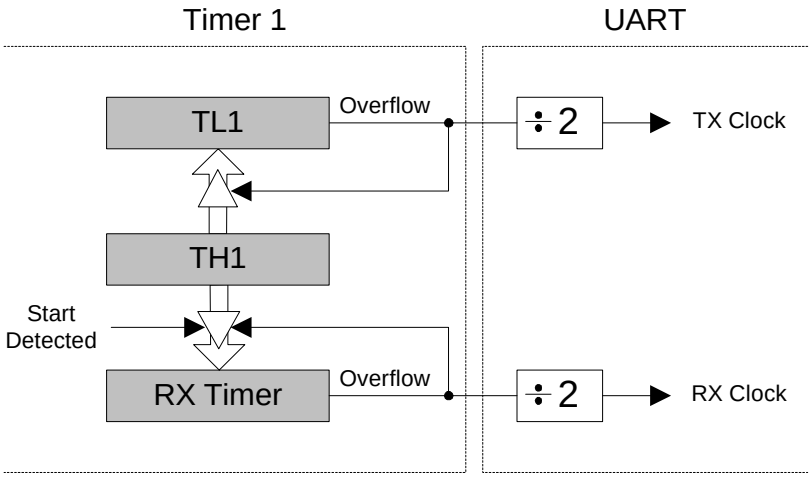

Figure 20.2. UART0 Baud Rate Logic

Timer 1 should be configured for Mode 2, 8-bit auto-reload (see Section "22.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload' on page 197). The Timer 1 reload value should be set so that overflows will occur at two times the desired UART baud rate frequency. Note that Timer 1 may be clocked by one of six sources: SYSCLK, SYSCLK / 4, SYSCLK / 12, SYSCLK / 48, the external oscillator clock / 8, or an external input T1. The UART0 baud rate is determined by Equation 20.1-A and Equation 20.1-B.

A) $$\text{UartBaudRate} = \frac{1}{2} \times \text{T1\_Overflow\_Rate}$$

B) $$\text{T1\_Overflow\_Rate} = \frac{\text{T1}_{\text{CLK}}}{256 - \text{TH1}}$$

Equation 20.1. UART0 Baud Rate

Where $T1_{CLK}$ is the frequency of the clock supplied to Timer 1, and *T1H* is the high byte of Timer 1 (reload value). Timer 1 clock frequency is selected as described in Section "22. Timers' on page 195. A quick reference for typical baud rates and system clock frequencies is given in Table 20.1 through Table 20.6. Note that the internal oscillator may still generate the system clock when the external oscillator is driving Timer 1.

Table 20.5. Timer Settings for Standard Baud Rates Using an External 11.0592 MHz Oscillator

	Frequency: 11.0592 MHz						
	Target Baud Rate (bps)	Baud Rate % Error	Oscilla-tor Divide Factor	Timer Clock Source	SCA1–SCA0 (pre-scale select)*	T1M*	Timer 1 Reload Value (hex)
SYSCLK from External Osc.	230400	0.00%	48	SYSCLK	XX	1	0xE8
	115200	0.00%	96	SYSCLK	XX	1	0xD0
	57600	0.00%	192	SYSCLK	XX	1	0xA0
	28800	0.00%	384	SYSCLK	XX	1	0x40
	14400	0.00%	768	SYSCLK / 12	00	0	0xE0
	9600	0.00%	1152	SYSCLK / 12	00	0	0xD0
	2400	0.00%	4608	SYSCLK / 12	00	0	0x40
	1200	0.00%	9216	SYSCLK / 48	10	0	0xA0
SYSCLK from Internal Osc.	230400	0.00%	48	EXTCLK / 8	11	0	0xFD
	115200	0.00%	96	EXTCLK / 8	11	0	0xFA
	57600	0.00%	192	EXTCLK / 8	11	0	0xF4
	28800	0.00%	384	EXTCLK / 8	11	0	0xE8
	14400	0.00%	768	EXTCLK / 8	11	0	0xD0
	9600	0.00%	1152	EXTCLK / 8	11	0	0xB8

X = Don't care

***Note:** SCA1–SCA0 and T1M bit definitions can be found in Section 22.1.

Table 20.6. Timer Settings for Standard Baud Rates Using an External 3.6864 MHz Oscillator

	Frequency: 3.6864 MHz						
	Target Baud Rate (bps)	Baud Rate% Error	Oscilla-tor Divide Factor	Timer Clock Source	SCA1–SCA0 (pre-scale select)*	T1M*	Timer 1 Reload Value (hex)
SYSCLK from External Osc.	230400	0.00%	16	SYSCLK	XX	1	0xF8
	115200	0.00%	32	SYSCLK	XX	1	0xF0
	57600	0.00%	64	SYSCLK	XX	1	0xE0
	28800	0.00%	128	SYSCLK	XX	1	0xC0
	14400	0.00%	256	SYSCLK	XX	1	0x80
	9600	0.00%	384	SYSCLK	XX	1	0x40
	2400	0.00%	1536	SYSCLK / 12	00	0	0xC0
	1200	0.00%	3072	SYSCLK / 12	00	0	0x80
SYSCLK from Internal Osc.	230400	0.00%	16	EXTCLK / 8	11	0	0xFF
	115200	0.00%	32	EXTCLK / 8	11	0	0xFE
	57600	0.00%	64	EXTCLK / 8	11	0	0xFC
	28800	0.00%	128	EXTCLK / 8	11	0	0xF8
	14400	0.00%	256	EXTCLK / 8	11	0	0xF0
	9600	0.00%	384	EXTCLK / 8	11	0	0xE8

X = Don't care

***Note:** SCA1–SCA0 and T1M bit definitions can be found in Section 22.1.

22.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload

Mode 2 configures Timer 0 and Timer 1 to operate as 8-bit counter/timers with automatic reload of the start value. TL0 holds the count and TH0 holds the reload value. When the counter in TL0 overflows from all ones to 0x00, the timer overflow flag TF0 (TCON.5) is set and the counter in TL0 is reloaded from TH0. If Timer 0 interrupts are enabled, an interrupt will occur when the TF0 flag is set. The reload value in TH0 is not changed. TL0 must be initialized to the desired value before enabling the timer for the first count to be correct. When in Mode 2, Timer 1 operates identically to Timer 0.

Both counter/timers are enabled and configured in Mode 2 in the same manner as Mode 0. Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or when the input signal /INT0 is active as defined by bit IN0PL in register IT01CF (see Section “12.5. External Interrupts’ on page 111 for details on the external input signals /INT0 and /INT1).

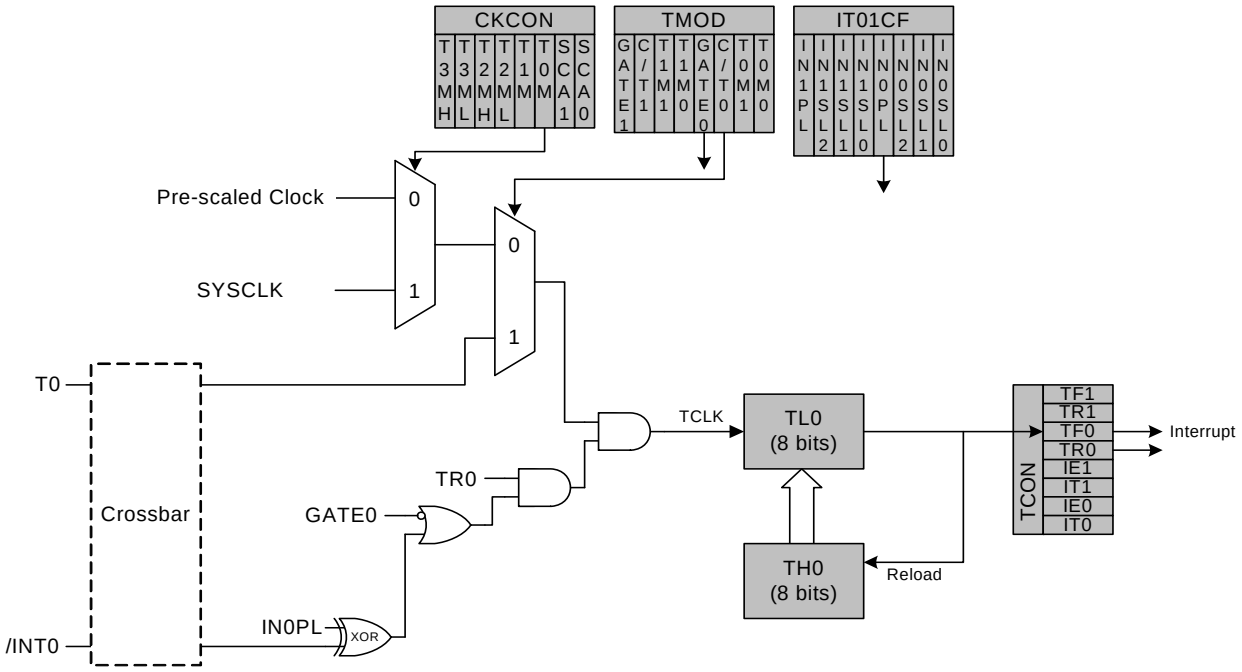

Figure 22.2. T0 Mode 2 Block Diagram

22.2.2. 8-bit Timers with Auto-Reload

When T2SPLIT is set, Timer 2 operates as two 8-bit timers (TMR2H and TMR2L). Both 8-bit timers operate in auto-reload mode as shown in Figure 22.5. TMR2RLL holds the reload value for TMR2L; TMR2RLH holds the reload value for TMR2H. The TR2 bit in TMR2CN handles the run control for TMR2H. TMR2L is always running when configured for 8-bit Mode.

Each 8-bit timer may be configured to use SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. The Timer 2 Clock Select bits (T2MH and T2ML in CKCON) select either SYSCLK or the clock defined by the Timer 2 External Clock Select bit (T2XCLK in TMR2CN), as follows:

T2MH	T2XCLK	TMR2H Clock Source
0	0	SYSCLK / 12
0	1	External Clock / 8
1	X	SYSCLK

T2ML	T2XCLK	TMR2L Clock Source
0	0	SYSCLK / 12
0	1	External Clock / 8
1	X	SYSCLK

The TF2H bit is set when TMR2H overflows from 0xFF to 0x00; the TF2L bit is set when TMR2L overflows from 0xFF to 0x00. When Timer 2 interrupts are enabled (IE.5), an interrupt is generated each time TMR2H overflows. If Timer 2 interrupts are enabled and TF2LEN (TMR2CN.5) is set, an interrupt is generated each time either TMR2L or TMR2H overflows. When TF2LEN is enabled, software must check the TF2H and TF2L flags to determine the source of the Timer 2 interrupt. The TF2H and TF2L interrupt flags are not cleared by hardware and must be manually cleared by software.

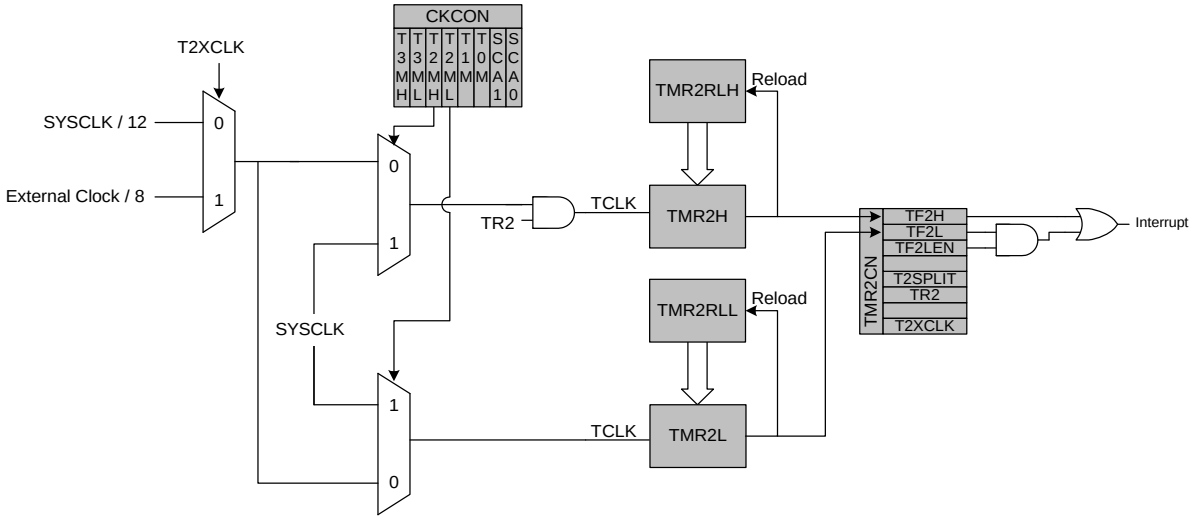

Figure 22.5. Timer 2 8-Bit Mode Block Diagram

22.3. Timer 3

Timer 3 is a 16-bit timer formed by two 8-bit SFRs: TMR3L (low byte) and TMR3H (high byte). Timer 3 may operate in 16-bit auto-reload mode or (split) 8-bit auto-reload mode. The T3SPLIT bit (TMR3CN.3) defines the Timer 3 operation mode.

Timer 3 may be clocked by the system clock, the system clock divided by 12, or the external oscillator source divided by 8. The external clock mode is ideal for real-time clock (RTC) functionality, where the internal oscillator drives the system clock while Timer 3 (and/or the PCA) is clocked by an external precision oscillator. Note that the external oscillator source divided by 8 is synchronized with the system clock.

22.3.1. 16-bit Timer with Auto-Reload

When T3SPLIT (TMR3CN.3) is zero, Timer 3 operates as a 16-bit timer with auto-reload. Timer 3 can be clocked by SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 3 reload registers (TMR3RLH and TM3RLL) is loaded into the Timer 3 register as shown in Figure 22.6, and the Timer 3 High Byte Overflow Flag (TMR3CN.7) is set. If Timer 3 interrupts are enabled, an interrupt will be generated each Timer 3 overflow. Additionally, if Timer 3 interrupts are enabled and the TF3LEN bit is set (TMR3CN.5), an interrupt will be generated each time the lower 8 bits (TMR3L) overflow from 0xFF to 0x00.

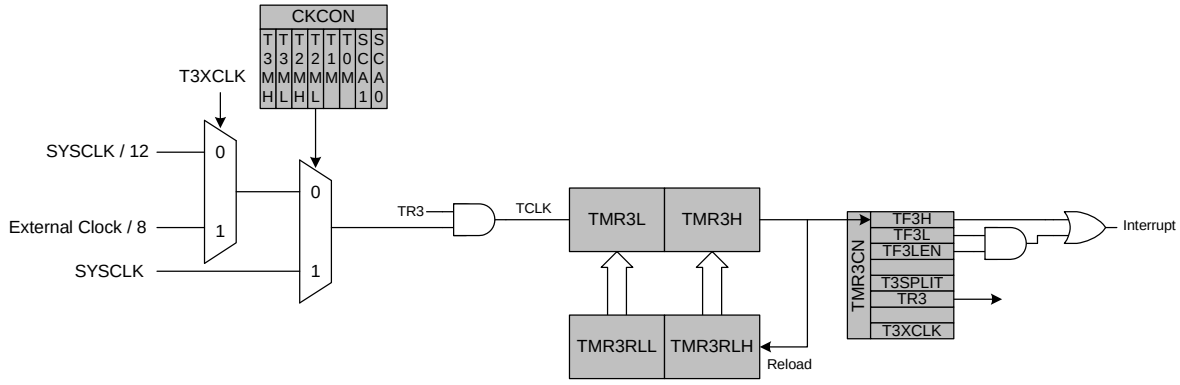

Figure 22.6. Timer 3 16-Bit Mode Block Diagram

22.3.2. 8-bit Timers with Auto-Reload

When T3SPLIT is set, Timer 3 operates as two 8-bit timers (TMR3H and TMR3L). Both 8-bit timers operate in auto-reload mode as shown in Figure 22.7. TMR3RLL holds the reload value for TMR3L; TMR3RLH holds the reload value for TMR3H. The TR3 bit in TMR3CN handles the run control for TMR3H. TMR3L is always running when configured for 8-bit Mode.

Each 8-bit timer may be configured to use SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. The Timer 3 Clock Select bits (T3MH and T3ML in CKCON) select either SYSCLK or the clock defined by the Timer 3 External Clock Select bit (T3XCLK in TMR3CN), as follows:

T3MH	T3XCLK	TMR3H Clock Source
0	0	SYSCLK / 12
0	1	External Clock / 8
1	X	SYSCLK

T3ML	T3XCLK	TMR3L Clock Source
0	0	SYSCLK / 12
0	1	External Clock / 8
1	X	SYSCLK

The TF3H bit is set when TMR3H overflows from 0xFF to 0x00; the TF3L bit is set when TMR3L overflows from 0xFF to 0x00. When Timer 3 interrupts are enabled (IE.5), an interrupt is generated each time TMR3H overflows. If Timer 3 interrupts are enabled and TF3LEN (TMR3CN.5) is set, an interrupt is generated each time either TMR3L or TMR3H overflows. When TF3LEN is enabled, software must check the TF3H and TF3L flags to determine the source of the Timer 3 interrupt. The TF3H and TF3L interrupt flags are not cleared by hardware and must be manually cleared by software.

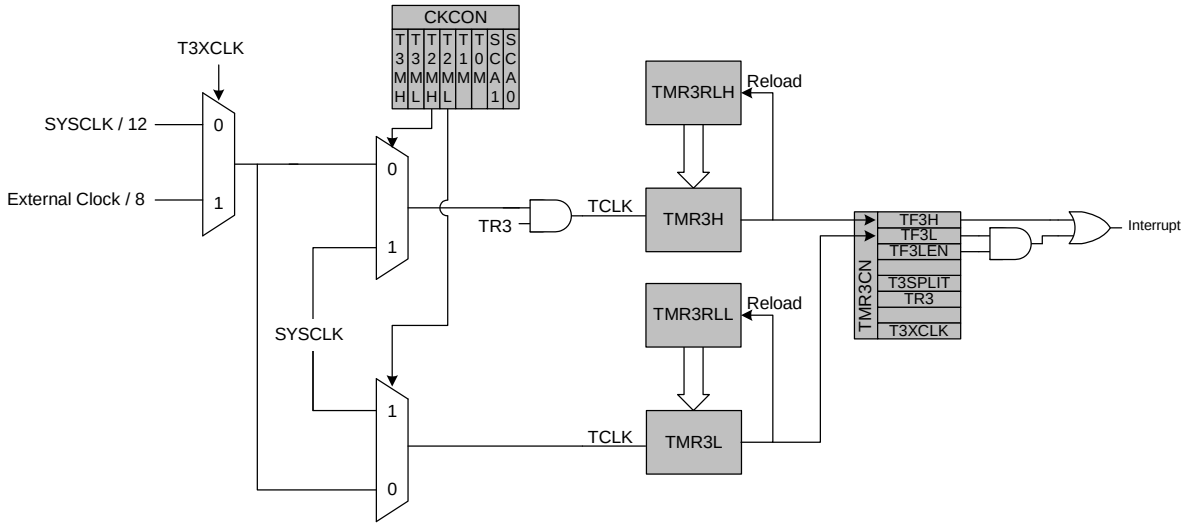

Figure 22.7. Timer 3 8-Bit Mode Block Diagram

23.2.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes the PCA to capture the value of the PCA counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPLn and PCA0CPHn). The CAPPn and CAPNn bits in the PCA0CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1 and an interrupt request is generated if CCF interrupts are enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPPn and CAPNn bits are set to logic 1, then the state of the Port pin associated with CEXn can be read directly to determine whether a rising-edge or falling-edge caused the capture.

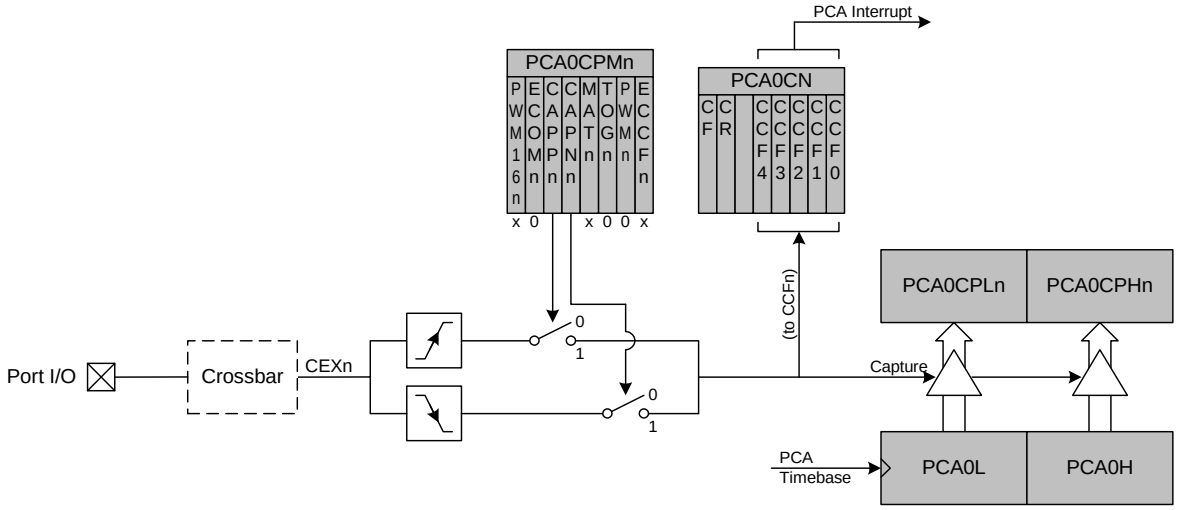

Figure 23.4. PCA Capture Mode Diagram

Note: The CEXn input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.