# Lattice Semiconductor Corporation - LAMXO1200E-3TN144E Datasheet

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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Active |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 5.1 ns |
| Voltage Supply - Internal | 1.14V ~ 1.26V |
| Number of Logic Elements/Blocks | - |
| Number of Macrocells | 600 |
| Number of Gates | - |
| Number of I/O | 113 |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lamxo1200e-3tn144e |

**Modes of Operation**

Each Slice is capable of four modes of operation: Logic, Ripple, RAM, and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

***Table 2-2. Slice Modes***

| | Logic | Ripple | RAM | ROM |
|---|---|---|---|---|
| PFU Slice | LUT 4x2 or LUT 5x1 | 2-bit Arithmetic Unit | SP 16x2 | ROM 16x1 x 2 |
| PFF Slice | LUT 4x2 or LUT 5x1 | 2-bit Arithmetic Unit | N/A | ROM 16x1 x 2 |

**Logic Mode:** In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables (LUT4). A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7, and LUT8 can be constructed by concatenating other Slices.

**Ripple Mode:** Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two additional signals, Carry Generate and Carry Propagate, are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

**RAM Mode:** In this mode, distributed RAM can be constructed using each LUT block as a 16x2-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

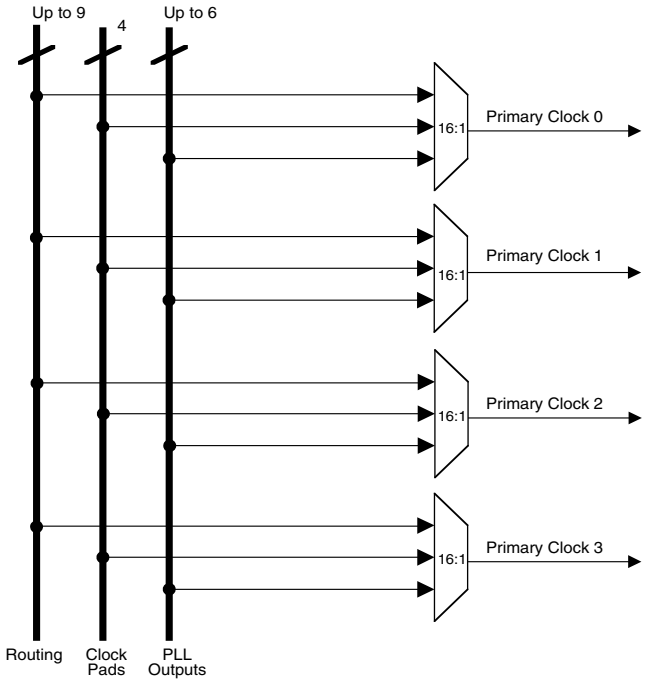
The ispLEVER design tool supports the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-6 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices. One Slice functions as the read-write port, while the other companion Slice supports the read-only port. For more information on RAM mode in LA-MachXO devices, please see details of additional technical documentation at the end of this data sheet.

***Table 2-3. Number of Slices Required For Implementing Distributed RAM***

| | SPR16x2 | DPR16x2 |
|---|---|---|
| Number of Slices | 1 | 2 |

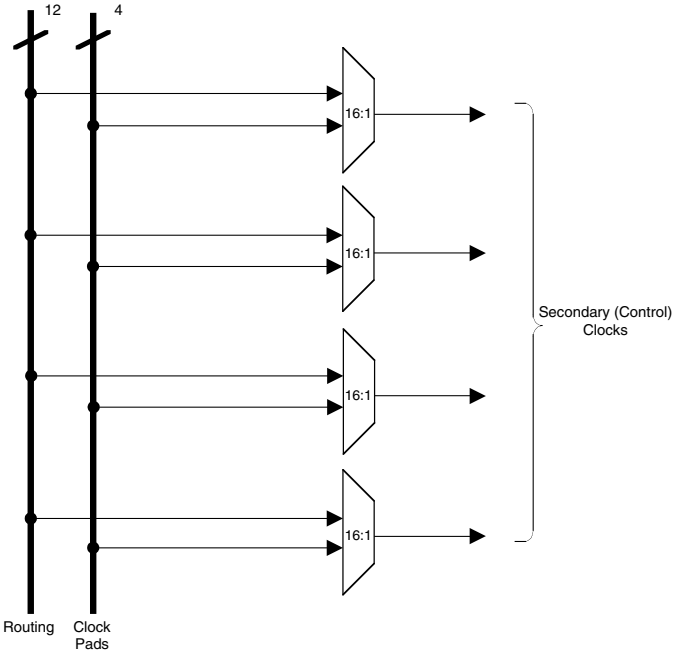
Note: SPR = Single Port RAM, DPR = Dual Port RAM

***Figure 2-8. Primary Clocks for LA-MachXO1200 and LA-MachXO2280 Devices***




Four secondary clocks are generated from four 16:1 muxes as shown in Figure 2-9. Four of the secondary clock sources come from dual function clock pins and 12 come from internal routing.

***Figure 2-9. Secondary Clocks for LA-MachXO Devices***



## sysCLOCK Phase Locked Loops (PLLs)

The LA-MachXO1200 and LA-MachXO2280 provide PLL support. The source of the PLL input divider can come from an external pin or from internal routing. There are four sources of feedback signals to the feedback divider: from CLKINTFB (internal feedback port), from the global clock nets, from the output of the post scalar divider, and from the routing (or from an external pin). There is a PLL_LOCK signal to indicate that the PLL has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the $t_{LOCK}$ parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider, and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

***Figure 2-10. PLL Diagram***

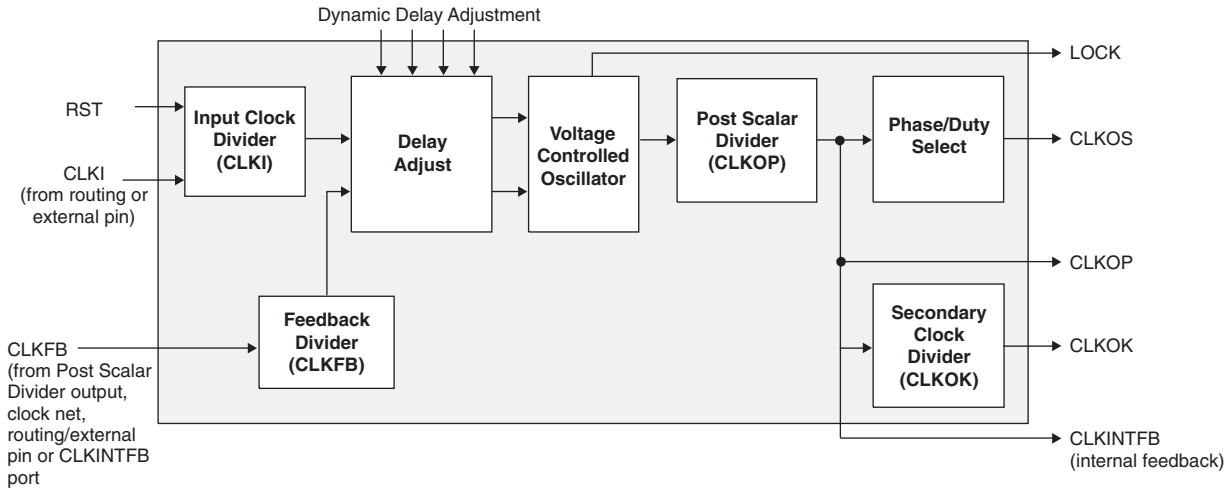
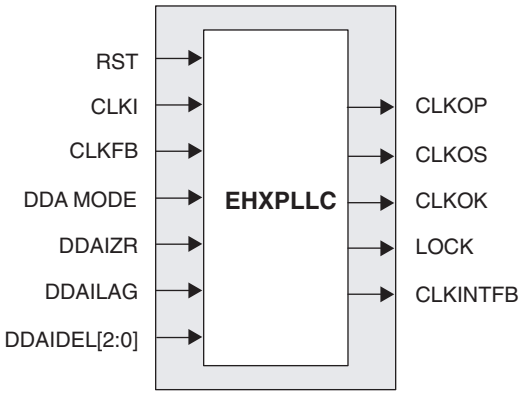



Figure 2-11 shows the available macros for the PLL. Table 2-5 provides signal description of the PLL Block.

***Figure 2-11. PLL Primitive***



of the devices also support differential input buffers. PCI clamps are available on the top Bank I/O buffers. The PCI clamp is enabled after $V_{CC}$, $V_{CCAUX}$, and $V_{CCIO}$ are at valid operating levels and the device has been configured.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

2. **Left and Right sysIO Buffer Pairs**
The sysIO buffer pairs in the left and right Banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (supporting ratioed and absolute input levels). The devices also have a differential driver per output pair. The referenced input buffer can also be configured as a differential input buffer. In these Banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

**Typical I/O Behavior During Power-up**
The internal power-on-reset (POR) signal is deactivated when $V_{CC}$ and $V_{CCAUX}$ have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all $V_{CCIO}$ Banks are active with valid input logic levels to properly control the output logic states of all the I/O Banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-up to VCCIO. The I/O pins will maintain the blank configuration until VCC, VCCAUX and VCCIO have reached satisfactory levels at which time the I/Os will take on the user-configured settings.

The $V_{CC}$ and $V_{CCAUX}$ supply the power to the FPGA core fabric, whereas the $V_{CCIO}$ supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, the I/O buffers should be powered up along with the FPGA core fabric. Therefore, $V_{CCIO}$ supplies should be powered up before or together with the $V_{CC}$ and $V_{CCAUX}$ supplies

**Supported Standards**
The LA-MachXO sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS and LVTTL. The buffer supports the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS and LVPECL output emulation is supported on all devices. The LA-MachXO1200 and LA-MachXO2280 support on-chip LVDS output buffers on approximately 50% of the I/Os on the left and right Banks. Differential receivers for LVDS, BLVDS and LVPECL are supported on all Banks of LA-MachXO1200 and LA-MachXO2280 devices. PCI support is provided in the top Banks of the LA-MachXO1200 and LA-MachXO2280 devices. Table 2-8 summarizes the I/O characteristics of the devices in the LA-MachXO family.

Tables 2-9 and 2-10 show the I/O standards (together with their supply and reference voltages) supported by the LA-MachXO devices. For further information on utilizing the sysIO buffer to support a variety of standards please see the details of additional technical documentation at the end of this data sheet.

*Table 2-10. Supported Output Standards*

| Output Standard | Drive | $V_{CCIO}$ (Typ.) |
|---|---|---|
| **Single-ended Interfaces** | | |
| LVTTL | 4mA, 8mA, 12mA, 16mA | 3.3 |
| LVCMOS33 | 4mA, 8mA, 12mA, 14mA | 3.3 |
| LVCMOS25 | 4mA, 8mA, 12mA, 14mA | 2.5 |
| LVCMOS18 | 4mA, 8mA, 12mA, 14mA | 1.8 |
| LVCMOS15 | 4mA, 8mA | 1.5 |
| LVCMOS12 | 2mA, 6mA | 1.2 |
| LVCMOS33, Open Drain | 4mA, 8mA, 12mA, 14mA | — |
| LVCMOS25, Open Drain | 4mA, 8mA, 12mA, 14mA | — |
| LVCMOS18, Open Drain | 4mA, 8mA, 12mA, 14mA | — |
| LVCMOS15, Open Drain | 4mA, 8mA | — |
| LVCMOS12, Open Drain | 2mA, 6mA | — |
| PCI33[3] | N/A | 3.3 |
| **Differential Interfaces** | | |
| LVDS[1, 2] | N/A | 2.5 |
| BLVDS, RSDS[2] | N/A | 2.5 |
| LVPECL[2] | N/A | 3.3 |

1. LA-MachXO1200 and LA-MachXO2280 devices have dedicated LVDS buffers.
2. These interfaces can be emulated with external resistors in all devices.
3. Top Banks of LA-MachXO1200 and LA-MachXO2280 devices only.

## sysIO Buffer Banks

The number of Banks vary between the devices of this family. Eight Banks surround the two larger devices, the LA-MachXO1200 and LA-MachXO2280 (two Banks per side). The LA-MachXO640 has four Banks (one Bank per side). The smallest member of this family, the LA-MachXO256, has only two Banks.

Each sysIO buffer Bank is capable of supporting multiple I/O standards. Each Bank has its own I/O supply voltage ($V_{CCIO}$) which allows it to be completely independent from the other Banks. Figure 2-18, Figure 2-18, Figure 2-20 and Figure 2-21 shows the sysIO Banks and their associated supplies for all devices.

## Device Configuration

All LA-MachXO devices contain a test access port that can be used for device configuration and programming.

The non-volatile memory in the LA-MachXO can be configured in two different modes:

- In IEEE 1532 mode via the IEEE 1149.1 port. In this mode, the device is off-line and I/Os are controlled by BSCAN registers.
- In background mode via the IEEE 1149.1 port. This allows the device to remain operational in user mode while reprogramming takes place.

The SRAM configuration memory can be configured in three different ways:

- At power-up via the on-chip non-volatile memory.
- After a refresh command is issued via the IEEE 1149.1 port.
- In IEEE 1532 mode via the IEEE 1149.1 port.

Figure 2-22 provides a pictorial representation of the different programming modes available in the LA-MachXO devices. On power-up, the SRAM is ready to be configured with IEEE 1149.1 serial TAP port using IEEE 1532 protocols.

**Leave Alone I/O**
When using IEEE 1532 mode for non-volatile memory programming, SRAM configuration, or issuing a refresh command, users may specify I/Os as high, low, tristated or held at current value. This provides excellent flexibility for implementing systems where reconfiguration or reprogramming occurs on-the-fly.

**TransFR (Transparent Field Reconfiguration)**
TransFR (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. See Lattice technical note #TN1087, *Minimizing System Interruption During Configuration Using TransFR Technology,* for details.

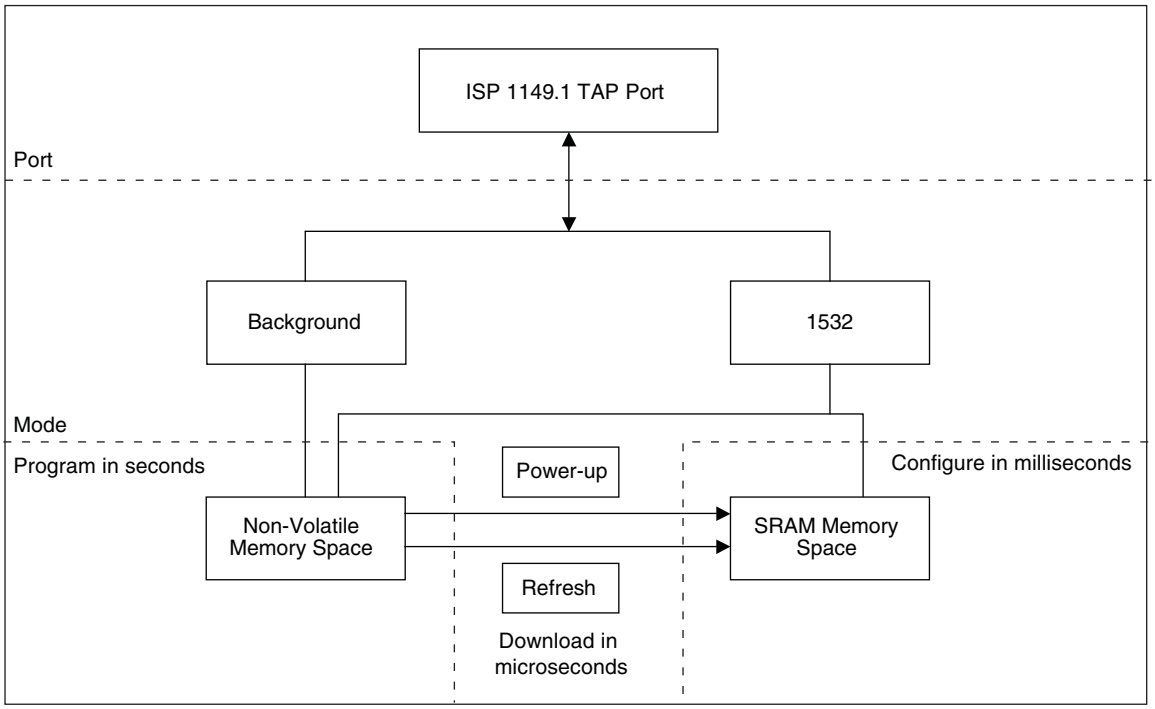
**Security**
The LA-MachXO automotive devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile memory spaces. Once set, the only way to clear the security bits is to erase the memory space.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

# AEC-Q100 Tested and Qualified

The Automotive Electronics Council (AEC) consists of two committees: the Quality Systems Committee and the Component Technical Committee. These committees are composed of representatives from sustaining and other associate members. The AEC Component Technical Committee is the standardization body for establishing standards for reliable, high quality electronic components. In particular, the AEC-Q100 specification “Stress Test for Qualification for Integrated Circuits” defines qualification and re-qualification requirements for electronic components. Components meeting these specifications are suitable for use in the harsh automotive environment without additional component-level qualification testing. Lattice's LA-ispMACH 4000V and LA-MachXO devices completed and passed the requirements of the AEC-Q100 specification.

*Figure 2-22. LA-MachXO Configuration and Programming*




## Density Shifting

The LA-MachXO family has been designed to enable density migration in the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

## LA-MachXO1200 and LA-MachXO2280 Hot Socketing Specifications[1, 2, 3, 4]

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Non-LVDS General Purpose sysIOs** | | | | | | |
| $I_{DK}$ | Input or I/O Leakage Current | $0 \le V_{IN} \le V_{IH}$ (MAX.) | — | — | +/-1000 | µA |
| **LVDS General Purpose sysIOs** | | | | | | |
| $I_{DK\_LVDS}$ | Input or I/O Leakage Current | $V_{IN} \le V_{CCIO}$ | — | — | +/-1000 | µA |
| | | $V_{IN} > V_{CCIO}$ | — | 35 | — | mA |

1. Insensitive to sequence of $V_{CC}$, $V_{CCAUX}$, and $V_{CCIO}$. However, assumes monotonic rise/fall rates for $V_{CC}$, $V_{CCAUX}$, and $V_{CCIO}$.
2. $0 \le V_{CC} \le V_{CC}$ (MAX), $0 \le V_{CCIO} \le V_{CCIO}$ (MAX), and $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX).
3. $I_{DK}$ is additive to $I_{PU}$, $I_{PW}$ or $I_{BH}$.
4. LVCMOS and LVTTL only.

## DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1, 4, 5] | Input or I/O Leakage | $0 \le V_{IN} \le (V_{CCIO} - 0.2V)$ | — | — | 10 | µA |
| | | $(V_{CCIO} - 0.2V) < V_{IN} \le 3.6V$ | — | — | 40 | µA |
| $I_{PU}$ | I/O Active Pull-up Current | $0 \le V_{IN} \le 0.7\ V_{CCIO}$ | -30 | — | -150 | µA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$ (MAX) $\le V_{IN} \le V_{IH}$ (MAX) | 30 | — | 150 | µA |
| $I_{BHLS}$ | Bus Hold Low sustaining current | $V_{IN} = V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High sustaining current | $V_{IN} = 0.7V_{CCIO}$ | -30 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive current | $0 \le V_{IN} \le V_{IH}$ (MAX) | — | — | 150 | µA |
| $I_{BHHO}$ | Bus Hold High Overdrive current | $0 \le V_{IN} \le V_{IH}$ (MAX) | — | — | -150 | µA |
| $V_{BHT}$[3] | Bus Hold trip Points | $0 \le V_{IN} \le V_{IH}$ (MAX) | $V_{IL}$ (MAX) | — | $V_{IH}$ (MIN) | V |
| C1 | I/O Capacitance[2] | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = Typ., $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 8 | — | pf |
| C2 | Dedicated Input Capacitance[2] | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = Typ., $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 8 | — | pf |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. $T_A$ 25°C, f = 1.0MHz
3. Please refer to $V_{IL}$ and $V_{IH}$ in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Not applicable to SLEEPN pin.
5. When $V_{IH}$ is higher than $V_{CCIO}$, a transient current typically of 30ns in duration or less with a peak current of 6mA can occur on the high-to-low transition. For LA-MachXO1200 and LA-MachXO2280 true LVDS output pins, $V_{IH}$ must be less than or equal to $V_{CCIO}$.

## Supply Current (Sleep Mode)[1, 2]

| Symbol | Parameter | Device | Typ.[3] | Max. | Units |
|---|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LCMXO256C | 12 | 25 | µA |
| | | LCMXO640C | 12 | 25 | µA |
| $I_{CCAUX}$ | Auxiliary Power Supply | LCMXO256C | 1 | 15 | µA |
| | | LCMXO640C | 1 | 25 | µA |
| $I_{CCIO}$ | Bank Power Supply[4] | All LCMXO 'C' Devices | 2 | 30 | µA |

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.
2. Frequency = 0MHz.
3. $T_A$ = 25°C, power supplies at nominal voltage.
4. Per Bank.

## Supply Current (Standby)[1, 2, 3, 4]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typ.[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | LCMXO256C | 7 | mA |
| | | LCMXO640C | 9 | mA |
| | | LCMXO256E | 4 | mA |
| | | LCMXO640E | 6 | mA |
| | | LCMXO1200E | 10 | mA |
| | | LCMXO2280E | 12 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply $V_{CCAUX}$ = 3.3V | LCMXO256E/C | 5 | mA |
| | | LCMXO640E/C | 7 | mA |
| | | LCMXO1200E | 12 | mA |
| | | LCMXO2280E | 13 | mA |
| $I_{CCIO}$ | Bank Power Supply[6] | All devices | 2 | mA |

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at $V_{CCIO}$ or GND.
3. Frequency = 0MHz.
4. User pattern = blank.
5. $T_J$ = 25ºC, power supplies at nominal voltage.
6. Per Bank. $V_{CCIO}$ = 2.5V. Does not include pull-up/pull-down.

## sysIO Recommended Operating Conditions

| Standard | $V_{CCIO}$ (V) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| LVCMOS 3.3 | 3.135 | 3.3 | 3.465 |
| LVCMOS 2.5 | 2.375 | 2.5 | 2.625 |
| LVCMOS 1.8 | 1.71 | 1.8 | 1.89 |
| LVCMOS 1.5 | 1.425 | 1.5 | 1.575 |
| LVCMOS 1.2 | 1.14 | 1.2 | 1.26 |
| LVTTL | 3.135 | 3.3 | 3.465 |
| PCI[3] | 3.135 | 3.3 | 3.465 |
| LVDS[1, 2] | 2.375 | 2.5 | 2.625 |
| LVPECL[1] | 3.135 | 3.3 | 3.465 |
| BLVDS[1] | 2.375 | 2.5 | 2.625 |
| RSDS[1] | 2.375 | 2.5 | 2.625 |

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. MachXO1200 and MachXO2280 devices have dedicated LVDS buffers
3. Input on the top bank of the MachXO1200 and MachXO2280 only.

*Table 3-1. LVDS DC Conditions*

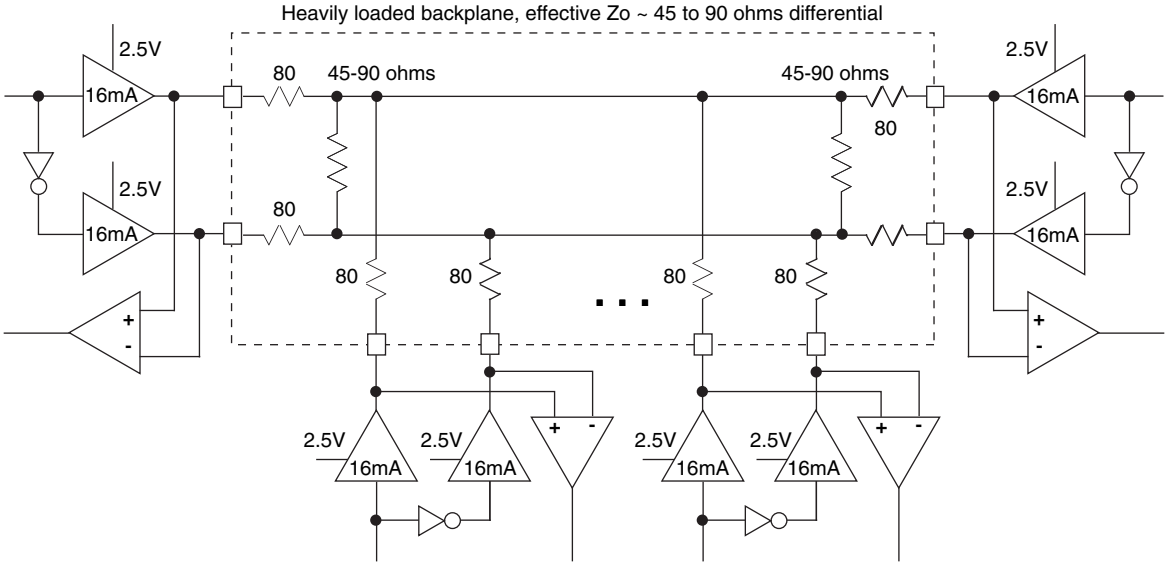
**Over Recommended Operating Conditions**

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ω |
| $R_S$ | Driver series resistor | 294 | Ω |
| $R_P$ | Driver parallel resistor | 121 | Ω |
| $R_T$ | Receiver termination | 100 | Ω |
| $V_{OH}$ | Output high voltage | 1.43 | V |
| $V_{OL}$ | Output low voltage | 1.07 | V |
| $V_{OD}$ | Output differential voltage | 0.35 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 100 | Ω |
| $I_{DC}$ | DC output current | 3.66 | mA |

## BLVDS

The LA-MachXO automotive family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. The input standard is supported by the LVDS differential input buffer on certain devices. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

*Figure 3-2. BLVDS Multi-point Output Example*



# LA-MachXO Internal Timing Parameters[1]

**Over Recommended Operating Conditions**

| Parameter | Description | -3 | | Units |
|---|---|---|---|---|
| | | Min. | Max. | |
| **PFU/PFF Logic Mode Timing** | | | | |
| $t_{LUT4\_PFU}$ | LUT4 delay (A to D inputs to F output) | — | 0.39 | ns |
| $t_{LUT6\_PFU}$ | LUT6 delay (A to D inputs to OFX output) | — | 0.62 | ns |
| $t_{LSR\_PFU}$ | Set/Reset to output of PFU | — | 1.26 | ns |
| $t_{SUM\_PFU}$ | Clock to Mux (M0,M1) input setup time | 0.15 | — | ns |
| $t_{HM\_PFU}$ | Clock to Mux (M0,M1) input hold time | -0.07 | — | ns |
| $t_{SUD\_PFU}$ | Clock to D input setup time | 0.18 | — | ns |
| $t_{HD\_PFU}$ | Clock to D input hold time | -0.04 | — | ns |
| $t_{CK2Q\_PFU}$ | Clock to Q delay, D-type register configuration | — | 0.56 | ns |
| $t_{LE2Q\_PFU}$ | Clock to Q delay latch configuration | — | 0.74 | ns |
| $t_{LD2Q\_PFU}$ | D to Q throughput delay when latch is enabled | — | 0.77 | ns |
| **PFU Dual Port Memory Mode Timing** | | | | |
| $t_{CORAM\_PFU}$ | Clock to Output | — | 0.56 | ns |
| $t_{SUDATA\_PFU}$ | Data Setup Time | -0.25 | — | ns |
| $t_{HDATA\_PFU}$ | Data Hold Time | 0.39 | — | ns |
| $t_{SUADDR\_PFU}$ | Address Setup Time | -0.65 | — | ns |
| $t_{HADDR\_PFU}$ | Address Hold Time | 0.99 | — | ns |
| $t_{SUWREN\_PFU}$ | Write/Read Enable Setup Time | -0.30 | — | ns |
| $t_{HWREN\_PFU}$ | Write/Read Enable Hold Time | 0.47 | — | ns |
| **PIO Input/Output Buffer Timing** | | | | |
| $t_{IN\_PIO}$ | Input Buffer Delay | — | 1.06 | ns |
| $t_{OUT\_PIO}$ | Output Buffer Delay | — | 1.80 | ns |
| **EBR Timing (1200 and 2280 Devices Only)** | | | | |
| $t_{CO\_EBR}$ | Clock to output from Address or Data with no output register | — | 3.14 | ns |
| $t_{COO\_EBR}$ | Clock to output from EBR output Register | — | 0.75 | ns |
| $t_{SUDATA\_EBR}$ | Setup Data to EBR Memory | -0.37 | — | ns |
| $t_{HDATA\_EBR}$ | Hold Data to EBR Memory | 0.57 | — | ns |
| $t_{SUADDR\_EBR}$ | Setup Address to EBR Memory | -0.37 | — | ns |
| $t_{HADDR\_EBR}$ | Hold Address to EBR Memory | 0.57 | — | ns |
| $t_{SUWREN\_EBR}$ | Setup Write/Read Enable to EBR Memory | -0.23 | — | ns |
| $t_{HWREN\_EBR}$ | Hold Write/Read Enable to EBR Memory | 0.36 | — | ns |
| $t_{SUCE\_EBR}$ | Clock Enable Setup Time to EBR Output Register | 0.27 | — | ns |
| $t_{HCE\_EBR}$ | Clock Enable Hold Time to EBR Output Register | -0.18 | — | ns |
| $t_{RSTO\_EBR}$ | Reset To Output Delay Time from EBR Output Register | — | 1.44 | ns |
| **PLL Parameters (1200 and 2280 Devices Only)** | | | | |
| $t_{RSTREC}$ | Reset Recovery to Rising Clock | — | 1.00 | ns |
| $t_{RSTSU}$ | Reset Signal Setup Time | 1.00 | — | ns |

1. Internal parameters are characterized but not tested on every device.

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## LA-MachXO Family Timing Adders[1, 2, 3]

**Over Recommended Operating Conditions**

| Buffer Type | Description | -3 | Units |
|---|---|---|---|
| **Input Adjusters** | | | |
| LVDS25[4] | LVDS | 0.61 | ns |
| BLVDS25[4] | BLVDS | 0.61 | ns |
| LVPECL33[4] | LVPECL | 0.59 | ns |
| LVTTL33 | LVTTL | 0.01 | ns |
| LVCMOS33 | LVCMOS 3.3 | 0.01 | ns |
| LVCMOS25 | LVCMOS 2.5 | 0.00 | ns |
| LVCMOS18 | LVCMOS 1.8 | 0.10 | ns |
| LVCMOS15 | LVCMOS 1.5 | 0.19 | ns |
| LVCMOS12 | LVCMOS 1.2 | 0.56 | ns |
| PCI33[4] | PCI | 0.01 | ns |
| **Output Adjusters** | | | |
| LVDS25E | LVDS 2.5 E | -0.18 | ns |
| LVDS25[4] | LVDS 2.5 | -0.30 | ns |
| BLVDS25 | BLVDS 2.5 | -0.04 | ns |
| LVPECL33 | LVPECL 3.3 | 0.05 | ns |
| LVTTL33_4mA | LVTTL 4mA drive | 0.05 | ns |
| LVTTL33_8mA | LVTTL 8mA drive | 0.08 | ns |
| LVTTL33_12mA | LVTTL 12mA drive | -0.01 | ns |
| LVTTL33_16mA | LVTTL 16mA drive | 0.70 | ns |
| LVCMOS33_4mA | LVCMOS 3.3 4mA drive | 0.05 | ns |
| LVCMOS33_8mA | LVCMOS 3.3 8mA drive | 0.08 | ns |
| LVCMOS33_12mA | LVCMOS 3.3 12mA drive | -0.01 | ns |
| LVCMOS33_14mA | LVCMOS 3.3 14mA drive | 0.70 | ns |
| LVCMOS25_4mA | LVCMOS 2.5 4mA drive | 0.07 | ns |
| LVCMOS25_8mA | LVCMOS 2.5 8mA drive | 0.13 | ns |
| LVCMOS25_12mA | LVCMOS 2.5 12mA drive | 0.00 | ns |
| LVCMOS25_14mA | LVCMOS 2.5 14mA drive | 0.47 | ns |
| LVCMOS18_4mA | LVCMOS 1.8 4mA drive | 0.15 | ns |
| LVCMOS18_8mA | LVCMOS 1.8 8mA drive | 0.06 | ns |
| LVCMOS18_12mA | LVCMOS 1.8 12mA drive | -0.08 | ns |
| LVCMOS18_14mA | LVCMOS 1.8 14mA drive | 0.09 | ns |
| LVCMOS15_4mA | LVCMOS 1.5 4mA drive | 0.22 | ns |
| LVCMOS15_8mA | LVCMOS 1.5 8mA drive | 0.07 | ns |
| LVCMOS12_2mA | LVCMOS 1.2 2mA drive | 0.36 | ns |
| LVCMOS12_6mA | LVCMOS 1.2 6mA drive | 0.07 | ns |
| PCI33[4] | PCI33 | 2.59 | ns |

1. Timing adders are characterized but not tested on every device.
2. LVCMOS timing is measured with the load specified in Switching Test Conditions table.
3. All other standards tested according to the appropriate specifications.
4. I/O standard only available in LCMXO1200 and LCMXO2280 devices.

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## Switching Test Conditions

Figure 3-6 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3-5.

***Figure 3-6. Output Test Load, LVTTL and LVCMOS Standards***

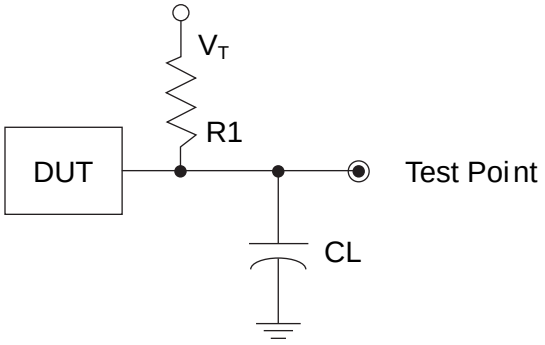


***Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces***

| Test Condition | $R_1$ | $C_L$ | Timing Ref. | $V_T$ |
|---|---|---|---|---|
| LVTTL and LVCMOS settings (L -> H, H -> L) | ∞ | 0pF | LVTTL, LVCMOS 3.3 = 1.5V | — |
| | | | LVCMOS 2.5 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.8 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.5 = $V_{CCIO}/2$ | — |
| | | | LVCMOS 1.2 = $V_{CCIO}/2$ | — |
| LVTTL and LVCMOS 3.3 (Z -> H) | 188 | 0pF | 1.5 | $V_{OL}$ |
| LVTTL and LVCMOS 3.3 (Z -> L) | | | | $V_{OH}$ |
| Other LVCMOS (Z -> H) | | | $V_{CCIO}/2$ | $V_{OL}$ |
| Other LVCMOS (Z -> L) | | | $V_{CCIO}/2$ | $V_{OH}$ |
| LVTTL + LVCMOS (H -> Z) | | | $V_{OH}$ - 0.15 | $V_{OL}$ |
| LVTTL + LVCMOS (L -> Z) | | | $V_{OL}$ - 0.15 | $V_{OH}$ |

Note: Output test conditions for all other interfaces are determined by the respective standards.

## LA-MachXO1200 and LA-MachXO2280 Logic Signal Connections: 100 TQFP

| Pin Number | LAMXO1200 | | | | LAMXO2280 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Dual Function | Differential | Ball Function | Bank | Dual Function | Differential |
| 1 | PL2A | 7 | | T | PL2A | 7 | LUM0_PLLT_FB_A | T |
| 2 | PL2B | 7 | | C | PL2B | 7 | LUM0_PLLC_FB_A | C |
| 3 | PL3C | 7 | | T | PL3C | 7 | LUM0_PLLT_IN_A | T |
| 4 | PL3D | 7 | | C | PL3D | 7 | LUM0_PLLC_IN_A | C |
| 5 | PL4B | 7 | | | PL4B | 7 | | |
| 6 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| 7 | PL6A | 7 | | T* | PL7A | 7 | | T* |
| 8 | PL6B | 7 | GSRN | C* | PL7B | 7 | GSRN | C* |
| 9 | GND | - | | | GND | - | | |
| 10 | PL7C | 7 | | T | PL9C | 7 | | T |
| 11 | PL7D | 7 | | C | PL9D | 7 | | C |
| 12 | PL8C | 7 | | T | PL10C | 7 | | T |
| 13 | PL8D | 7 | | C | PL10D | 7 | | C |
| 14 | PL9C | 6 | | | PL11C | 6 | | |
| 15 | PL10A | 6 | | T* | PL13A | 6 | | T* |
| 16 | PL10B | 6 | | C* | PL13B | 6 | | C* |
| 17 | VCC | - | | | VCC | - | | |
| 18 | PL11B | 6 | | | PL14D | 6 | | C |
| 19 | PL11C | 6 | TSALL | | PL14C | 6 | TSALL | T |
| 20 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| 21 | PL13C | 6 | | | PL16C | 6 | | |
| 22 | PL14A | 6 | LLM0_PLLT_FB_A | T* | PL17A | 6 | LLM0_PLLT_FB_A | T* |
| 23 | PL14B | 6 | LLM0_PLLC_FB_A | C* | PL17B | 6 | LLM0_PLLC_FB_A | C* |
| 24 | PL15A | 6 | LLM0_PLLT_IN_A | T* | PL18A | 6 | LLM0_PLLT_IN_A | T* |
| 25 | PL15B | 6 | LLM0_PLLC_IN_A | C* | PL18B | 6 | LLM0_PLLC_IN_A | C* |
| 26** | GNDIO6 GNDIO5 | - | | | GNDIO6 GNDIO5 | - | | |
| 27 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 28 | TMS | 5 | TMS | | TMS | 5 | TMS | |
| 29 | TCK | 5 | TCK | | TCK | 5 | TCK | |
| 30 | PB3B | 5 | | | PB3B | 5 | | |
| 31 | PB4A | 5 | | T | PB4A | 5 | | T |
| 32 | PB4B | 5 | | C | PB4B | 5 | | C |
| 33 | TDO | 5 | TDO | | TDO | 5 | TDO | |
| 34 | TDI | 5 | TDI | | TDI | 5 | TDI | |
| 35 | VCC | - | | | VCC | - | | |
| 36 | VCCAUX | - | | | VCCAUX | - | | |
| 37 | PB6E | 5 | | T | PB8E | 5 | | T |
| 38 | PB6F | 5 | | C | PB8F | 5 | | C |
| 39 | PB7B | 4 | PCLK4_1*** | | PB10F | 4 | PCLK4_1*** | |
| 40 | PB7F | 4 | PCLK4_0*** | | PB10B | 4 | PCLK4_0*** | |

## LA-MachXO1200 and LA-MachXO2280 Logic Signal Connections: 100 TQFP (Cont.)

| Pin Number | LAMXO1200 | | | | LAMXO2280 | | | |
|---|---|---|---|---|---|---|---|---|
| | Ball Function | Bank | Dual Function | Differential | Ball Function | Bank | Dual Function | Differential |
| 41 | GND | - | | | GND | - | | |
| 42 | PB9A | 4 | | T | PB12A | 4 | | T |
| 43 | PB9B | 4 | | C | PB12B | 4 | | C |
| 44 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| 45 | PB10A | 4 | | T | PB13A | 4 | | T |
| 46 | PB10B | 4 | | C | PB13B | 4 | | C |
| 47 | NC | - | NC | | NC | - | NC | |
| 48 | PB11A | 4 | | T | PB16A | 4 | | T |
| 49 | PB11B | 4 | | C | PB16B | 4 | | C |
| 50** | GNDIO3 GNDIO4 | - | | | GNDIO3 GNDIO4 | - | | |
| 51 | PR16B | 3 | | | PR19B | 3 | | |
| 52 | PR15B | 3 | | C* | PR18B | 3 | | C* |
| 53 | PR15A | 3 | | T* | PR18A | 3 | | T* |
| 54 | PR14B | 3 | | C* | PR17B | 3 | | C* |
| 55 | PR14A | 3 | | T* | PR17A | 3 | | T* |
| 56 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| 57 | PR12B | 3 | | C* | PR15B | 3 | | C* |
| 58 | PR12A | 3 | | T* | PR15A | 3 | | T* |
| 59 | GND | - | | | GND | - | | |
| 60 | PR10B | 3 | | C* | PR13B | 3 | | C* |
| 61 | PR10A | 3 | | T* | PR13A | 3 | | T* |
| 62 | PR9B | 3 | | C* | PR11B | 3 | | C* |
| 63 | PR9A | 3 | | T* | PR11A | 3 | | T* |
| 64 | PR8B | 2 | | C* | PR10B | 2 | | C* |
| 65 | PR8A | 2 | | T* | PR10A | 2 | | T* |
| 66 | VCC | - | | | VCC | - | | |
| 67 | PR6C | 2 | | | PR8C | 2 | | |
| 68 | PR6B | 2 | | C* | PR8B | 2 | | C* |
| 69 | PR6A | 2 | | T* | PR8A | 2 | | T* |
| 70 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| 71 | PR4D | 2 | | | PR5D | 2 | | |
| 72 | PR4B | 2 | | C* | PR5B | 2 | | C* |
| 73 | PR4A | 2 | | T* | PR5A | 2 | | T* |
| 74 | PR2B | 2 | | C | PR3B | 2 | | C* |
| 75 | PR2A | 2 | | T | PR3A | 2 | | T* |
| 76** | GNDIO1 GNDIO2 | - | | | GNDIO1 GNDIO2 | - | | |
| 77 | PT11C | 1 | | | PT15C | 1 | | |
| 78 | PT11B | 1 | | C | PT14B | 1 | | C |
| 79 | PT11A | 1 | | T | PT14A | 1 | | T |

# LA-MachXO640, LA-MachXO1200 and LA-MachXO2280 Logic Signal Connections: 256 ftBGA (Cont.)

| LAMXO640 | | | | | LAMXO1200 | | | | | LAMXO2280 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball Function | Bank | Dual Function | Differential | Ball Number | Ball Function | Bank | Dual Function | Differential | Ball Number | Ball Function | Bank | Dual Function | Differential |
| J4 | PL8A | 3 | | T | J4 | PL13A | 6 | | T** | J4 | PL16A | 6 | | T** |
| J5 | PL8B | 3 | | C | J5 | PL13B | 6 | | C** | J5 | PL16B | 6 | | C** |
| R1 | PL11A | 3 | | T | R1 | PL13C | 6 | | T | R1 | PL16C | 6 | | T |
| R2 | PL11B | 3 | | C | R2 | PL13D | 6 | | C | R2 | PL16D | 6 | | C |
| - | - | - | | | - | - | - | | | GND | GND | - | | |
| K5 | NC | | | | K5 | PL14A | 6 | LLM0_PLLT_FB_A | T** | K5 | PL17A | 6 | LLM0_PLLT_FB_A | T** |
| K4 | NC | | | | K4 | PL14B | 6 | LLM0_PLLC_FB_A | C** | K4 | PL17B | 6 | LLM0_PLLC_FB_A | C** |
| L5 | PL10C | 3 | | T | L5 | PL14C | 6 | | T | L5 | PL17C | 6 | | T |
| L4 | PL10D | 3 | | C | L4 | PL14D | 6 | | C | L4 | PL17D | 6 | | C |
| M5 | NC | | | | M5 | PL15A | 6 | LLM0_PLLT_IN_A | T** | M5 | PL18A | 6 | LLM0_PLLT_IN_A | T** |
| M4 | NC | | | | M4 | PL15B | 6 | LLM0_PLLC_IN_A | C** | M4 | PL18B | 6 | LLM0_PLLC_IN_A | C** |
| N4 | PL11C | 3 | | T | N4 | PL16A | 6 | | T | N4 | PL19A | 6 | | T |
| N3 | PL11D | 3 | | C | N3 | PL16B | 6 | | C | N3 | PL19B | 6 | | C |
| VCCIO3 | VCCIO3 | 3 | | | VCCIO6 | VCCIO6 | 6 | | | VCCIO6 | VCCIO6 | 6 | | |
| GND | GNDIO3 | 3 | | | GND | GNDIO6 | 6 | | | GND | GNDIO6 | 6 | | |
| GND | GNDIO2 | 2 | | | GND | GNDIO5 | 5 | | | GND | GNDIO5 | 5 | | |
| VCCIO2 | VCCIO2 | 2 | | | VCCIO5 | VCCIO5 | 5 | | | VCCIO5 | VCCIO5 | 5 | | |
| P4 | TMS | 2 | TMS | | P4 | TMS | 5 | TMS | | P4 | TMS | 5 | TMS | |
| P2 | NC | | | | P2 | PB2A | 5 | | T | P2 | PB2A | 5 | | T |
| P3 | NC | | | | P3 | PB2B | 5 | | C | P3 | PB2B | 5 | | C |
| N5 | NC | | | | N5 | PB2C | 5 | | T | N5 | PB2C | 5 | | T |
| R3 | TCK | 2 | TCK | | R3 | TCK | 5 | TCK | | R3 | TCK | 5 | TCK | |
| N6 | NC | | | | N6 | PB2D | 5 | | C | N6 | PB2D | 5 | | C |
| T2 | PB2A | 2 | | T | T2 | PB3A | 5 | | T | T2 | PB3A | 5 | | T |
| T3 | PB2B | 2 | | C | T3 | PB3B | 5 | | C | T3 | PB3B | 5 | | C |
| R4 | PB2C | 2 | | T | R4 | PB3C | 5 | | T | R4 | PB3C | 5 | | T |
| R5 | PB2D | 2 | | C | R5 | PB3D | 5 | | C | R5 | PB3D | 5 | | C |
| P5 | PB3A | 2 | | T | P5 | PB4A | 5 | | T | P5 | PB4A | 5 | | T |
| P6 | PB3B | 2 | | C | P6 | PB4B | 5 | | C | P6 | PB4B | 5 | | C |
| T5 | PB3C | 2 | | T | T5 | PB4C | 5 | | T | T5 | PB4C | 5 | | T |
| M6 | TDO | 2 | TDO | | M6 | TDO | 5 | TDO | | M6 | TDO | 5 | TDO | |
| T4 | PB3D | 2 | | C | T4 | PB4D | 5 | | C | T4 | PB4D | 5 | | C |
| R6 | PB4A | 2 | | T | R6 | PB5A | 5 | | T | R6 | PB5A | 5 | | T |
| GND | GNDIO2 | 2 | | | GND | GNDIO5 | 5 | | | GND | GNDIO5 | 5 | | |
| VCCIO2 | VCCIO2 | 2 | | | VCCIO5 | VCCIO5 | 5 | | | VCCIO5 | VCCIO5 | 5 | | |
| T6 | PB4B | 2 | | C | T6 | PB5B | 5 | | C | T6 | PB5B | 5 | | C |
| N7 | TDI | 2 | TDI | | N7 | TDI | 5 | TDI | | N7 | TDI | 5 | TDI | |
| T8 | PB4C | 2 | | T | T8 | PB5C | 5 | | T | T8 | PB6A | 5 | | T |
| T7 | PB4D | 2 | | C | T7 | PB5D | 5 | | C | T7 | PB6B | 5 | | C |
| M7 | NC | | | | M7 | PB6A | 5 | | T | M7 | PB7C | 5 | | T |
| M8 | NC | | | | M8 | PB6B | 5 | | C | M8 | PB7D | 5 | | C |
| T9 | VCCAUX | - | | | T9 | VCCAUX | - | | | T9 | VCCAUX | - | | |
| R7 | PB4E | 2 | | T | R7 | PB6C | 5 | | T | R7 | PB8C | 5 | | T |
| R8 | PB4F | 2 | | C | R8 | PB6D | 5 | | C | R8 | PB8D | 5 | | C |
| - | - | | | | VCCIO5 | VCCIO5 | 5 | | | VCCIO5 | VCCIO5 | 5 | | |
| - | - | | | | GND | GNDIO5 | 5 | | | GND | GNDIO5 | 5 | | |
| P7 | PB5C | 2 | | T | P7 | PB6E | 5 | | T | P7 | PB9A | 4 | | T |
| P8 | PB5D | 2 | | C | P8 | PB6F | 5 | | C | P8 | PB9B | 4 | | C |
| N8 | PB5A | 2 | | T | N8 | PB7A | 4 | | T | N8 | PB10E | 4 | | T |
| N9 | PB5B | 2 | PCLK2_1**** | C | N9 | PB7B | 4 | PCLK4_1**** | C | N9 | PB10F | 4 | PCLK4_1**** | C |
| P10 | PB7B | 2 | | C | P10 | PB7D | 4 | | C | P10 | PB10D | 4 | | C |
| P9 | PB7A | 2 | | T | P9 | PB7C | 4 | | T | P9 | PB10C | 4 | | T |
| M9 | PB6B | 2 | PCLK2_0**** | C | M9 | PB7F | 4 | PCLK4_0**** | C | M9 | PB10B | 4 | PCLK4_0**** | C |

## LA-MachXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

| LAMXO2280 | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball Function** | **Bank** | **Dual Function** | **Differential** |
| V10 | PB9B | 4 | | C |
| N10 | PB9C | 4 | | T |
| R10 | PB9D | 4 | | C |
| P10 | PB10F | 4 | PCLK4_1** | C |
| T10 | PB10E | 4 | | T |
| U10 | PB10D | 4 | | C |
| V11 | PB10C | 4 | | T |
| U11 | PB10B | 4 | PCLK4_0** | C |
| VCCIO4 | VCCIO4 | 4 | | |
| GND | GNDIO4 | 4 | | |
| T11 | PB10A | 4 | | T |
| U12 | PB11A | 4 | | T |
| R11 | PB11B | 4 | | C |
| GND | GND | - | | |
| T12 | PB11C | 4 | | T |
| P11 | PB11D | 4 | | C |
| V12 | PB12A | 4 | | T |
| V13 | PB12B | 4 | | C |
| R12 | PB12C | 4 | | T |
| N11 | PB12D | 4 | | C |
| U13 | PB12E | 4 | | T |
| VCCIO4 | VCCIO4 | 4 | | |
| GND | GNDIO4 | 4 | | |
| V14 | PB12F | 4 | | C |
| T13 | PB13A | 4 | | T |
| P12 | PB13B | 4 | | C |
| R13 | PB13C | 4 | | T |
| N12 | PB13D | 4 | | C |
| V15 | PB14A | 4 | | T |
| U14 | PB14B | 4 | | C |
| V16 | PB14C | 4 | | T |
| GND | GND | - | | |
| T14 | PB14D | 4 | | C |
| U15 | PB15A | 4 | | T |
| V17 | PB15B | 4 | | C |
| P13 | NC | - | | |
| T15 | PB15D | 4 | | |
| U16 | PB16A | 4 | | T |
| V18 | PB16B | 4 | | C |
| N13 | PB16C | 4 | | T |
| R14 | PB16D | 4 | | C |
| VCCIO4 | VCCIO4 | 4 | | |
| GND | GNDIO4 | 4 | | |

## LA-MachXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

| LAMXO2280 | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball Function** | **Bank** | **Dual Function** | **Differential** |
| G8 | VCCIO0 | 0 | | |
| G7 | VCCIO0 | 0 | | |

* Supports true LVDS outputs.
** Primary clock inputs are single-ended.

# LA-MachXO Automotive Family Data Sheet Supplemental Information

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## For Further Information

A variety of technical notes for the LA-MachXO family are available on the Lattice web site at www.latticesemi.com.

- MachXO sysIO Usage Guide (TN1091)
- MachXO sysCLOCK PLL Design and Usage Guide (TN1089)
- MachXO Memory Usage Guide (TN1092)
- Power Estimation and Management for MachXO Devices (TN1090)
- MachXO JTAG Programming and Configuration User's Guide (TN1086)
- Minimizing System Interruption During Configuration Using TransFR Technology (TN1087)
- MachXO Density Migration (TN1097)
- IEEE 1149.1 Boundary Scan Testability in Lattice Devices

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS): www.jedec.org
- PCI: www.pcisig.com