Lattice Semiconductor Corporation - LAMXO256E-3TN100E Datasheet

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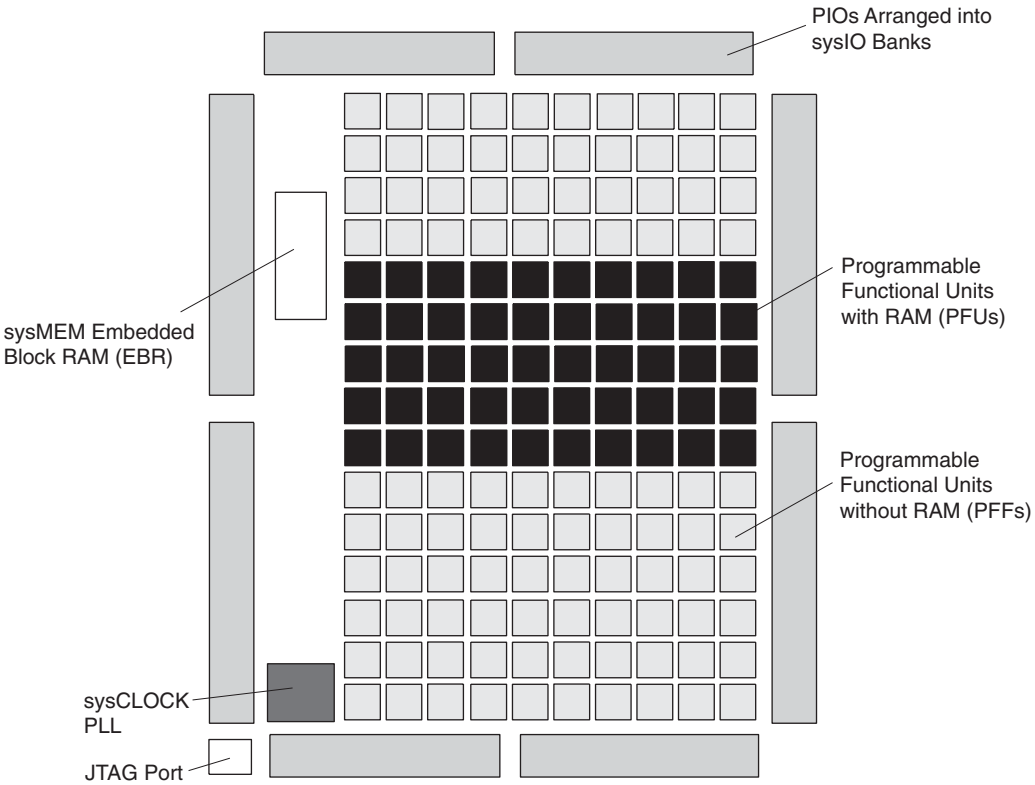
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

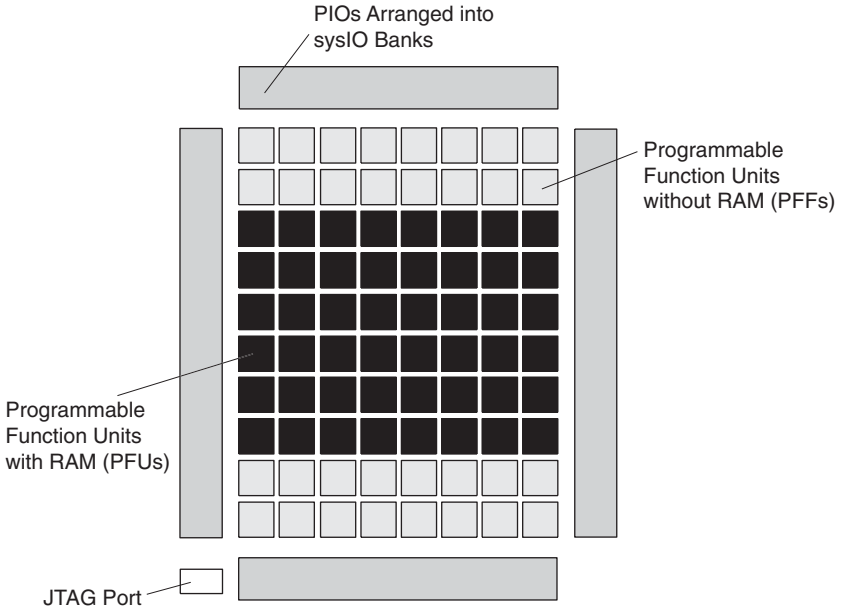
Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	4.9 ns
Voltage Supply - Internal	1.14V ~ 1.26V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	78
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lamxo256e-3tn100e

Figure 2-1. Top View of the LA-MachXO1200 Device[1]



1. Top view of the LA-MachXO2280 device is similar but with higher LUT count, two PLLs, and three EBR blocks.

Figure 2-2. Top View of the LA-MachXO640 Device



Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM, and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SP 16x2	ROM 16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM 16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables (LUT4). A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7, and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two additional signals, Carry Generate and Carry Propagate, are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x2-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

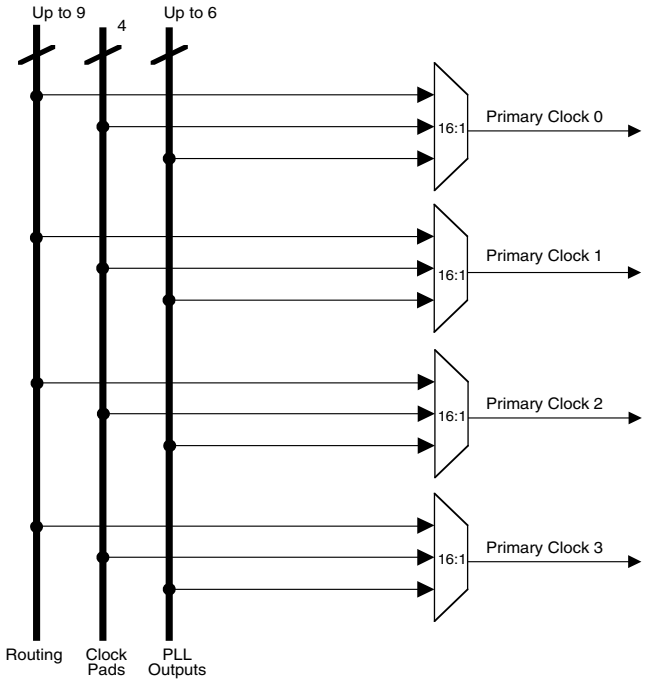
The ispLEVER design tool supports the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-6 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices. One Slice functions as the read-write port, while the other companion Slice supports the read-only port. For more information on RAM mode in LA-MachXO devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of Slices	1	2

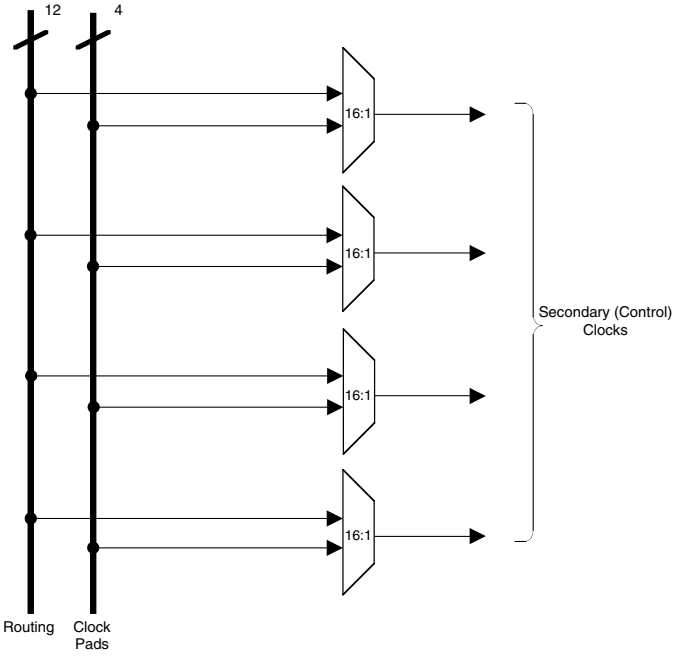
Note: SPR = Single Port RAM, DPR = Dual Port RAM

Figure 2-8. Primary Clocks for LA-MachXO1200 and LA-MachXO2280 Devices



Four secondary clocks are generated from four 16:1 muxes as shown in Figure 2-9. Four of the secondary clock sources come from dual function clock pins and 12 come from internal routing.

Figure 2-9. Secondary Clocks for LA-MachXO Devices

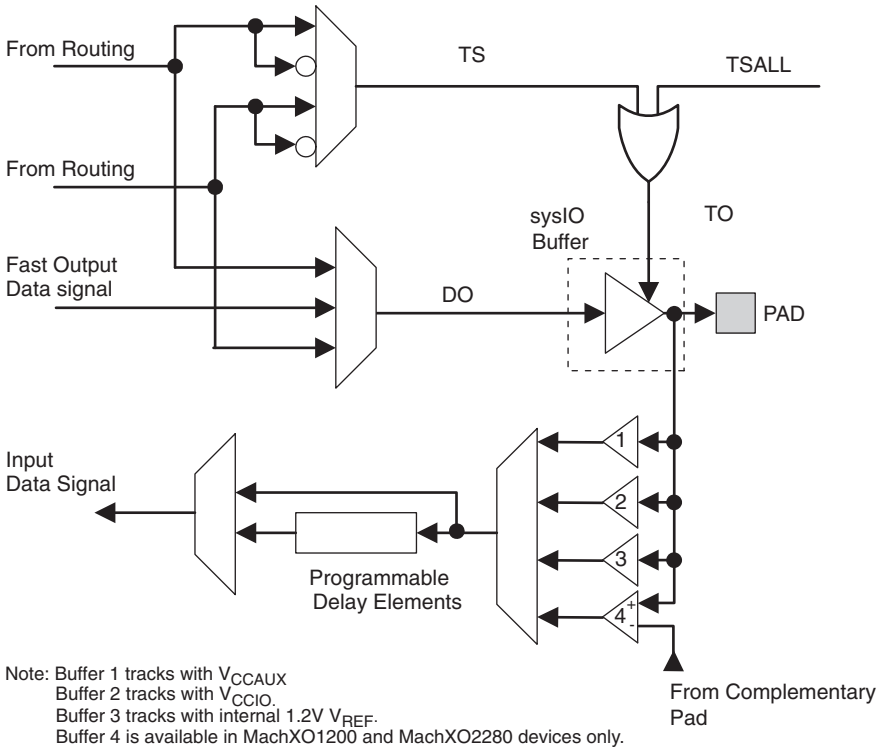


output data signals are multiplexed and provide a single signal to the I/O pin via the sysIO buffer. Figure 2-17 shows the LA-MachXO PIO logic.

The tristate control signal is multiplexed from the output data signals and their complements. In addition a global signal (TSALL) from a dedicated pad can be used to tristate the sysIO buffer.

The PIO receives an input signal from the pin via the sysIO buffer and provides this signal to the core of the device. In addition there are programmable elements that can be utilized by the design tools to avoid positive hold times.

Figure 2-17. LA-MachXO PIO Block Diagram



sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as Banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, TTL, BLVDS, LVDS and LVPECL.

In the LA-MachXO devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO}. In addition to the Bank V_{CCIO} supplies, the LA-MachXO devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that powers up a variety of internal circuits including all the differential and referenced input buffers.

LA-MachXO256 and LA-MachXO640 devices contain single-ended input buffers and single-ended output buffers with complementary outputs on all the I/O Banks.

LA-MachXO1200 and LA-MachXO2280 devices contain two types of sysIO buffer pairs.

1. **Top and Bottom sysIO Buffer Pairs**
   The sysIO buffer pairs in the top and bottom Banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (for ratioed or absolute input levels). The I/O pairs on the top and bottom

Programming and Erase Flash Supply Current[1, 2, 3, 4]

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply	LCMXO256C	9	mA
		LCMXO640C	11	mA
		LCMXO256E	6	mA
		LCMXO640E	8	mA
		LCMXO1200E	12	mA
		LCMXO2280E	14	mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3V	LCMXO256E/C	8	mA
		LCMXO640E/C	10	mA
		LCMXO1200E	15	mA
		LCMXO2280E	16	mA
I_{CCIO}	Bank Power Supply[6]	All devices	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all I/O pins are held at V_{CCIO} or GND.
3. Typical user pattern.
4. JTAG programming is at 25MHz.
5. T_J = 25°C, power supplies at nominal voltage.
6. Per Bank. V_{CCIO} = 2.5V. Does not include pull-up/pull-down.

sysIO Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-14, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	2.4	16	-16
					0.4	V_{CCIO} - 0.4	12, 8, 4	-12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-14, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-14, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2 (“C” Version)	-0.3	0.42	0.78	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2 (“E” Version)	-0.3	$0.35V_{CC}$	$0.65V_{CC}$	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O Bank and the end of an I/O Bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between Bank GND connections or between the last GND in a Bank and the end of a Bank.

LA-MachXO Family Timing Adders[1, 2, 3]

Over Recommended Operating Conditions

Buffer Type	Description	-3	Units
Input Adjusters			
LVDS25[4]	LVDS	0.61	ns
BLVDS25[4]	BLVDS	0.61	ns
LVPECL33[4]	LVPECL	0.59	ns
LVTTL33	LVTTL	0.01	ns
LVCMOS33	LVCMOS 3.3	0.01	ns
LVCMOS25	LVCMOS 2.5	0.00	ns
LVCMOS18	LVCMOS 1.8	0.10	ns
LVCMOS15	LVCMOS 1.5	0.19	ns
LVCMOS12	LVCMOS 1.2	0.56	ns
PCI33[4]	PCI	0.01	ns
Output Adjusters			
LVDS25E	LVDS 2.5 E	-0.18	ns
LVDS25[4]	LVDS 2.5	-0.30	ns
BLVDS25	BLVDS 2.5	-0.04	ns
LVPECL33	LVPECL 3.3	0.05	ns
LVTTL33_4mA	LVTTL 4mA drive	0.05	ns
LVTTL33_8mA	LVTTL 8mA drive	0.08	ns
LVTTL33_12mA	LVTTL 12mA drive	-0.01	ns
LVTTL33_16mA	LVTTL 16mA drive	0.70	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive	0.05	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive	0.08	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive	-0.01	ns
LVCMOS33_14mA	LVCMOS 3.3 14mA drive	0.70	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive	0.07	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive	0.13	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive	0.00	ns
LVCMOS25_14mA	LVCMOS 2.5 14mA drive	0.47	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive	0.15	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive	0.06	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive	-0.08	ns
LVCMOS18_14mA	LVCMOS 1.8 14mA drive	0.09	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive	0.22	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive	0.07	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive	0.36	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive	0.07	ns
PCI33[4]	PCI33	2.59	ns

1. Timing adders are characterized but not tested on every device.
2. LVCMOS timing is measured with the load specified in Switching Test Conditions table.
3. All other standards tested according to the appropriate specifications.
4. I/O standard only available in LCMXO1200 and LCMXO2280 devices.

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sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		25	420	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		25	420	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)		0.195	210	MHz
f_{VCO}	PLL VCO Frequency		420	840	MHz
f_{PFD}	Phase Detector Input Frequency		25	—	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected[3]	45	55	%
t_{PH}[4]	Output Phase Accuracy		—	0.05	UI
t_{OPJIT}[1]	Output Clock Period Jitter	Fout ≥ 100MHz	—	+/-120	ps
		Fout < 100MHz	—	0.02	UIPP
t_{SK}	Input Clock to Output Clock Skew	Divider ratio = integer	—	+/-200	ps
t_W	Output Clock Pulse Width	At 90% or 10%[3]	1	—	ns
t_{LOCK}[2]	PLL Lock-in Time		—	150	µs
t_{PA}	Programmable Delay Unit		100	450	ps
t_{IPJIT}	Input Clock Period Jitter		—	+/-200	ps
t_{FBKDLY}	External Feedback Delay		—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{RST}	RST Pulse Width		10	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output.

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LA-MachXO "C" Sleep Mode Timing

Symbol	Parameter	Device	Min.	Typ.	Max	Units
t_{PWRDN}	SLEEPN Low to Power Down	All	—	—	400	ns
t_{PWRUP}	SLEEPN High to Power Up	LCMXO256	—	—	400	µs
		LCMXO640	—	—	600	µs
$t_{WSLEEPN}$	SLEEPN Pulse Width	All	400	—	—	ns
t_{WAWAKE}	SLEEPN Pulse Rejection	All	—	—	100	ns

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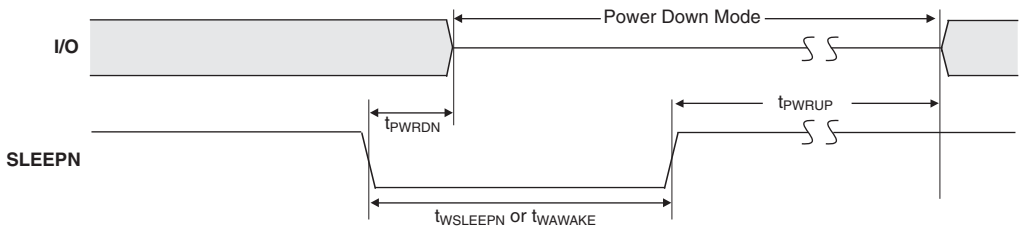

Flash Download Time

Symbol	Parameter		Min.	Typ.	Max.	Units
$t_{REFRESH}$	Minimum V_{CC} or V_{CCAUX} (later of the two supplies) to Device I/O Active	LCMXO256	—	—	0.4	ms
		LCMXO640	—	—	0.6	ms
		LCMXO1200	—	—	0.8	ms
		LCMXO2280	—	—	1.0	ms

JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	TCK [BSCAN] clock frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to output valid	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to output disabled	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to output enabled	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to output valid	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to output disabled	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to output enabled	—	25	ns

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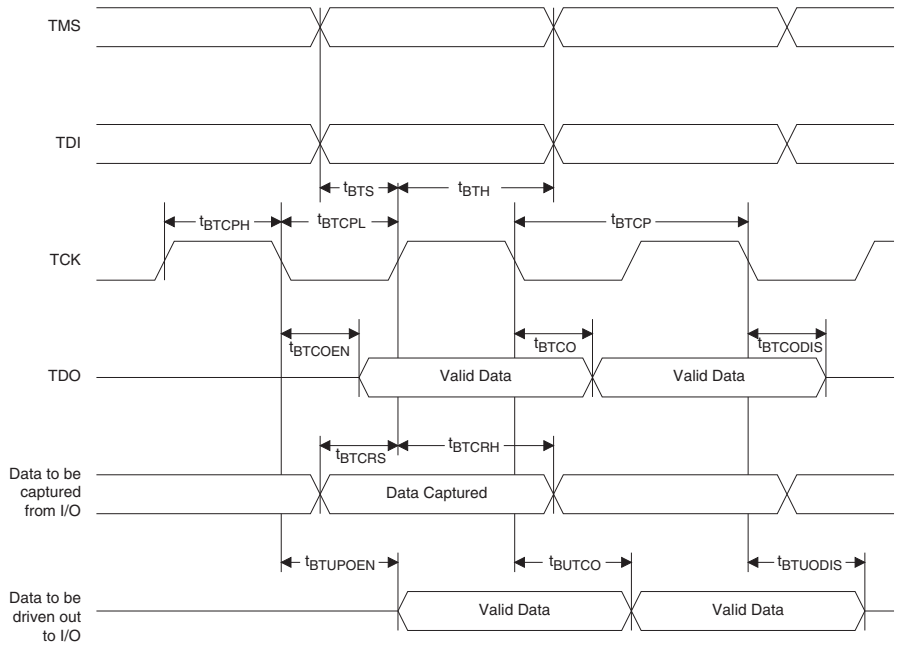
Figure 3-5. JTAG Port Timing Waveforms



Power Supply and NC

Signal	100 TQFP[1]	144 TQFP[1]
VCC	**LAMXO256/640**: 35, 90 **LAMXO1200/2280**: 17, 35, 66, 91	21, 52, 93, 129
VCCIO0	**LAMXO256**: 60, 74, 92 **LAMXO640**: 80, 92 **LAMXO1200/2280**: 94	**LAMXO640**: 117, 135 **LAMXO1200/2280**: 135
VCCIO1	**LAMXO256**: 10, 24, 41 **LAMXO640**: 60, 74 **LAMXO1200/2280**: 80	**LAMXO640**: 82, 98 **LAMXO1200/2280**: 117
VCCIO2	**LAMXO256**: None **LAMXO640**: 29, 41 **LAMXO1200/2280**: 70	**LAMXO640**: 38, 63 **LAMXO1200/2280**: 98
VCCIO3	**LAMXO256**: None **LAMXO640**: 10, 24 **LAMXO1200/2280**: 56	**LAMXO640**: 10, 26 **LAMXO1200/2280**: 82
VCCIO4	**LAMXO256/640**: None **LAMXO1200/2280**: 44	**LAMXO640**: None **LAMXO1200/2280**: 63
VCCIO5	**LAMXO256/640**: None **LAMXO1200/2280**: 27	**LAMXO640**: None **LAMXO1200/2280**: 38
VCCIO6	**LAMXO256/640**: None **LAMXO1200/2280**: 20	**LAMXO640**: None **LAMXO1200/2280**: 26
VCCIO7	**LAMXO256/640**: None **LAMXO1200/2280**: 6	**LAMXO640**: None **LAMXO1200/2280**: 10
VCCAUX	**LAMXO256/640**: 88 **LAMXO1200/2280**: 36, 90	53, 128
GND[2]	**LAMXO256**: 40, 84, 62, 75, 93, 12, 25, 42 **LAMXO640**: 40, 84, 81, 93, 62, 75, 30, 42, 12, 25 **LAMXO1200/2280**: 9, 41, 59, 83, 100, 76, 50, 26	16, 59, 88, 123, 118, 136, 83, 99, 37, 64, 11, 27
NC[3]		

1. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
2. All grounds must be electrically connected at the board level. For fpBGA and ftBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
3. NC pins should not be connected to any active signals, VCC or GND.

Power Supply and NC (Cont.)

Signal	256 ftBGA[1]	324 ftBGA[1]
VCC	G7, G10, K7, K10	F14, G11, G9, H7, L7, M9
VCCIO0	**LAMXO640**: F8, F7, F9, F10 **LAMXO1200/2280**: F8, F7	G8, G7
VCCIO1	**LAMXO640**: H11, G11, K11, J11 **LAMXO1200/2280**: F9, F10	G12, G10
VCCIO2	**LAMXO640**: L9, L10, L8, L7 **LAMXO1200/2280**: H11, G11	J12, H12
VCCIO3	**LAMXO640**: K6, J6, H6, G6 **LAMXO1200/2280**: K11, J11	L12, K12
VCCIO4	**LAMXO640**: None **LAMXO1200/2280**: L9, L10	M12, M11
VCCIO5	**LAMXO640**: None **LAMXO1200/2280**: L8, L7	M8, R9
VCCIO6	**LAMXO640**: None **LAMXO1200/2280**: K6, J6	M7, K7
VCCIO7	**LAMXO640**: None **LAMXO1200/2280**: H6, G6	H6, J7
VCCAUX	T9, A8	M10, F9
GND[2]	A1, A16, F11, G8, G9, H7, H8, H9, H10, J7, J8, J9, J10, K8, K9, L6, T1, T16	E14, F16, H10, H11, H8, H9, J10, J11, J4, J8, J9, K10, K11, K17, K8, K9, L10, L11, L8, L9, N2, P14, P5, R7
NC[3]	**LAMXO640**: E4, E5, F5, F6, C3, C2, G4, G5, H4, H5, K5, K4, M5, M4, P2, P3, N5, N6, M7, M8, N10, N11, R15, R16, P15, P16, M11, L11, N12, N13, M13, M12, K12, J12, F12, F13, E12, E13, D13, D14, B15, A15, C14, B14, E11, E10, E7, E6, D4, D3, B3, B2 **LAMXO1200**: None **LAMXO2280**: None	—

1. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
2. All grounds must be electrically connected at the board level. For fpBGA and ftBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
3. NC pins should not be connected to any active signals, VCC or GND.

LA-MachXO256 and LA-MachXO640 Logic Signal Connections: 100 TQFP

	LAMXO256				LAMXO640			
Pin Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
1	PL2A	1		T	PL2A	3		T
2	PL2B	1		C	PL2C	3		T
3	PL3A	1		T	PL2B	3		C
4	PL3B	1		C	PL2D	3		C
5	PL3C	1		T	PL3A	3		T
6	PL3D	1		C	PL3B	3		C
7	PL4A	1		T	PL3C	3		T
8	PL4B	1		C	PL3D	3		C
9	PL5A	1		T	PL4A	3		
10	VCCIO1	1			VCCIO3	3		
11	PL5B	1		C	PL4C	3		T
12	GNDIO1	1			GNDIO3	3		
13	PL5C	1		T	PL4D	3		C
14	PL5D	1	GSRN	C	PL5B	3	GSRN	
15	PL6A	1		T	PL7B	3		
16	PL6B	1	TSALL	C	PL8C	3	TSALL	T
17	PL7A	1		T	PL8D	3		C
18	PL7B	1		C	PL9A	3		
19	PL7C	1		T	PL9C	3		
20	PL7D	1		C	PL10A	3		
21	PL8A	1		T	PL10C	3		
22	PL8B	1		C	PL11A	3		
23	PL9A	1		T	PL11C	3		
24	VCCIO1	1			VCCIO3	3		
25	GNDIO1	1			GNDIO3	3		
26	TMS	1	TMS		TMS	2	TMS	
27	PL9B	1		C	PB2C	2		
28	TCK	1	TCK		TCK	2	TCK	
29	PB2A	1		T	VCCIO2	2		
30	PB2B	1		C	GNDIO2	2		
31	TDO	1	TDO		TDO	2	TDO	
32	PB2C	1		T	PB4C	2		
33	TDI	1	TDI		TDI	2	TDI	
34	PB2D	1		C	PB4E	2		
35	VCC	-			VCC	-		
36	PB3A	1	PCLK1_1**	T	PB5B	2	PCLK2_1**	
37	PB3B	1		C	PB5D	2		
38	PB3C	1	PCLK1_0**	T	PB6B	2	PCLK2_0**	
39	PB3D	1		C	PB6C	2		
40	GND	-			GND	-		
41	VCCIO1	1			VCCIO2	2		

LA-MachXO256 and LA-MachXO640 Logic Signal Connections: 100 TQFP (Cont.)

	LAMXO256				LAMXO640			
Pin Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
83	PT4C	0		T	PT7A	0		
84	GND	-			GND	-		
85	PT4B	0	PCLK0_1**	C	PT6B	0	PCLK0_1**	
86	PT4A	0	PCLK0_0**	T	PT5B	0	PCLK0_0**	C
87	PT3D	0		C	PT5A	0		T
88	VCCAUX	-			VCCAUX	-		
89	PT3C	0		T	PT4F	0		
90	VCC	-			VCC	-		
91	PT3B	0		C	PT3F	0		
92	VCCIO0	0			VCCIO0	0		
93	GNDIO0	0			GNDIO0	0		
94	PT3A	0		T	PT3B	0		C
95	PT2F	0		C	PT3A	0		T
96	PT2E	0		T	PT2F	0		C
97	PT2D	0		C	PT2E	0		T
98	PT2C	0		T	PT2B	0		C
99	PT2B	0		C	PT2C	0		
100	PT2A	0		T	PT2A	0		T

* NC for “E” devices.
** Primary clock inputs are single-ended.

LA-MachXO640, LA-MachXO1200 and LA-MachXO2280 Logic Signal Connections: 144 TQFP

Pin Number	LAMXO640				LAMXO1200				LAMXO2280			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
1	PL2A	3		T	PL2A	7		T	PL2A	7	LUM0_PLLT_FB_A	T
2	PL2C	3		T	PL2B	7		C	PL2B	7	LUM0_PLLC_FB_A	C
3	PL2B	3		C	PL3A	7		T*	PL3A	7		T*
4	PL3A	3		T	PL3B	7		C*	PL3B	7		C*
5	PL2D	3		C	PL3C	7		T	PL3C	7	LUM0_PLLT_IN_A	T
6	PL3B	3		C	PL3D	7		C	PL3D	7	LUM0_PLLC_IN_A	C
7	PL3C	3		T	PL4A	7		T*	PL4A	7		T*
8	PL3D	3		C	PL4B	7		C*	PL4B	7		C*
9	PL4A	3			PL4C	7			PL4C	7		
10	VCCIO3	3			VCCIO7	7			VCCIO7	7		
11	GNDIO3	3			GNDIO7	7			GNDIO7	7		
12	PL4D	3			PL5C	7			PL6C	7		
13	PL5A	3		T	PL6A	7		T*	PL7A	7		T*
14	PL5B	3	GSRN	C	PL6B	7	GSRN	C*	PL7B	7	GSRN	C*
15	PL5D	3			PL6D	7			PL7D	7		
16	GND	-			GND	-			GND	-		
17	PL6C	3		T	PL7C	7		T	PL9C	7		T
18	PL6D	3		C	PL7D	7		C	PL9D	7		C
19	PL7A	3		T	PL10A	6		T*	PL13A	6		T*
20	PL7B	3		C	PL10B	6		C*	PL13B	6		C*
21	VCC	-			VCC	-			VCC	-		
22	PL8A	3		T	PL11A	6		T*	PL13D	6		
23	PL8B	3		C	PL11B	6		C*	PL14D	6		C
24	PL8C	3	TSALL		PL11C	6	TSALL		PL14C	6	TSALL	T
25	PL9C	3		T	PL12B	6			PL15B	6		
26	VCCIO3	3			VCCIO6	6			VCCIO6	6		
27	GNDIO3	3			GNDIO6	6			GNDIO6	6		
28	PL9D	3		C	PL13D	6			PL16D	6		
29	PL10A	3		T	PL14A	6	LLM0_PLLT_FB_A	T*	PL17A	6	LLM0_PLLT_FB_A	T*
30	PL10B	3		C	PL14B	6	LLM0_PLLC_FB_A	C*	PL17B	6	LLM0_PLLC_FB_A	C*
31	PL10C	3		T	PL14C	6		T	PL17C	6		T
32	PL11A	3		T	PL14D	6		C	PL17D	6		C
33	PL10D	3		C	PL15A	6	LLM0_PLLT_IN_A	T*	PL18A	6	LLM0_PLLT_IN_A	T*
34	PL11C	3		T	PL15B	6	LLM0_PLLC_IN_A	C*	PL18B	6	LLM0_PLLC_IN_A	C*
35	PL11B	3		C	PL16A	6		T	PL19A	6		T
36	PL11D	3		C	PL16B	6		C	PL19B	6		C
37	GNDIO2	2			GNDIO5	5			GNDIO5	5		
38	VCCIO2	2			VCCIO5	5			VCCIO5	5		
39	TMS	2	TMS		TMS	5	TMS		TMS	5	TMS	
40	PB2C	2			PB2C	5		T	PB2A	5		T
41	PB3A	2		T	PB2D	5		C	PB2B	5		C
42	TCK	2	TCK		TCK	5	TCK		TCK	5	TCK	
43	PB3B	2		C	PB3A	5		T	PB3A	5		T
44	PB3C	2		T	PB3B	5		C	PB3B	5		C
45	PB3D	2		C	PB4A	5		T	PB4A	5		T
46	PB4A	2		T	PB4B	5		C	PB4B	5		C
47	TDO	2	TDO		TDO	5	TDO		TDO	5	TDO	
48	PB4B	2		C	PB4D	5			PB4D	5		
49	PB4C	2		T	PB5A	5		T	PB5A	5		T
50	PB4D	2		C	PB5B	5		C	PB5B	5		C

LA-MachXO640, LA-MachXO1200 and LA-MachXO2280 Logic Signal Connections: 256 ftBGA

LAMXO640					LAMXO1200					LAMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO3	3			GND	GNDIO7	7			GND	GNDIO7	7		
VCCIO3	VCCIO3	3			VCCIO7	VCCIO7	7			VCCIO7	VCCIO7	7		
E4	NC				E4	PL2A	7		T	E4	PL2A	7	LUM0_PLLT_FB_A	T
E5	NC				E5	PL2B	7		C	E5	PL2B	7	LUM0_PLLC_FB_A	C
F5	NC				F5	PL3A	7		T**	F5	PL3A	7		T**
F6	NC				F6	PL3B	7		C**	F6	PL3B	7		C**
F3	PL3A	3		T	F3	PL3C	7		T	F3	PL3C	7	LUM0_PLLT_IN_A	T
F4	PL3B	3		C	F4	PL3D	7		C	F4	PL3D	7	LUM0_PLLC_IN_A	C
E3	PL2C	3		T	E3	PL4A	7		T**	E3	PL4A	7		T**
E2	PL2D	3		C	E2	PL4B	7		C**	E2	PL4B	7		C**
C3	NC				C3	PL4C	7		T	C3	PL4C	7		T
C2	NC				C2	PL4D	7		C	C2	PL4D	7		C
B1	PL2A	3		T	B1	PL5A	7		T**	B1	PL5A	7		T**
C1	PL2B	3		C	C1	PL5B	7		C**	C1	PL5B	7		C**
VCCIO3	VCCIO3	3			VCCIO7	VCCIO7	7			VCCIO7	VCCIO7	7		
GND	GNDIO3	3			GND	GNDIO7	7			GND	GNDIO7	7		
D2	PL3C	3		T	D2	PL5C	7		T	D2	PL6C	7		T
D1	PL3D	3		C	D1	PL5D	7		C	D1	PL6D	7		C
F2	PL5A	3		T	F2	PL6A	7		T**	F2	PL7A	7		T**
G2	PL5B	3	GSRN	C	G2	PL6B	7	GSRN	C**	G2	PL7B	7	GSRN	C**
E1	PL4A	3		T	E1	PL6C	7		T	E1	PL7C	7		T
F1	PL4B	3		C	F1	PL6D	7		C	F1	PL7D	7		C
G4	NC				G4	PL7A	7		T**	G4	PL8A	7		T**
G5	NC				G5	PL7B	7		C**	G5	PL8B	7		C**
GND	GND	-			GND	GND	-			GND	GND	-		
G3	PL4C	3		T	G3	PL7C	7		T	G3	PL8C	7		T
H3	PL4D	3		C	H3	PL7D	7		C	H3	PL8D	7		C
H4	NC				H4	PL8A	7		T**	H4	PL9A	7		T**
H5	NC				H5	PL8B	7		C**	H5	PL9B	7		C**
-	-				VCCIO7	VCCIO7	7			VCCIO7	VCCIO7	7		
-	-				GND	GNDIO7	7			GND	GNDIO7	7		
G1	PL5C	3		T	G1	PL8C	7		T	G1	PL10C	7		T
H1	PL5D	3		C	H1	PL8D	7		C	H1	PL10D	7		C
H2	PL6A	3		T	H2	PL9A	6		T**	H2	PL11A	6		T**
J2	PL6B	3		C	J2	PL9B	6		C**	J2	PL11B	6		C**
J3	PL7C	3		T	J3	PL9C	6		T	J3	PL11C	6		T
K3	PL7D	3		C	K3	PL9D	6		C	K3	PL11D	6		C
J1	PL6C	3		T	J1	PL10A	6		T**	J1	PL12A	6		T**
-	-				VCCIO6	VCCIO6	6			VCCIO6	VCCIO6	6		
-	-				GND	GNDIO6	6			GND	GNDIO6	6		
K1	PL6D	3		C	K1	PL10B	6		C**	K1	PL12B	6		C**
K2	PL9A	3		T	K2	PL10C	6		T	K2	PL12C	6		T
L2	PL9B	3		C	L2	PL10D	6		C	L2	PL12D	6		C
L1	PL7A	3		T	L1	PL11A	6		T**	L1	PL13A	6		T**
M1	PL7B	3		C	M1	PL11B	6		C**	M1	PL13B	6		C**
P1	PL8D	3		C	P1	PL11D	6		C	P1	PL14D	6		C
N1	PL8C	3	TSALL	T	N1	PL11C	6	TSALL	T	N1	PL14C	6	TSALL	T
L3	PL10A	3		T	L3	PL12A	6		T**	L3	PL15A	6		T**
M3	PL10B	3		C	M3	PL12B	6		C**	M3	PL15B	6		C**
M2	PL9C	3		T	M2	PL12C	6		T	M2	PL15C	6		T
N2	PL9D	3		C	N2	PL12D	6		C	N2	PL15D	6		C
VCCIO3	VCCIO3	3			VCCIO6	VCCIO6	6			VCCIO6	VCCIO6	6		
GND	GNDIO3	3			GND	GNDIO6	6			GND	GNDIO6	6		

LA-MachXO640, LA-MachXO1200 and LA-MachXO2280 Logic Signal Connections: 256 ftBGA (Cont.)

LAMXO640					LAMXO1200					LAMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
J4	PL8A	3		T	J4	PL13A	6		T**	J4	PL16A	6		T**
J5	PL8B	3		C	J5	PL13B	6		C**	J5	PL16B	6		C**
R1	PL11A	3		T	R1	PL13C	6		T	R1	PL16C	6		T
R2	PL11B	3		C	R2	PL13D	6		C	R2	PL16D	6		C
-	-	-			-	-	-			GND	GND	-		
K5	NC				K5	PL14A	6	LLM0_PLLT_FB_A	T**	K5	PL17A	6	LLM0_PLLT_FB_A	T**
K4	NC				K4	PL14B	6	LLM0_PLLC_FB_A	C**	K4	PL17B	6	LLM0_PLLC_FB_A	C**
L5	PL10C	3		T	L5	PL14C	6		T	L5	PL17C	6		T
L4	PL10D	3		C	L4	PL14D	6		C	L4	PL17D	6		C
M5	NC				M5	PL15A	6	LLM0_PLLT_IN_A	T**	M5	PL18A	6	LLM0_PLLT_IN_A	T**
M4	NC				M4	PL15B	6	LLM0_PLLC_IN_A	C**	M4	PL18B	6	LLM0_PLLC_IN_A	C**
N4	PL11C	3		T	N4	PL16A	6		T	N4	PL19A	6		T
N3	PL11D	3		C	N3	PL16B	6		C	N3	PL19B	6		C
VCCIO3	VCCIO3	3			VCCIO6	VCCIO6	6			VCCIO6	VCCIO6	6		
GND	GNDIO3	3			GND	GNDIO6	6			GND	GNDIO6	6		
GND	GNDIO2	2			GND	GNDIO5	5			GND	GNDIO5	5		
VCCIO2	VCCIO2	2			VCCIO5	VCCIO5	5			VCCIO5	VCCIO5	5		
P4	TMS	2	TMS		P4	TMS	5	TMS		P4	TMS	5	TMS	
P2	NC				P2	PB2A	5		T	P2	PB2A	5		T
P3	NC				P3	PB2B	5		C	P3	PB2B	5		C
N5	NC				N5	PB2C	5		T	N5	PB2C	5		T
R3	TCK	2	TCK		R3	TCK	5	TCK		R3	TCK	5	TCK	
N6	NC				N6	PB2D	5		C	N6	PB2D	5		C
T2	PB2A	2		T	T2	PB3A	5		T	T2	PB3A	5		T
T3	PB2B	2		C	T3	PB3B	5		C	T3	PB3B	5		C
R4	PB2C	2		T	R4	PB3C	5		T	R4	PB3C	5		T
R5	PB2D	2		C	R5	PB3D	5		C	R5	PB3D	5		C
P5	PB3A	2		T	P5	PB4A	5		T	P5	PB4A	5		T
P6	PB3B	2		C	P6	PB4B	5		C	P6	PB4B	5		C
T5	PB3C	2		T	T5	PB4C	5		T	T5	PB4C	5		T
M6	TDO	2	TDO		M6	TDO	5	TDO		M6	TDO	5	TDO	
T4	PB3D	2		C	T4	PB4D	5		C	T4	PB4D	5		C
R6	PB4A	2		T	R6	PB5A	5		T	R6	PB5A	5		T
GND	GNDIO2	2			GND	GNDIO5	5			GND	GNDIO5	5		
VCCIO2	VCCIO2	2			VCCIO5	VCCIO5	5			VCCIO5	VCCIO5	5		
T6	PB4B	2		C	T6	PB5B	5		C	T6	PB5B	5		C
N7	TDI	2	TDI		N7	TDI	5	TDI		N7	TDI	5	TDI	
T8	PB4C	2		T	T8	PB5C	5		T	T8	PB6A	5		T
T7	PB4D	2		C	T7	PB5D	5		C	T7	PB6B	5		C
M7	NC				M7	PB6A	5		T	M7	PB7C	5		T
M8	NC				M8	PB6B	5		C	M8	PB7D	5		C
T9	VCCAUX	-			T9	VCCAUX	-			T9	VCCAUX	-		
R7	PB4E	2		T	R7	PB6C	5		T	R7	PB8C	5		T
R8	PB4F	2		C	R8	PB6D	5		C	R8	PB8D	5		C
-	-				VCCIO5	VCCIO5	5			VCCIO5	VCCIO5	5		
-	-				GND	GNDIO5	5			GND	GNDIO5	5		
P7	PB5C	2		T	P7	PB6E	5		T	P7	PB9A	4		T
P8	PB5D	2		C	P8	PB6F	5		C	P8	PB9B	4		C
N8	PB5A	2		T	N8	PB7A	4		T	N8	PB10E	4		T
N9	PB5B	2	PCLK2_1****	C	N9	PB7B	4	PCLK4_1****	C	N9	PB10F	4	PCLK4_1****	C
P10	PB7B	2		C	P10	PB7D	4		C	P10	PB10D	4		C
P9	PB7A	2		T	P9	PB7C	4		T	P9	PB10C	4		T
M9	PB6B	2	PCLK2_0****	C	M9	PB7F	4	PCLK4_0****	C	M9	PB10B	4	PCLK4_0****	C

LA-MachXO640, LA-MachXO1200 and LA-MachXO2280 Logic Signal Connections: 256 ftBGA (Cont.)

LAMXO640					LAMXO1200					LAMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
E11	NC				E11	PT10D	1		C	E11	PT15B	1		C
E10	NC				E10	PT10C	1		T	E10	PT15A	1		T
D12	PT9D	0		C	D12	PT10B	1		C	D12	PT14D	1		C
D11	PT9C	0		T	D11	PT10A	1		T	D11	PT14C	1		T
A14	PT7F	0		C	A14	PT9F	1		C	A14	PT14B	1		C
A13	PT7E	0		T	A13	PT9E	1		T	A13	PT14A	1		T
C12	PT8B	0		C	C12	PT9D	1		C	C12	PT13D	1		C
C11	PT8A	0		T	C11	PT9C	1		T	C11	PT13C	1		T
-	-				VCCIO1	VCCIO1	1			VCCIO1	VCCIO1	1		
-	-				GND	GNDIO1	1			GND	GNDIO1	1		
B12	PT7B	0		C	B12	PT9B	1		C	B12	PT12D	1		C
B11	PT7A	0		T	B11	PT9A	1		T	B11	PT12C	1		T
A12	PT7D	0		C	A12	PT8F	1		C	A12	PT12B	1		C
A11	PT7C	0		T	A11	PT8E	1		T	A11	PT12A	1		T
GND	GND	-			GND	GND	-			GND	GND	-		
B10	PT5D	0		C	B10	PT8D	1		C	B10	PT11B	1		C
B9	PT5C	0		T	B9	PT8C	1		T	B9	PT11A	1		T
D10	PT8D	0		C	D10	PT8B	1		C	D10	PT10F	1		C
D9	PT8C	0		T	D9	PT8A	1		T	D9	PT10E	1		T
-	-				VCCIO1	VCCIO1	1			VCCIO1	VCCIO1	1		
-	-				GND	GNDIO1	1			GND	GNDIO1	1		
C10	PT6D	0		C	C10	PT7F	1		C	C10	PT10D	1		C
C9	PT6C	0		T	C9	PT7E	1		T	C9	PT10C	1		T
A9	PT6B	0	PCLK0_1****	C	A9	PT7D	1	PCLK1_1****	C	A9	PT10B	1	PCLK1_1****	C
A10	PT6A	0		T	A10	PT7C	1		T	A10	PT10A	1		T
E9	PT9B	0		C	E9	PT7B	1		C	E9	PT9D	1		C
E8	PT9A	0		T	E8	PT7A	1		T	E8	PT9C	1		T
D7	PT5B	0	PCLK0_0****	C	D7	PT6F	0	PCLK1_0****	C	D7	PT9B	1	PCLK1_0****	C
D8	PT5A	0		T	D8	PT6E	0		T	D8	PT9A	1		T
VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0		
GND	GNDIO0	0			GND	GNDIO0	0			GND	GNDIO0	0		
C8	PT4F	0		C	C8	PT6D	0		C	C8	PT8D	0		C
B8	PT4E	0		T	B8	PT6C	0		T	B8	PT8C	0		T
A8	VCCAUX	-			A8	VCCAUX	-			A8	VCCAUX	-		
A7	PT4D	0		C	A7	PT6B	0		C	A7	PT7D	0		C
A6	PT4C	0		T	A6	PT6A	0		T	A6	PT7C	0		T
B7	PT4B	0		C	B7	PT5F	0		C	B7	PT7B	0		C
B6	PT4A	0		T	B6	PT5E	0		T	B6	PT7A	0		T
C6	PT3C	0		T	C6	PT5C	0		T	C6	PT6A	0		T
C7	PT3D	0		C	C7	PT5D	0		C	C7	PT6B	0		C
A5	PT3E	0		T	A5	PT5A	0		T	A5	PT6C	0		T
A4	PT3F	0		C	A4	PT5B	0		C	A4	PT6D	0		C
E7	NC				E7	PT4C	0		T	E7	PT6E	0		T
E6	NC				E6	PT4D	0		C	E6	PT6F	0		C
B5	PT3B	0		C	B5	PT3F	0		C	B5	PT5D	0		C
B4	PT3A	0		T	B4	PT3E	0		T	B4	PT5C	0		T
D5	PT2D	0		C	D5	PT3D	0		C	D5	PT5B	0		C
D6	PT2C	0		T	D6	PT3C	0		T	D6	PT5A	0		T
C4	PT2E	0		T	C4	PT4A	0		T	C4	PT4A	0		T
C5	PT2F	0		C	C5	PT4B	0		C	C5	PT4B	0		C
-	-	-			-	-	-			GND	GND	-		
D4	NC				D4	PT2D	0		C	D4	PT3D	0		C
D3	NC				D3	PT2C	0		T	D3	PT3C	0		T

LA-MachXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

LAMXO2280				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
T2	PL20B	6		C
P6	TMS	5	TMS	
V1	PB2A	5		T
U2	PB2B	5		C
T3	PB2C	5		T
N7	TCK	5	TCK	
R4	PB2D	5		C
R5	PB3A	5		T
T4	PB3B	5		C
VCC	VCC	-		
R6	PB3C	5		T
P7	PB3D	5		C
U3	PB4A	5		T
T5	PB4B	5		C
V2	PB4C	5		T
N8	TDO	5	TDO	
V3	PB4D	5		C
T6	PB5A	5		T
GND	GNDIO5	5		
VCCIO5	VCCIO5	5		
U4	PB5B	5		C
P8	PB5C	5		T
T7	PB5D	5		C
V4	TDI	5	TDI	
R8	PB6A	5		T
N9	PB6B	5		C
U5	PB6C	5		T
V5	PB6D	5		C
U6	PB7A	5		T
VCC	VCC	-		
V6	PB7B	5		C
P9	PB7C	5		T
T8	PB7D	5		C
U7	PB8A	5		T
V7	PB8B	5		C
M10	VCCAUX	-		
U8	PB8C	5		T
V8	PB8D	5		C
VCCIO5	VCCIO5	5		
GND	GNDIO5	5		
T9	PB8E	5		T
U9	PB8F	5		C
V9	PB9A	4		T

LA-MachXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

LAMXO2280				
Ball Number	**Ball Function**	**Bank**	**Dual Function**	**Differential**
E13	PT16D	1		C
C15	PT16C	1		T
F13	PT16B	1		C
D14	PT16A	1		T
A18	PT15D	1		C
B17	PT15C	1		T
A16	PT15B	1		C
A17	PT15A	1		T
VCC	VCC	-		
D13	PT14D	1		C
F12	PT14C	1		T
C14	PT14B	1		C
E12	PT14A	1		T
C13	PT13D	1		C
B16	PT13C	1		T
B15	PT13B	1		C
A15	PT13A	1		T
VCCIO1	VCCIO1	1		
GND	GNDIO1	1		
B14	PT12F	1		C
A14	PT12E	1		T
D12	PT12D	1		C
F11	PT12C	1		T
B13	PT12B	1		C
A13	PT12A	1		T
C12	PT11D	1		C
GND	GND	-		
B12	PT11C	1		T
E11	PT11B	1		C
D11	PT11A	1		T
C11	PT10F	1		C
A12	PT10E	1		T
VCCIO1	VCCIO1	1		
GND	GNDIO1	1		
F10	PT10D	1		C
D10	PT10C	1		T
B11	PT10B	1	PCLK1_1***	C
A11	PT10A	1		T
E10	PT9D	1		C
C10	PT9C	1		T
D9	PT9B	1	PCLK1_0***	C
E9	PT9A	1		T
B10	PT8F	0		C

LA-MachXO Automotive Family Data Sheet Ordering Information

April 2006 Data Sheet DS1003

Part Number Description

LAMXO XXXX X – X XXXXXX X

Device Family
LA-MachXO Automotive PLD

Logic Capacity
256 LUTs = 256
640 LUTs = 640
1200 LUTs = 1200
2280 LUTs = 2280

Supply Voltage
C = 1.8V/2.5V/3.3V
E = 1.2V

Grade
E = Automotive

Package
TN100 = 100-pin Lead-Free TQFP
TN144 = 144-pin Lead-Free TQFP
FTN256 = 256-ball Lead-Free ftBGA
FTN324 = 324-ball Lead-Free ftBGA

Speed
3 = -3 Speed Grade

Note: Parts dual marked as described.

Ordering Information

Part Number	LUTs	Supply Voltage	I/Os	Grade	Package	Pins	Temp.
LAMXO256C-3TN100E	256	1.8V/2.5V/3.3V	78	-3	Lead-Free TQFP	100	AUTO
LAMXO640C-3TN100E	640	1.8V/2.5V/3.3V	74	-3	Lead-Free TQFP	100	AUTO
LAMXO640C-3TN144E	640	1.8V/2.5V/3.3V	113	-3	Lead-Free TQFP	144	AUTO
LAMXO640C-3FTN256E	640	1.8V/2.5V/3.3V	159	-3	Lead-Free ftBGA	256	AUTO
LAMXO256E-3TN100E	256	1.2V	78	-3	Lead-Free TQFP	100	AUTO
LAMXO640E-3TN100E	640	1.2V	74	-3	Lead-Free TQFP	100	AUTO
LAMXO640E-3TN144E	640	1.2V	113	-3	Lead-Free TQFP	144	AUTO
LAMXO640E-3FTN256E	640	1.2V	159	-3	Lead-Free ftBGA	256	AUTO
LAMXO1200E-3TN100E	1200	1.2V	73	-3	Lead-Free TQFP	100	AUTO
LAMXO1200E-3TN144E	1200	1.2V	113	-3	Lead-Free TQFP	144	AUTO
LAMXO1200E-3FTN256E	1200	1.2V	211	-3	Lead-Free ftBGA	256	AUTO
LAMXO2280E-3TN100E	2280	1.2V	73	-3	Lead-Free TQFP	100	AUTO
LAMXO2280E-3TN144E	2280	1.2V	113	-3	Lead-Free TQFP	144	AUTO
LAMXO2280E-3FTN256E	2280	1.2V	211	-3	Lead-Free ftBGA	256	AUTO
LAMXO2280E-3FTN324E	2280	1.2V	271	-3	Lead-Free ftBGA	324	AUTO