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Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixedfunction ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	4.9 ns
Voltage Supply - Internal	1.71V ~ 3.465V
Number of Logic Elements/Blocks	-
Number of Macrocells	320
Number of Gates	-
Number of I/O	159
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lamxo640c-3ftn256e

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Lattice LA-MachXO Automotive Family Data Sheet **Architecture**

February 2007

Data Sheet DS1003

Architecture Overview

The LA-MachXO family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). Some devices in this family have sysCLOCK PLLs and blocks of sysMEM[™] Embedded Block RAM (EBRs). Figures 2-1, 2-2, and 2-3 show the block diagrams of the various family members.

The logic blocks are arranged in a two-dimensional grid with rows and columns. The EBR blocks are arranged in a column to the left of the logic array. The PIO cells are located at the periphery of the device, arranged into Banks. The PIOs utilize a flexible I/O buffer referred to as a sysIO interface that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and the Programmable Functional unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PFF block contains building blocks for logic, arithmetic, ROM, and register functions. Both the PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and effectively. Logic blocks are arranged in a two-dimensional array. Only one type of block is used per row.

In the LA-MachXO family, the number of sysIO Banks varies by device. There are different types of I/O Buffers on different Banks. See the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found only in the larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag "hard" control logic to minimize LUT use.

The LA-MachXO architecture provides up to two sysCLOCK[™] Phase Locked Loop (PLL) blocks on larger devices. These blocks are located at either end of the memory blocks. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

Every device in the family has a JTAG Port that supports programming and configuration of the device as well as access to the user logic. The LA-MachXO devices are available for operation from 3.3V, 2.5V, 1.8V, and 1.2V power supplies, providing easy integration into the overall system.

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Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM, and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SP 16x2	ROM 16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM 16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables (LUT4). A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7, and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
- A greater-than-or-equal-to B
- A not-equal-to B
- A less-than-or-equal-to B

Two additional signals, Carry Generate and Carry Propagate, are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x2-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

The ispLEVER design tool supports the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-6 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices. One Slice functions as the read-write port, while the other companion Slice supports the read-only port. For more information on RAM mode in LA-MachXO devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of Slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

The LA-MachXO automotive family of devices provides global signals that are available to all PFUs. These signals consist of four primary clocks and four secondary clocks. Primary clock signals are generated from four 16:1 muxes as shown in Figure 2-7 and Figure 2-8. The available clock sources for the LA-MachXO256 and LA-MachXO640 devices are four dual function clock pins and 12 internal routing signals. The available clock sources for the LA-MachXO2280 devices are four dual function clock pins, up to nine internal routing signals and up to six PLL outputs.





Table 2-10.	. Supported	Output	Standards
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Output Standard	Drive	V _{ССЮ} (Тур.)
Single-ended Interfaces	, , , , , , , , , , , , , , , , , , ,	
LVTTL	4mA, 8mA, 12mA, 16mA	3.3
LVCMOS33	4mA, 8mA, 12mA, 14mA	3.3
LVCMOS25	4mA, 8mA, 12mA, 14mA	2.5
LVCMOS18	4mA, 8mA, 12mA, 14mA	1.8
LVCMOS15	4mA, 8mA	1.5
LVCMOS12	2mA, 6mA	1.2
LVCMOS33, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVCMOS25, Open Drain	4mA, 8mA, 12mA, 14mA	_
LVCMOS18, Open Drain	4mA, 8mA, 12mA, 14mA	_
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA, 6mA	_
PCI33 ³	N/A	3.3
Differential Interfaces		
LVDS ^{1, 2}	N/A	2.5
BLVDS, RSDS ²	N/A	2.5
LVPECL ²	N/A	3.3

1. LA-MachXO1200 and LA-MachXO2280 devices have dedicated LVDS buffers.

2. These interfaces can be emulated with external resistors in all devices.

3. Top Banks of LA-MachXO1200 and LA-MachXO2280 devices only.

sysIO Buffer Banks

The number of Banks vary between the devices of this family. Eight Banks surround the two larger devices, the LA-MachXO1200 and LA-MachXO2280 (two Banks per side). The LA-MachXO640 has four Banks (one Bank per side). The smallest member of this family, the LA-MachXO256, has only two Banks.

Each sysIO buffer Bank is capable of supporting multiple I/O standards. Each Bank has its own I/O supply voltage (V_{CCIO}) which allows it to be completely independent from the other Banks. Figure 2-18, Figure 2-18, Figure 2-20 and Figure 2-21 shows the sysIO Banks and their associated supplies for all devices.

Programming and Erase Flash Supply Current^{1, 2, 3, 4}

Symbol	Parameter	Device	Typ.⁵	Units
		LCMXO256C	9	mA
		LCMXO640C	11	mA
	Care Dower Supply	LCMXO256E	6	mA
Icc	Core Power Supply	LCMXO640E	8	mA
		LCMXO1200E	12	mA
		LCMXO2280E	14	mA
Iccaux		LCMXO256E/C	8	mA
	Auxiliary Power Supply	LCMXO640E/C	10	mA
	$V_{CCAUX} = 3.3V$	LCMXO1200E	15	mA
		LCMXO2280E	16	mA
I _{CCIO}	Bank Power Supply ⁶	All devices	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.

2. Assumes all I/O pins are held at $V_{\mbox{CCIO}}$ or GND.

3. Typical user pattern.

4. JTAG programming is at 25MHz.

5. $T_J = 25^{\circ}$ C, power supplies at nominal voltage. 6. Per Bank. V_{CCIO} = 2.5V. Does not include pull-up/pull-down.

Input/Output	V _{IL}		V _{IH}		Vo. Max	Vou Min	lau ¹	leu ¹
Standard	Min. (V)	Max. (V)	Min. (V)	Max. (V)	(V)	(V)	(mA)	(mA)
	0.2	0.9	2.0	2.6	0.4	V _{CCIO} - 0.4	16, 12, 8, 4	-14, -12, -8, -4
	-0.3	0.0	2.0	3.0	0.2	V _{CCIO} - 0.2	0.1	-0.1
					0.4	2.4	16	-16
LVTTL	-0.3	0.8	2.0	3.6	0.4	V _{CCIO} - 0.4	12, 8, 4	-12, -8, -4
			(0.2	V _{CCIO} - 0.2	0.1	-0.1	
	-0.3	0.7	17	3.6	0.4	V _{CCIO} - 0.4	16, 12, 8, 4	-14, -12, -8, -4
2001000 2.5	-0.5	-0.5 0.7	1.7	. 5.0	0.2	V _{CCIO} - 0.2	0.1	-0.1
	-0.3	0.351/2010	0.651/2010	3.6	0.4	V _{CCIO} - 0.4	16, 12, 8, 4	-14, -12, -8, -4
	-0.5	0.00 0.00	0.034 CCIO	0.0	0.2	V _{CCIO} - 0.2	0.1	-0.1
	-0.3	0.351/	0.651/	3.6	0.4	V _{CCIO} - 0.4	8, 4	-8, -4
	-0.5	0.33 A CCIO	0.03 4 CCIO	5.0	0.2	V _{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2	-03	0 / 2	0.78	3.6	0.4	V _{CCIO} - 0.4	6, 2	-6, -2
("C" Version)	-0.5	0.42	0.70	0.0	0.2	V _{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2	-0.3	0.35\/	0.65\/	3.6	0.4	V _{CCIO} - 0.4	6, 2	-6, -2
("E" Version)	-0.5	0.00 v CC	0.03 4 CC	0.0	0.2	V _{CCIO} - 0.2	0.1	-0.1
PCI	-0.3	0.3V _{CCIO}	0.5V _{CCIO}	3.6	0.1V _{CCIO}	0.9V _{CCIO}	1.5	-0.5

sysIO Single-Ended DC Electrical Characteristics

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O Bank and the end of an I/O Bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between Bank GND connections or between the last GND in a Bank and the end of a Bank.

sysIO Differential Electrical Characteristics LVDS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Тур.	Max.	Units
V _{INP,} V _{INM}	Input Voltage		0		2.4	V
V _{THD}	Differential Input Threshold		+/-100	_	—	mV
		100mV ≤ V _{THD}	V _{THD} /2	1.2	1.8	V
V _{CM}	Input Common Mode Voltage	$200 \text{mV} \le \text{V}_{\text{THD}}$	V _{THD} /2	1.2	1.9	V
		350mV ≤ V _{THD}	V _{THD} /2	1.2	2.0	V
I _{IN}	Input current	Power on	—	_	+/-10	μA
V _{OH}	Output high voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	—	1.38	1.60	V
V _{OL}	Output low voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	0.9V	1.03	—	V
V _{OD}	Output voltage differential	(V _{OP} - V _{OM}), R _T = 100 Ohm	250	350	450	mV
ΔV _{OD}	Change in V _{OD} between high and low		_	_	50	mV
V _{OS}	Output voltage offset	$(V_{OP} - V_{OM})/2, R_{T} = 100 \text{ Ohm}$	1.125	1.25	1.375	V
ΔV _{OS}	Change in V _{OS} between H and L		—	_	50	mV
I _{OSD}	Output short circuit current	V _{OD} = 0V Driver outputs shorted	_	_	6	mA

Over Recommended Operating Conditions

LVDS Emulation

LA-MachXO automotive devices can support LVDS outputs via emulation (LVDS25E), in addition to the LVDS support that is available on-chip on certain devices. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

Figure 3-1. LVDS Using External Resistors (LVDS25E)



Note: All resistors are $\pm 1\%$.

The LVDS differential input buffers are available on certain devices in the LA-MachXO family.

Table 3-1. LVDS DC Conditions

Parameter	Description	Typical	Units
Z _{OUT}	Output impedance	20	Ω
R _S	Driver series resistor	294	Ω
R _P	Driver parallel resistor	121	Ω
R _T	Receiver termination	100	Ω
V _{OH}	Output high voltage	1.43	V
V _{OL}	Output low voltage	1.07	V
V _{OD}	Output differential voltage	0.35	V
V _{CM}	Output common mode voltage	1.25	V
Z _{BACK}	Back impedance	100	Ω
I _{DC}	DC output current	3.66	mA

Over Recommended Operating Conditions

BLVDS

The LA-MachXO automotive family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. The input standard is supported by the LVDS differential input buffer on certain devices. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example



Table 3-2. BLVDS DC Conditions¹

		Nominal		
Symbol	Description	Zo = 45	Zo = 90	Units
Z _{OUT}	Output impedance	100	100	ohm
R _{TLEFT}	Left end termination	45	90	ohm
R _{TRIGHT}	Right end termination	45	90	ohm
V _{OH}	Output high voltage	1.375	1.48	V
V _{OL}	Output low voltage	1.125	1.02	V
V _{OD}	Output differential voltage	0.25	0.46	V
V _{CM}	Output common mode voltage	1.25	1.25	V
I _{DC}	DC output current	11.2	10.2	mA
4 Carlingard In 16				

Over Recommended Operating Conditions

1. For input buffer, see LVDS table.

LVPECL

The LA-MachXO automotive family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer on certain devices. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL



Table 3-3. LVPECL DC Conditions¹

Over Recommended	Operating	Conditions
	operating	oonantions

Symbol	Description	Nominal	Units
Z _{OUT}	Output impedance	100	ohm
R _P	Driver parallel resistor	150	ohm
R _T	Receiver termination	100	ohm
V _{OH}	Output high voltage	2.03	V
V _{OL}	Output low voltage	1.27	V
V _{OD}	Output differential voltage	0.76	V
V _{CM}	Output common mode voltage	1.65	V
Z _{BACK}	Back impedance	85.7	ohm
I _{DC}	DC output current	12.7	mA

1. For input buffer, see LVDS table.

Typical Building Block Function Performance¹

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	-3 Timing	Units		
Basic Functions				
16-bit decoder	9.4	ns		
4:1 MUX	6.3	ns		
16:1 MUX	7.1	ns		

Register-to-Register Performance

Function	-3 Timing	Units							
Basic Functions									
16:1 MUX	348	MHz							
16-bit adder	209	MHz							
16-bit counter	277	MHz							
64-bit counter	143	MHz							
Embedded Memory Functions (1200 and 2280 Devices Only)									
256x36 Single Port RAM	203	MHz							
512x18 True-Dual Port RAM	203	MHz							
Distributed Memory Functions									
16x2 Single Port RAM	310	MHz							
64x2 Single Port RAM	229	MHz							
128x4 Single Port RAM	186	MHz							
32x2 Pseudo-Dual Port RAM	224	MHz							
64x4 Pseudo-Dual Port RAM	194	MHz							

 The above timing numbers are generated using the ispLEVER design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
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Derating Logic Timing

Logic Timing provided in the following sections of the data sheet and the ispLEVER design tools are worst case numbers in the operating range. Actual delays may be much faster. The ispLEVER design tool from Lattice can provide logic timing numbers at a particular temperature and voltage.

sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min.	Max.	Units
f _{IN}	Input Clock Frequency (CLKI, CLKFB)		25	420	MHz
f _{OUT}	Output Clock Frequency (CLKOP, CLKOS)		25	420	MHz
f _{OUT2}	K-Divider Output Frequency (CLKOK)		0.195	210	MHz
f _{VCO}	PLL VCO Frequency		420	840	MHz
f _{PFD}	Phase Detector Input Frequency		25	—	MHz
AC Characte	eristics				
t _{DT}	Output Clock Duty Cycle	Default duty cycle selected ³	45	55	%
t _{PH} ⁴	Output Phase Accuracy		—	0.05	UI
+ . 1	Output Clock Poriod litter	Fout ≥ 100MHz	_	+/-120	ps
OPJIT		Fout < 100MHz	_	0.02	UIPP
t _{SK}	Input Clock to Output Clock Skew	Divider ratio = integer	—	+/-200	ps
t _W	Output Clock Pulse Width	At 90% or 10% ³	1		ns
t _{LOCK} ²	PLL Lock-in Time		—	150	μs
t _{PA}	Programmable Delay Unit		100	450	ps
t _{IPJIT}	Input Clock Period Jitter		_	+/-200	ps
t _{FBKDLY}	External Feedback Delay		—	10	ns
t _{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t _{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t _{RST}	RST Pulse Width		10	—	ns

Over Recommended Operating Conditions

1. Jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. CLKOS as compared to CLKOP output.

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LA-MachXO "C" Sleep Mode Timing

Symbol	Parameter	Device	Min.	Тур.	Max	Units
t _{PWRDN}	SLEEPN Low to Power Down	All	—	_	400	ns
t	SI EEPN High to Power Lin	LCMXO256	—	-	400	μs
PWRUP		LCMXO640	—	-	600	μs
t _{WSLEEPN}	SLEEPN Pulse Width	All	400	_	—	ns
t _{WAWAKE}	SLEEPN Pulse Rejection	All		_	100	ns

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Pin Information Summary

		LAMXO256C/E		LAMXO640C/E	
Pin Type		100 TQFP	100 TQFP	144 TQFP	256 ftBGA
Single Ended User I/O		78	78 74 113		159
Differential Pair User I/O ¹	38	17	43	79	
Muxed		6	6	6	6
ТАР		4	4	4	4
Dedicated (Total Without Supplie	5	5	5	5	
VCC	2	2	4	4	
VCCAUX		1	1 1 2		2
	Bank0	3	2	2	4
VCCIO	Bank1	3	2	2	4
	Bank2	—	2	2	4
	Bank3	—	2	2	4
GND		8	10	12	18
NC		0	0	0	52
	Bank0	41/20	18/5	29/10	42/21
Single Ended/Differential I/O	Bank1	37/18	21/4	30/11	40/20
perBank	Bank2	—	14/2	24/9	36/18
	Bank3	—	21/6	30/13	40/20

1. These devices support emulated LVDS outputs. LVDS inputs are not supported.

			LAMXO1200E			LAMX	D2280E	
Pin Type		100 TQFP	144 TQFP	256 ftBGA	100 TQFP	144 TQFP	256 ftBGA	324 ftBGA
Single Ended User I/O		73	113	211	73	113	211	271
Differential Pair User I/O ¹		27	48	105	30	47	105	134
Muxed		6	6	6	6	6	6	6
TAP		4	4	4	4	4	4	4
Dedicated (Total Without Sup	plies)	5	5	5	5	5	5	5
VCC		4	4	4	2	4	4	6
VCCAUX		2	2	2	2	2	2	2
	Bank0	1	1	2	1	1	2	2
	Bank1	1	1	2	1	1	2	2
	Bank2	1	1	2	1	1	2	2
VCCIO	Bank3	1	1	2	1	1	2	2
	Bank4	1	1	2	1	1	2	2
	Bank5	1	1	2	1	1	2	2
	Bank6	1	1	2	1	1	2	2
	Bank7	1	1	2	1	1	2	2
GND		8	12	18	8	12	18	24
NC		0	0	0	0	0	0	0
	Bank0	10/3	14/6	26/13	9/3	13/6	24/12	34/17
	Bank1	8/2	15/7	28/14	9/3	16/7	30/15	36/18
	Bank2	10/4	15/7	26/13	10/4	15/7	26/13	34/17
Single Ended/Differential I/O	Bank3	11/5	15/7	28/14	11/5	15/7	28/14	34/17
per Bank	Bank4	8/3	14/5	27/13	8/3	14/4	29/14	35/17
	Bank5	5/2	10/4	22/11	5/2	10/4	20/10	30/15
	Bank6	10/3	15/6	28/14	10/4	15/6	28/14	34/17
	Bank7	11/5	15/6	26/13	11/5	15/6	26/13	34/17
1. These devices support on-chip	LVDS buffers	for left and right I/0	D Banks.					

LA-MachXO256 and LA-MachXO640 Logic Signal Connections: 100 TQFP (Cont.)

		LAM>	(O256		LAMXO640				
	Ball		Dual		Ball		Dual		
Pin Number	Function	Bank	Function	Differential	Function	Bank	Function	Differential	
42	GNDIO1	1			GNDIO2	2			
43	PB4A	1		Т	PB8B	2			
44	PB4B	1		С	PB8C	2		Т	
45	PB4C	1		Т	PB8D	2		С	
46	PB4D	1		С	PB9A	2			
47	PB5A	1			PB9C	2		Т	
48*	SLEEPN	-	SLEEPN		SLEEPN	-	SLEEPN		
49	PB5C	1		Т	PB9D	2		С	
50	PB5D	1		С	PB9F	2			
51	PR9B	0		С	PR11D	1		С	
52	PR9A	0		Т	PR11B	1		С	
53	PR8B	0		С	PR11C	1		Т	
54	PR8A	0		Т	PR11A	1		Т	
55	PR7D	0		С	PR10D	1		С	
56	PR7C	0		Т	PR10C	1		Т	
57	PR7B	0		С	PR10B	1		С	
58	PR7A	0		Т	PR10A	1		Т	
59	PR6B	0		С	PR9D	1			
60	VCCIO0	0			VCCIO1	1			
61	PR6A	0		Т	PR9B	1			
62	GNDIO0	0			GNDIO1	1			
63	PR5D	0		С	PR7B	1			
64	PR5C	0		Т	PR6C	1			
65	PR5B	0		С	PR6B	1			
66	PR5A	0		Т	PR5D	1			
67	PR4B	0		С	PR5B	1			
68	PR4A	0		Т	PR4D	1			
69	PR3D	0		С	PR4B	1			
70	PR3C	0		Т	PR3D	1			
71	PR3B	0		С	PR3B	1			
72	PR3A	0		Т	PR2D	1			
73	PR2B	0		С	PR2B	1			
74	VCCIO0	0			VCCIO1	1			
75	GNDIO0	0			GNDIO1	1			
76	PR2A	0		Т	PT9F	0		С	
77	PT5C	0			PT9E	0		Т	
78	PT5B	0		С	PT9C	0			
79	PT5A	0		Т	PT9A	0			
80	PT4F	0		С	VCCIO0	0			
81	PT4E	0		Т	GNDIO0	0			
82	PT4D	0		С	PT7E	0			

LA-MachXO1200 and LA-MachXO2280 Logic Signal Connections: 100 TQFP (Cont.)

		ļ	LAMXO1200		LAMXO2280				
Pin Number	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential	
41	GND	-			GND	-			
42	PB9A	4		Т	PB12A	4		Т	
43	PB9B	4		С	PB12B	4		С	
44	VCCIO4	4			VCCIO4	4			
45	PB10A	4		Т	PB13A	4		Т	
46	PB10B	4		С	PB13B	4		С	
47	NC	-	NC		NC	-	NC		
48	PB11A	4		Т	PB16A	4		Т	
49	PB11B	4		С	PB16B	4		С	
50**	GNDIO3 GNDIO4	-			GNDIO3 GNDIO4	-			
51	PR16B	3			PR19B	3			
52	PR15B	3		C*	PR18B	3		C*	
53	PR15A	3		T*	PR18A	3		T*	
54	PR14B	3		C*	PR17B	3		C*	
55	PR14A	3		T*	PR17A	3		T*	
56	VCCIO3	3			VCCIO3	3			
57	PR12B	3		C*	PR15B	3		C*	
58	PR12A	3		T*	PR15A	3		T*	
59	GND	-			GND	-			
60	PR10B	3		C*	PR13B	3		C*	
61	PR10A	3		T*	PR13A	3		T*	
62	PR9B	3		C*	PR11B	3		C*	
63	PR9A	3		T*	PR11A	3		T*	
64	PR8B	2		C*	PR10B	2		C*	
65	PR8A	2		T*	PR10A	2		T*	
66	VCC	-			VCC	-			
67	PR6C	2			PR8C	2			
68	PR6B	2		C*	PR8B	2		C*	
69	PR6A	2		T*	PR8A	2		T*	
70	VCCIO2	2			VCCIO2	2			
71	PR4D	2			PR5D	2			
72	PR4B	2		C*	PR5B	2		C*	
73	PR4A	2		T*	PR5A	2		T*	
74	PR2B	2		С	PR3B	2		C*	
75	PR2A	2		Т	PR3A	2		T*	
76**	GNDIO1 GNDIO2	-			GNDIO1 GNDIO2	-			
77	PT11C	1			PT15C	1			
78	PT11B	1		С	PT14B	1		С	
79	PT11A	1		Т	PT14A	1		Т	

LA-MachXO640, LA-MachXO1200 and LA-MachXO2280 Logic Signal Connections: 256 ftBGA (Cont.)

		LAM	(O 640		LAMXO1200			LAMXO2280						
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
J4	PL8A	3		Т	J4	PL13A	6		T**	J4	PL16A	6		T**
J5	PL8B	3		С	J5	PL13B	6		C**	J5	PL16B	6		C**
R1	PL11A	3		Т	R1	PL13C	6		Т	R1	PL16C	6		Т
R2	PL11B	3		С	R2	PL13D	6		С	R2	PL16D	6		С
-	-	-			-	-	-			GND	GND	-		
K5	NC				K5	PL14A	6	LLM0_PLLT_FB_A	T**	K5	PL17A	6	LLM0_PLLT_FB_A	T**
K4	NC				K4	PL14B	6	LLM0_PLLC_FB_A	C**	K4	PL17B	6	LLM0_PLLC_FB_A	C**
L5	PL10C	3		Т	L5	PL14C	6		Т	L5	PL17C	6		Т
L4	PL10D	3		С	L4	PL14D	6		С	L4	PL17D	6		С
M5	NC				M5	PL15A	6	LLM0_PLLT_IN_A	T**	M5	PL18A	6	LLM0_PLLT_IN_A	T**
M4	NC				M4	PL15B	6	LLM0_PLLC_IN_A	C**	M4	PL18B	6	LLM0_PLLC_IN_A	C**
N4	PL11C	3		Т	N4	PL16A	6		Т	N4	PL19A	6		Т
N3	PL11D	3		С	N3	PL16B	6		С	N3	PL19B	6		С
VCCIO3	VCCIO3	3			VCCIO6	VCCIO6	6			VCCIO6	VCCIO6	6		
GND	GNDIO3	3			GND	GNDIO6	6			GND	GNDIO6	6		
GND	GNDIO2	2			GND	GNDIO5	5			GND	GNDIO5	5		
VCCIO2	VCCIO2	2			VCCIO5	VCCIO5	5			VCCI05	VCCI05	5		
P4	TMS	2	TMS		P4	TMS	5	TMS		P4	TMS	5	TMS	
P2	NC				P2	PB2A	5		Т	P2	PB2A	5		Т
P3	NC				P3	PB2B	5		С	P3	PB2B	5		С
N5	NC				N5	PB2C	5		Т	N5	PB2C	5		Т
R3	TCK	2	TCK		R3	TCK	5	тск		R3	TCK	5	тск	
N6	NC				N6	PB2D	5		С	N6	PB2D	5		С
T2	PB2A	2		Т	T2	PB3A	5		Т	T2	PB3A	5		Т
T3	PB2B	2		С	Т3	PB3B	5		С	Т3	PB3B	5		С
R4	PB2C	2		т	R4	PB3C	5		Т	R4	PB3C	5		Т
R5	PB2D	2		С	R5	PB3D	5		С	R5	PB3D	5		С
P5	PB3A	2		Т	P5	PB4A	5		Т	P5	PB4A	5		Т
P6	PB3B	2		С	P6	PB4B	5		С	P6	PB4B	5		С
T5	PB3C	2		Т	T5	PB4C	5		Т	T5	PB4C	5		Т
M6	TDO	2	TDO		M6	TDO	5	TDO		M6	TDO	5	TDO	
T4	PB3D	2		С	T4	PB4D	5		С	T4	PB4D	5		С
R6	PB4A	2		Т	R6	PB5A	5		Т	R6	PB5A	5		Т
GND	GNDIO2	2			GND	GNDIO5	5			GND	GNDIO5	5		
VCCIO2	VCCIO2	2			VCCIO5	VCCIO5	5			VCCIO5	VCCIO5	5		
T6	PB4B	2		С	Т6	PB5B	5		С	Т6	PB5B	5		С
N7	TDI	2	TDI		N7	TDI	5	TDI		N7	TDI	5	TDI	
Т8	PB4C	2		т	Т8	PB5C	5		Т	Т8	PB6A	5		Т
T7	PB4D	2		С	T7	PB5D	5		С	T7	PB6B	5		С
M7	NC				M7	PB6A	5		Т	M7	PB7C	5		Т
M8	NC				M8	PB6B	5		С	M8	PB7D	5		С
Т9	VCCAUX	-			Т9	VCCAUX	-			Т9	VCCAUX	-		
R7	PB4E	2		Т	R7	PB6C	5		Т	R7	PB8C	5		Т
R8	PB4F	2		С	R8	PB6D	5		С	R8	PB8D	5		С
-	-				VCCIO5	VCCI05	5			VCCIO5	VCCI05	5		
-	-				GND	GNDIO5	5			GND	GNDIO5	5		
P7	PB5C	2		Т	P7	PB6E	5		Т	P7	PB9A	4		Т
P8	PB5D	2		С	P8	PB6F	5		С	P8	PB9B	4		С
N8	PB5A	2		Т	N8	PB7A	4		Т	N8	PB10E	4		Т
N9	PB5B	2	PCLK2_1****	С	N9	PB7B	4	PCLK4_1****	С	N9	PB10F	4	PCLK4_1****	С
P10	PB7B	2		С	P10	PB7D	4		С	P10	PB10D	4		С
P9	PB7A	2		Т	P9	PB7C	4		Т	P9	PB10C	4		Т
M9	PB6B	2	PCLK2_0****	С	M9	PB7F	4	PCLK4_0****	С	M9	PB10B	4	PCLK4_0****	С

LA-MachXO640, LA-MachXO1200 and LA-MachXO2280 Logic Signal Connections: 256 ftBGA (Cont.)

Ball Ball Ball Dual Numerial Ball Partial Partia Partia Partia			LAM)	(0640				LAM	IXO1200		LAMXO2280				
E11 NC V E11 P100 1 CC E11 P130 1 CC P130 1 CC P130 1 C P130 1	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
ICI NC NC C Dir PinC 1 C Dir PinD Dir Dir <thdir< th=""> Dir Dir Di</thdir<>	E11	NC				E11	PT10D	1		С	E11	PT15B	1		С
D12 PT00 0 C D12 PT00 1 PT100 1	E10	NC				E10	PT10C	1		Т	E10	PT15A	1		Т
D11 PT0C 0 C D11 PT100 1 C D110 PT100 1 C D110 PT100 1 C D110 PT100 1 C D110 PT100 D110 PT101 D110 PT100 D110 PT100 D110 PT100 D110 PT100 D110 PT100 D110 DT100 <	D12	PT9D	0		С	D12	PT10B	1		С	D12	PT14D	1		С
Anta PPTF 0 0 A14 PTFF 1 0 C A14 PTH8 1 0 C A13 PTF8 1 1 0 T A13 PTF8 0 C C1 A13 PTF8 1 C C 1 1 C T C1 PTF8 1 C T C1 PTF8 1 C C C1 PTT8 0 C C1 PTF8 0 C C1 PTF8 0 C 1 PTT8 0 C C A12 PTF8 1 C C A14 PTF8 1 C A14 PTF8 1 C C A14 PTF8 1 C C A14 PTF8 1 C C C C <td< td=""><td>D11</td><td>PT9C</td><td>0</td><td></td><td>Т</td><td>D11</td><td>PT10A</td><td>1</td><td></td><td>Т</td><td>D11</td><td>PT14C</td><td>1</td><td></td><td>Т</td></td<>	D11	PT9C	0		Т	D11	PT10A	1		Т	D11	PT14C	1		Т
A13 PTPE 0 A33 PTPE 1 A13 PTTA A14 PTTA A13 PTTA A14 PTTA A13 PTTA A14 PTTA A13 PTTA A14 PTTA A14 A14 A14 PTTA A14 <th< td=""><td>A14</td><td>PT7F</td><td>0</td><td></td><td>С</td><td>A14</td><td>PT9F</td><td>1</td><td></td><td>С</td><td>A14</td><td>PT14B</td><td>1</td><td></td><td>С</td></th<>	A14	PT7F	0		С	A14	PT9F	1		С	A14	PT14B	1		С
C12 PT8A 0 C C12 PT3D 1 C C1 PT3C 1 C C PT3D 1 C C C11 PT8A 0 C C11 PT3C 1 C T C11 PT3C 1 C T C T C T	A13	PT7E	0		Т	A13	PT9E	1		Т	A13	PT14A	1		Т
Ch1 PT8 0 Ch1 PT0C 1 C C PT0C V COID VCCID	C12	PT8B	0		С	C12	PT9D	1		С	C12	PT13D	1		С
· · · VCCI0 VCCI0 VCI0 I VCCI0 VCI0 I · · ·	C11	PT8A	0		Т	C11	PT9C	1		Т	C11	PT13C	1		Т
· · · · · · · · · · · · · · · B12 PT78 0 · C B12 PT80 1 · C B11 PT120 1 · C B11 PT120 1 · C A12 PT18 1 · C B11 PT120 1 · C A11 PT120 1 · C A11 PT120 1 · C A11 PT18 1 · C A11 PT120 1 · C A11 PT18 1 · C A11 PT180 1 · C B10 PT180 1 · C C D </td <td>-</td> <td>-</td> <td></td> <td></td> <td></td> <td>VCCIO1</td> <td>VCCIO1</td> <td>1</td> <td></td> <td></td> <td>VCCIO1</td> <td>VCCIO1</td> <td>1</td> <td></td> <td></td>	-	-				VCCIO1	VCCIO1	1			VCCIO1	VCCIO1	1		
B12 PT78 0 C B12 PT38 1 CC B12 PT120 1 C C B11 PT74 0 C A11 PT84 1 CT B11 PT120 1 C C B11 PT76 0 C C A12 PT78 1 C B11 PT120 1 C B11 PT120 1 C A11 PT76 0 C C A11 PT86 1 C A11 PT120 1 C C B10 PT50 0 C C B10 PT180 1 C B10 PT130 1 C B10 PT50 0 C B10 PT30 1 C B10 PT130 1 C B10 PT50 0 C C B10 PT30 1 C B10 D110 D1 D1 D1 D1 B10 PT50 1 PT60 1 PT60 1 PT60 D1 D1 D1 D1 C10 PT60 0 C C10 PT78 1 PC10 <th< td=""><td>-</td><td>-</td><td></td><td></td><td></td><td>GND</td><td>GNDIO1</td><td>1</td><td></td><td></td><td>GND</td><td>GNDIO1</td><td>1</td><td></td><td></td></th<>	-	-				GND	GNDIO1	1			GND	GNDIO1	1		
Bit PTA 0 T Bit PTA 1 T Bit PTA 0 A12 PTD 0 C A12 PTB 1 C A12 PT128 1 C A11 PT7C 0 C A11 PTB 1 C A11 PT124 1 C GND GND - C B10 PTB 0 C B10 PT0 1 C A11 PT124 1 C C B10 PTBC 0 C B10 PTB 1 C GND GND - C B11 PTBC 0 C B10 PTB 1 C GND GND C C B11 PTBC 0 C B10 PTB 1 C B10 PT114 1 C C B11 PTBC 0 C C D10 PTB 1 C D10 PT114 1 C C C - - C C D10 PTB 1 C C D10 PT0 1 C - -	B12	PT7B	0		С	B12	PT9B	1		С	B12	PT12D	1		С
A12 PT70 0 C A12 PT8F 1 C A12 PT12A 1 C A12 PT12A 1 A11 PT3C 0 C T A11 PT8E 1 C A11 PT12A 1 C A11 B10 PT70 0 C C B10 PT8C 1 C C B10 PT11A 1 C C B10 PT50 0 C C B10 PT8C 1 C C B10 PT11A 1 C C B10 PT80 0 C D10 PT80 0 C D10 PT80 1 C D10 PT10 1 C C D10 PT80 0 C D10 PT80 1 C D10 D10 D1 <t< td=""><td>B11</td><td>PT7A</td><td>0</td><td></td><td>Т</td><td>B11</td><td>PT9A</td><td>1</td><td></td><td>Т</td><td>B11</td><td>PT12C</td><td>1</td><td></td><td>Т</td></t<>	B11	PT7A	0		Т	B11	PT9A	1		Т	B11	PT12C	1		Т
A11 PTZ 0 (T A11 PTB 1 (T A11 PTIA 1 (T GN0	A12	PT7D	0		С	A12	PT8F	1		С	A12	PT12B	1		С
Image	A11	PT7C	0		Т	A11	PT8E	1		Т	A11	PT12A	1		Т
Bi0PTSD0CBi0PTSD1CCBi0PT1181CCBi0PT1181CCBi0Bi9PTSC0CTBi9PT8C1CBi0PT1181CTDi0PTSD0CDi0PT1681CDi0PT10F1CCDi0Di9PT3C0CTDi9PT8A1CCDi0PT10F1CCCCCCDi9PT8A1CCDi0PT10E1CCCCCCDi0PT7A1CCDi0Di1CCCPT6D0CCCOPT7F1CCCCDi01CCCPT6D0CCCOPT7F1CCCC1CCCPT6D0PCLCCCDi0PT101CCCDi01CCCPT6D0PCLCCDiPT7D1PCLCDiPCLDi<	GND	GND	-			GND	GND	-			GND	GND	-		
B9 PTSC 0 T B9 PT11A 1 1 T D10 PT8D 0 C D10 PT8C 1 C D10 PT104 1 C D10 D10 PT8C 0 C D10 PT10 1 C C D10 PT100 1 D1 C C C D10 PT10 D1 C T D1 C C C D10 PT10 D1 C T C C C C C D10 PT10 D1 C C C C C C C D10 PT10 D1 C C C PT60 0 C C C D1 PT10 D1 PT10 D1 D1 C PT60 0 PCLK0_1*** C C D1 PT10 D1 PCLK1_1*** C A PT64 0 PCLK0_1*** C A PT2 1 PCLK1_1*** C D1 PT64 0 PCLK0_0*** C A PT2 <td>B10</td> <td>PT5D</td> <td>0</td> <td></td> <td>С</td> <td>B10</td> <td>PT8D</td> <td>1</td> <td></td> <td>С</td> <td>B10</td> <td>PT11B</td> <td>1</td> <td></td> <td>С</td>	B10	PT5D	0		С	B10	PT8D	1		С	B10	PT11B	1		С
D10PT800CD10PT81CD10PT0F1CD2PT0F1CCD9PT8C0CTD9PT8C1CD9PT10F1D9PT10F1CTD9PT10F1CTD9PT10F1CD710F1CD710F1CD710F1CD710F1CD710F1CD710F1CD710F1CD710F1CD710F1CD710F1CD710F1CD710F1CD710F1CD710F1CD710F1D710F1D710F1D710F1D710F1D710F1D710F1D710F1D710F1D710F1D710F1D710F1D710F1D710FD710F1D710F	B9	PT5C	0		Т	B9	PT8C	1		Т	B9	PT11A	1		Т
D9 P18C 0 0 P18C 1 P18A 1 P18A 1 P10A P10B P10B P10	D10	PT8D	0		С	D10	PT8B	1		С	D10	PT10F	1		С
·· ··< ··< ··< ··<	D9	PT8C	0		Т	D9	PT8A	1		Т	D9	PT10E	1		Т
····III	-	-				VCCIO1	VCCIO1	1			VCCIO1	VCCIO1	1		
C10PT6D00CC10PT7F1CCC10PT1001ICCTG9PT6C00CTG9PT7C1PCLK1TG9PT1001TTA9PT6B0PCLK0TG9PT1001PCLK1TCA9PT1001PCLK1TA10PT6B0PCLK0TA9PT7B1PCLK1TA0PT01PCLK1TA10PT9B0CCE9PT901CE8PT001CCPT890PCLK0TE8PT7A1PCLK1TE8PT001PCLK1TPT80PT5A0PCLK0TE8PT071CTT <td>-</td> <td>-</td> <td></td> <td></td> <td></td> <td>GND</td> <td>GNDIO1</td> <td>1</td> <td></td> <td></td> <td>GND</td> <td>GNDIO1</td> <td>1</td> <td></td> <td></td>	-	-				GND	GNDIO1	1			GND	GNDIO1	1		
PAGe970.0PCT1.0PC	C10	PT6D	0		С	C10	PT7F	1		С	C10	PT10D	1		С
A9PT6B0PCLK0_1****CCA9PT7D1PCLK1_1****CCA9PT10B1PCLK1_1****CA10PT6A0CTA10PT7C1TA10PT1AA10PT1AA1TA10TE9PT9B0CCE9PT7B1CA10PT1AA1PCLK1_1***CCE8PT9A0CCE9PT7A1CCE9PT9D1CCF80PCBK0_0***CD7PT60PCLK1_0****CD7PT81PCLK1_0****CD8PT5A0PCLK0_0***CD7PT60PCLK1_0****D8PT9A1PCLK1_0****CD7VCC00VC0PCLK0_0***CD7PT60PCLK1_0****D8PT9A1PCLK1_0****CD8PT5A0PCLK0_0***CD7PT60PCLT_0****D8PT9A1PCLK1_0****CVCC00VCC000PT6D8PT6E0PCLT_0****D8PT9A1PCLK1_0****CVCC00VCC000CCD7D8PT9A1PCLK1_0****CD7D8PT9A1PCLK1_0****VCC00VCC000CCCCD7D8PT6AD8P	C9	PT6C	0		Т	C9	PT7E	1		Т	C9	PT10C	1		Т
A10PT6A0TA10PT7C1TA10PT10A1TA10PT10A1E9PT9B0CE9PT7B1CE9PT9D1CCE8PT9A0TE8PT7A1TE8PT9C1TCCD7PT5B0PCLK0_0****CD7PT6F0PCLK1_0****CD7PT9B1PCLK1_0****CD8PT5A0PCLK0_0****CD7PT6F0PCLK1_0****CD7PT9B1PCLK1_0****CD8PT5A0PCLK0_0****CD7PT6F0PCLK1_0*****CD7PT9B1PCLK1_0****CD8PT5A0PCLK0_0****CD7PT6F0PCLK1_0****CD7PT9B1PCLK1_0****CD8PT5A0PCLK0_0****CD7PT6F0TD8PT9A1TTTVC100VC0100CGND1000CGNDGND1000CGNDGND100CGNDGND100CGNDGND100CGNDGND100CGNDGND100CGNDGND100CGNDGND10GND10GND10GND10GND10GND10GND10GND10GND10GND10<	A9	PT6B	0	PCLK0_1****	С	A9	PT7D	1	PCLK1_1****	С	A9	PT10B	1	PCLK1_1****	С
E9PT980CE9PT781CE9PT901CCCE8PT940TE8PT741TE8PT901TTD7PT580PCLK0_0***CD7PT6F0PCLK1_0****CD7PT981PCLK1_0****CD8PT540CTD8PT6F0PCLK1_0****CD7PT981PCLK1_0****CD8PT540CTD8PT6F0PCLK1_0****CD7PT981PCLK1_0****CD8PT540CTD8PT6F0PCLK1_0****CD7PT981PCLK1_0****CD8PT540CTD8PT6F0CTD8PT941TTC0VCC100VC100VC100VC100VC100VC100VC1	A10	PT6A	0		Т	A10	PT7C	1		Т	A10	PT10A	1		Т
E8PT9A0TE8PT7A1TE8PT3C1PT3C1PT3C1PCLK1_0****CD7PT3B0PCLK0_0****CD7PT6F0PCLK1_0****CD7PT9B1PCLK1_0****CD8PT3A0CTD8PT6E0PCLK1_0****D8PT9A1PCLK1_0****CD8PT3A0CTD8PT6E0CD7D781PCLK1_0****CVCC00VCC000CCD7VC100VCC100VC100<	E9	PT9B	0		С	E9	PT7B	1		С	E9	PT9D	1		С
D7PT5B0PCLK0_0****CD7PT6F0PCLK1_0****CD7PT9B1PCLK1_0****CD8PT5A0TD8TD8PT6E0TD8PT9A1TTVCC100VCC1000VCC100VCC100VCC1000VCC100VCC100VCC1000VCC1000TTGNDGND000CGNDGND00CGNDGND0CCCG8PT4F0CCCRPT6D0CCCRPT6D0CCB8PT4E0CCCRPT6D0CCCRPT6C0CCRTRA8VCCAUX-TB8PT6C0CCA8VCCAUX-CA8VCCAUX-CCA7PT4D0CA8VCCAUX-CA8VCCAUX-CCCTCCA6PT4C0CA7PT6B0CCA7PT7D0CCCA7PT4D0CA7PT6B0CCA7PT7D0CCCA6PT4C0TA6PT6C0TA6PT7D0CT	E8	PT9A	0		Т	E8	PT7A	1		Т	E8	PT9C	1		Т
D8PT5A0TD8PT6E0TD8PT9A1ITTVCCIO0 <td>D7</td> <td>PT5B</td> <td>0</td> <td>PCLK0_0****</td> <td>С</td> <td>D7</td> <td>PT6F</td> <td>0</td> <td>PCLK1_0****</td> <td>С</td> <td>D7</td> <td>PT9B</td> <td>1</td> <td>PCLK1_0****</td> <td>С</td>	D7	PT5B	0	PCLK0_0****	С	D7	PT6F	0	PCLK1_0****	С	D7	PT9B	1	PCLK1_0****	С
VCCIO0VCCIO0VCCIO0VCCIO0VCCIO0VCCIO0VCCIO0VCCIO0VCCIO0VCCIO00GNDGNDIO00GNDIO00GNDIO00GNDIO000 <td< td=""><td>D8</td><td>PT5A</td><td>0</td><td></td><td>Т</td><td>D8</td><td>PT6E</td><td>0</td><td></td><td>Т</td><td>D8</td><td>PT9A</td><td>1</td><td></td><td>Т</td></td<>	D8	PT5A	0		Т	D8	PT6E	0		Т	D8	PT9A	1		Т
GNDGND0GNDGNDGND/O0GND/O0GND/O00C8PT4F0CC8PT6D0CC8PT8D0CCB8PT4E0TB8PT6C0TB8PT8C0TTA8VCCAUX-A8VCCAUX-A8VCCAUX-CA7PT7D0CA6PT4C0CA7PT6B0CA7PT7D0CCA6PT4C0CA7PT6B0CA7PT7D0CCA6PT4C0CA7PT6B0CA7PT7D0CCA6PT4C0CA7PT6B0CA7PT7D0CCA6PT4C0CA7PT6B0CA7PT7D0CCA6PT4A0CB7PT5F0CB7PT7B0CCB6PT4A0CB6PT5C0TB6PT7A0CTC6PT3C0CC7PT5D0CC7PT6B0CCA5PT3E0CC7PT5A0CCA4PT6D0CCA4PT3F0C <td>VCCIO0</td> <td>VCCIO0</td> <td>0</td> <td></td> <td></td> <td>VCCIO0</td> <td>VCCIO0</td> <td>0</td> <td></td> <td></td> <td>VCCIO0</td> <td>VCCIO0</td> <td>0</td> <td></td> <td></td>	VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0		
C8PT4F0CC8PT6D0CC8PT8D0CCB8PT4E0TB8PT6C0TB8PT8C0TTA8VCCAUX-A8VCCAUX-A8VCCAUX-A8VCCAUX-A7PT4D0CA7PT6B0CA7PT7D0CCA6PT4C0CA7PT6B0CA7PT7D0CCA6PT4C0CA7PT6B0CA7PT7D0CCA6PT4C0CA7PT6B0CA7PT7D0CCA6PT4C0CA7PT6B0CA7PT7D0CCA6PT4C0CA7PT6B0CA7PT7D0CCA6PT4C0CB7PT5F0CB7PT7D0CCB6PT4A0CTB6PT5C0TB6PT7A0CTC6PT3C0CC7PT5D0CCC7PT6B0CCA5PT3E0CCCPT5D0CCA4PT6D0CTA4PT3F0<	GND	GNDIO0	0			GND	GNDIO0	0			GND	GNDIO0	0		
B8PT4E0TB8PT6C0TB8PT8C0TA8VCCAUX-A8VCCAUX-A8VCCAUX-A8VCCAUX-A7PT4D0CA7PT6B0CA7PT7D0CCA6PT4C0TA6PT6A0TA6PT7C0CTB7PT4B0CB7PT5F0CB7PT7B0CTB6PT4A0CB7PT5F0CB7PT7B0CCB6PT4A0CB7PT5F0CB7PT7B0CTC6PT4A0CB7PT5F0CB7PT7B0CTC6PT4A0CTC6PT5C0TB6PT7A0CTC6PT3C0CC7PT5D0CC7PT6B0CCA5PT3E0CC7PT5A0CA4PT6D0CTA4PT3F0CA4PT5B0CA4PT6D0CTA4PT3F0CA4PT5B0CA4PT6D0CTE6NCVE6PT4D0 <td< td=""><td>C8</td><td>PT4F</td><td>0</td><td></td><td>С</td><td>C8</td><td>PT6D</td><td>0</td><td></td><td>С</td><td>C8</td><td>PT8D</td><td>0</td><td></td><td>С</td></td<>	C8	PT4F	0		С	C8	PT6D	0		С	C8	PT8D	0		С
A8VCCAUX-AA6PT4C0TA6PT60TA6PT70CCCTA8PT30CA8PT30CTA8PT40TA8PT40TA8PT40CTA8PT40CTA8PT30CCA7PT30CTA5PT60CA7PT30CCA8PT60CCA8PT60CA8PT60C <t< td=""><td>B8</td><td>PT4E</td><td>0</td><td></td><td>Т</td><td>B8</td><td>PT6C</td><td>0</td><td></td><td>Т</td><td>B8</td><td>PT8C</td><td>0</td><td></td><td>Т</td></t<>	B8	PT4E	0		Т	B8	PT6C	0		Т	B8	PT8C	0		Т
A7PT4D0CA7PT6B0CA7PT7D0CCA6PT4C0TA6PT6A0TA6PT7C0TTB7PT4B0CB7PT5F0CB7PT7B0CTB6PT4A0TB6PT5E0CB7PT7B0CCB6PT4A0TB6PT5E0TB6PT7A0TTC6PT3C0TC6PT5C0TC6PT6A0TTC7PT3D0CC7PT5D0CC7PT6B0CTA5PT3E0TA5PT3E0CA4PT6B0CTA4PT3F0CA4PT5B0CA4PT6D0CTE6NCLE6PT4D0CE6PT6F0CC	A8	VCCAUX	-			A8	VCCAUX	-			A8	VCCAUX	-		
A6PT4C0TA6PT6A0TA6PT7C0TTB7PT4B0CB7PT5F0CB7PT7B0CCB6PT4A0TB6PT5E0TB6PT7A0TCB6PT3C0TB6PT5C0TB6PT7A0TTC6PT3C0TC6PT5C0TC6PT6A0TTC7PT3D0CC7PT5D0CC7PT6B0CCA5PT3E0TA5PT3C0TA5PT6C0TCA4PT3F0CA4PT5B0CA4PT6D0TCE6NCLE6PT4D0CE6PT6F0CC	A7	PT4D	0		С	A7	PT6B	0		С	A7	PT7D	0		С
B7PT4B0CB7PT5F0CB7PT7B0CCB6PT4A0TB6PT5E0TB6PT7A0TTC6PT3C0TC6PT5C0TC6PT6A0TTC7PT3D0CC7PT5D0CC7PT6A0CTA5PT3E0CC7PT5A0CCC7PT6A0CA4PT3F0CA4PT5B0CA4PT6D0CTE6NCLE6PT4D0CE6PT6F0CC	A6	PT4C	0		Т	A6	PT6A	0		Т	A6	PT7C	0		Т
B6PT4A0TB6PT5E0TB6PT7A0TTC6PT3C0TC6PT5C0TC6PT6A0TTC7PT3D0CC7PT5D0CC7PT6B0CCA5PT3E0TA5PT5A0TA5PT6C0CTA4PT3F0CA4PT5B0CA4PT6D0CCE7NCLE6PT4D0CE6PT6F0CC	B7	PT4B	0		С	B7	PT5F	0		С	B7	PT7B	0		С
C6 PT3C 0 T C6 PT5C 0 T C6 PT6A 0 T C7 PT3D 0 C C7 PT3D 0 C C7 PT6B 0 C C A5 PT3E 0 T A5 PT5A 0 T A5 PT6C 0 C C A4 PT3F 0 C A4 PT5B 0 C A4 PT6D 0 C C E7 NC C E7 PT4C 0 T E7 PT6E 0 T E6 NC L E6 PT4D 0 C E6 PT6F 0 C C	B6	PT4A	0		т	B6	PT5E	0		Т	B6	PT7A	0		Т
C7 PT3D 0 C C7 PT5D 0 C C7 PT6B 0 C C A5 PT3E 0 T A5 PT5A 0 T A5 PT6C 0 T A5 A4 PT3F 0 C A4 PT5B 0 C A4 PT6C 0 T A7 NC C C A4 PT5B 0 C A4 PT6C 0 C C E7 NC C E7 PT4C 0 T E7 PT6E 0 T E6 NC E6 PT4D 0 C E6 PT6F 0 C C	C6	PT3C	0		т	C6	PT5C	0		Т	C6	PT6A	0		Т
A5 PT3E 0 T A5 PT3C 0 T A5 PT6C 0 T A4 PT3F 0 C A4 PT5B 0 C A4 PT6D 0 C T A4 PT3F 0 C A4 PT5B 0 C A4 PT6D 0 C E7 NC C E6 PT4C 0 T E7 PT6C 0 T E6 NC L E6 PT4D 0 C E6 PT6F 0 C C	C7	PT3D	0		С	C7	PT5D	0		С	C7	PT6B	0		С
A4 PT3F 0 C A4 PT5B 0 C A4 PT6D 0 C E7 NC E7 PT4C 0 T E7 PT6E 0 T E6 NC E6 PT4D 0 C E6 PT6F 0 C	A5	PT3E	0		т	A5	PT5A	0		Т	A5	PT6C	0		Т
E7 NC E7 PT4C 0 T E7 PT6E 0 T E6 NC E6 PT4D 0 C E6 PT6F 0 C	A4	PT3F	0		С	A4	PT5B	0		С	A4	PT6D	0		С
E6 NC E6 PT4D 0 C E6 PT6F 0 C	E7	NC				E7	PT4C	0		Т	E7	PT6E	0		Т
	E6	NC				E6	PT4D	0		С	E6	PT6F	0		С
B5 PT3B 0 C B5 PT3F 0 C B5 PT5D 0 C	B5	PT3B	0		С	B5	PT3F	0		С	B5	PT5D	0		С
B4 PT3A 0 T B4 PT3E 0 T B4 PT5C 0 T	B4	РТЗА	0		Т	B4	PT3E	0		Т	B4	PT5C	0		Т
D5 PT2D 0 C D5 PT3D 0 C D5 PT5B 0 C	D5	PT2D	0		С	D5	PT3D	0		С	D5	PT5B	0		С
D6 PT2C 0 T D6 PT3C 0 T D6 PT5A 0 T	D6	PT2C	0		Т	D6	PT3C	0		Т	D6	PT5A	0		Т
C4 PT2E 0 T C4 PT4A 0 T C4 PT4A 0 T	C4	PT2E	0		Т	C4	PT4A	0		Т	C4	PT4A	0		Т
C5 PT2F 0 C C5 PT4B 0 C C5 PT4B 0 C	C5	PT2F	0		С	C5	PT4B	0		С	C5	PT4B	0		С
GND GND -	-	-	-			-	-	-			GND	GND	-		
D4 NC D4 PT2D 0 C D4 PT3D 0 C	D4	NC				D4	PT2D	0		С	D4	PT3D	0		С
D3 NC D3 PT2C 0 T D3 PT3C 0 T	D3	NC				D3	PT2C	0		Т	D3	PT3C	0		Т

LA-MachXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

LAMXO2280										
Ball Number	Ball Function	Bank	Dual Function	Differential						
G2	PL11A	6		T*						
H2	PL11B	6		C*						
L3	PL11C	6		Т						
L5	PL11D	6		С						
H1	PL12A	6		Τ*						
VCCIO6	VCCIO6	6								
GND	GNDIO6	6								
J2	PL12B	6		C*						
L4	PL12C	6		Т						
L6	PL12D	6		С						
K2	PL13A	6		Τ*						
K1	PL13B	6		C*						
J1	PL13C	6		Т						
VCC	VCC	-								
L2	PL13D	6		С						
M5	PL14D	6		С						
M3	PL14C	6	TSALL	Т						
L1	PL14B	6		C*						
M2	PL14A	6		Τ*						
M1	PL15A	6		Τ*						
N1	PL15B	6		C*						
M6	PL15C	6		Т						
M4	PL15D	6		С						
VCCIO6	VCCIO6	6								
GND	GNDIO6	6								
P1	PL16A	6		Τ*						
P2	PL16B	6		C*						
N3	PL16C	6		Т						
N4	PL16D	6		С						
GND	GND	-								
T1	PL17A	6	LLM0_PLLT_FB_A	Τ*						
R1	PL17B	6	LLM0_PLLC_FB_A	C*						
P3	PL17C	6		Т						
N5	PL17D	6		С						
R3	PL18A	6	LLM0_PLLT_IN_A	T*						
R2	PL18B	6	LLM0_PLLC_IN_A	C*						
P4	PL19A	6		Т						
N6	PL19B	6		С						
U1	PL20A	6		Т						
VCCIO6	VCCIO6	6								
GND	GNDIO6	6								
GND	GNDIO5	5								
VCCIO5	VCCIO5	5								

LA-MachXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

LAMXO2280										
Ball Number	Ball Function	Bank	Dual Function	Differential						
E13	PT16D	1		С						
C15	PT16C	1		Т						
F13	PT16B	1		С						
D14	PT16A	1		Т						
A18	PT15D	1		С						
B17	PT15C	1		Т						
A16	PT15B	1		С						
A17	PT15A	1		Т						
VCC	VCC	-								
D13	PT14D	1		С						
F12	PT14C	1		Т						
C14	PT14B	1		С						
E12	PT14A	1		Т						
C13	PT13D	1		С						
B16	PT13C	1		Т						
B15	PT13B	1		С						
A15	PT13A	1		Т						
VCCIO1	VCCIO1	1								
GND	GNDIO1	1								
B14	PT12F	1		С						
A14	PT12E	1		Т						
D12	PT12D	1		С						
F11	PT12C	1		Т						
B13	PT12B	1		С						
A13	PT12A	1		Т						
C12	PT11D	1		С						
GND	GND	-								
B12	PT11C	1		Т						
E11	PT11B	1		С						
D11	PT11A	1		Т						
C11	PT10F	1		С						
A12	PT10E	1		Т						
VCCIO1	VCCIO1	1								
GND	GNDIO1	1								
F10	PT10D	1		С						
D10	PT10C	1		Т						
B11	PT10B	1	PCLK1_1***	С						
A11	PT10A	1		Т						
E10	PT9D	1		С						
C10	PT9C	1		Т						
D9	PT9B	1	PCLK1_0***	С						
E9	PT9A	1		Т						
B10	PT8F	0		С						

LA-MachXO2280 Logic Signal Connections: 324 ftBGA (Cont.)

LAMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
G8	VCCIO0	0		
G7	VCCIO0	0		

* Supports true LVDS outputs.

** Primary clock inputs are single-ended.



Lattice LA-MachXO Automotive Family Data Sheet Supplemental Information

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For Further Information

A variety of technical notes for the LA-MachXO family are available on the Lattice web site at www.latticesemi.com.

- MachXO sysIO Usage Guide (TN1091)
- MachXO sysCLOCK PLL Design and Usage Guide (TN1089)
- MachXO Memory Usage Guide (TN1092)
- Power Estimation and Management for MachXO Devices (TN1090)
- MachXO JTAG Programming and Configuration User's Guide (TN1086)
- Minimizing System Interruption During Configuration Using TransFR Technology (TN1087)
- MachXO Density Migration (TN1097)
- IEEE 1149.1 Boundary Scan Testability in Lattice Devices

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS): <u>www.jedec.org</u>
- PCI: www.pcisig.com

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