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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

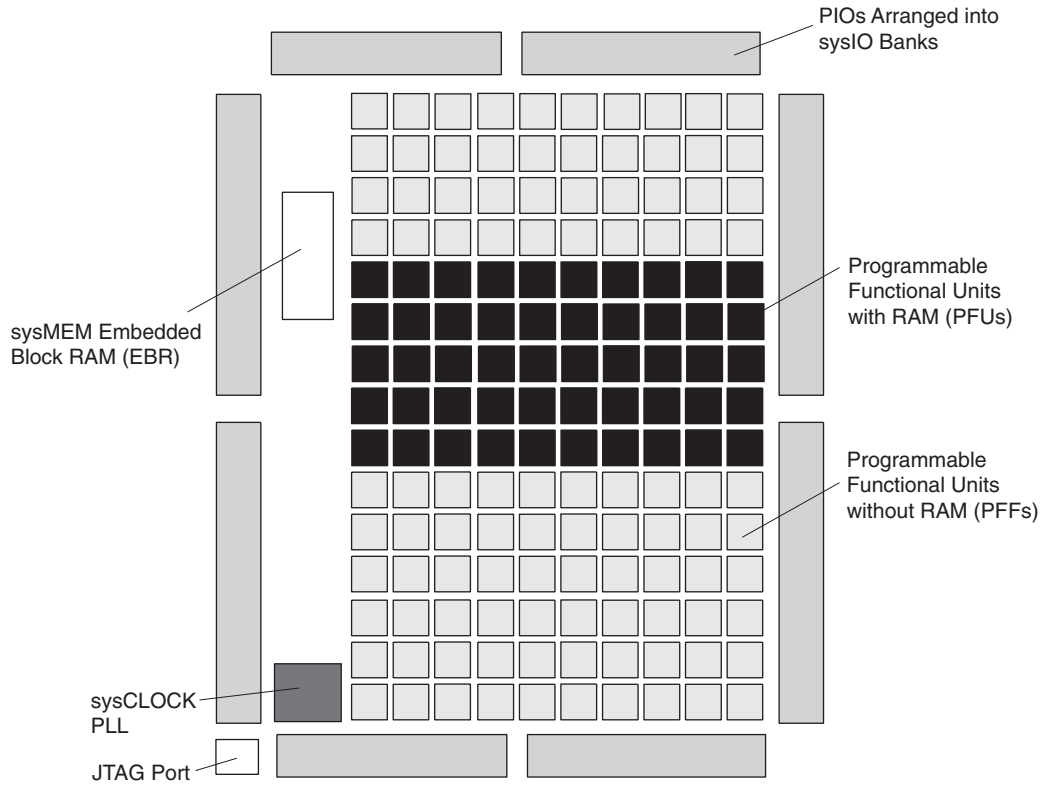
Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

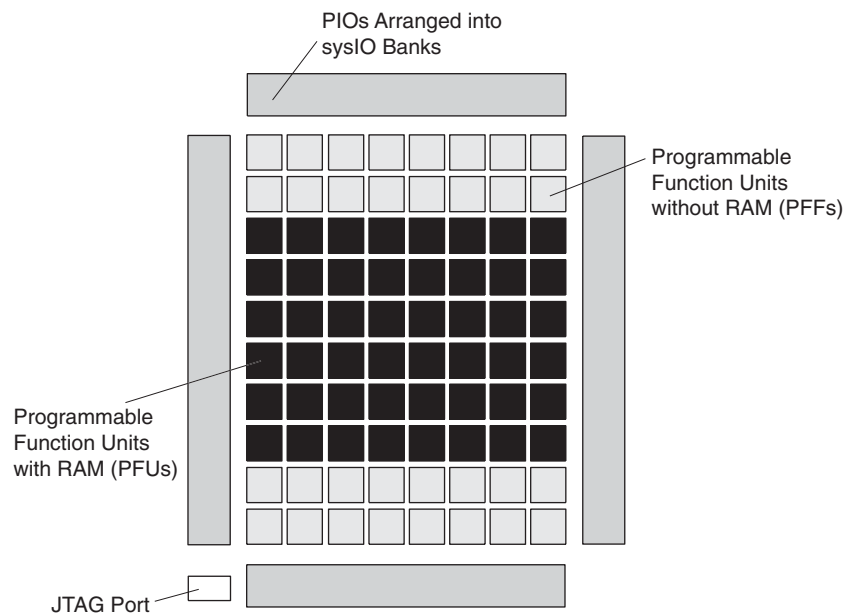
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	4.9 ns
Voltage Supply - Internal	1.14V ~ 1.26V
Number of Logic Elements/Blocks	-
Number of Macrocells	320
Number of Gates	-
Number of I/O	74
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lamxo640e-3tn100e">https://www.e-xfl.com/product-detail/lattice-semiconductor/lamxo640e-3tn100e</a>

Figure 2-1. Top View of the LA-MachXO1200 Device<sup>1</sup>



1. Top view of the LA-MachXO2280 device is similar but with higher LUT count, two PLLs, and three EBR blocks.

Figure 2-2. Top View of the LA-MachXO640 Device

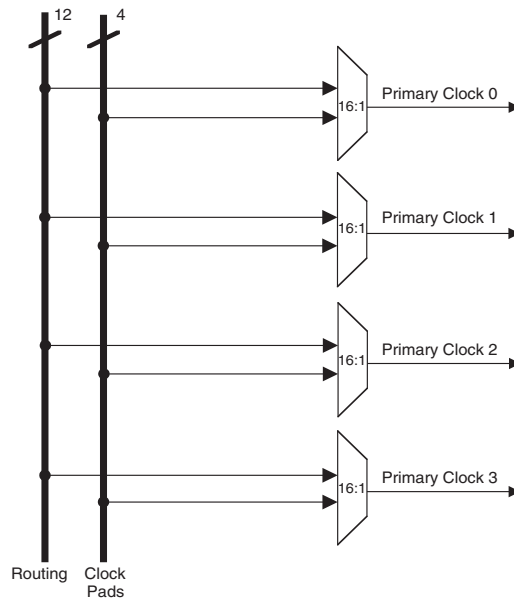


The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

### Clock/Control Distribution Network

The LA-MachXO automotive family of devices provides global signals that are available to all PFUs. These signals consist of four primary clocks and four secondary clocks. Primary clock signals are generated from four 16:1 muxes as shown in Figure 2-7 and Figure 2-8. The available clock sources for the LA-MachXO256 and LA-MachXO640 devices are four dual function clock pins and 12 internal routing signals. The available clock sources for the LA-MachXO1200 and LA-MachXO2280 devices are four dual function clock pins, up to nine internal routing signals and up to six PLL outputs.

Figure 2-7. Primary Clocks for LA-MachXO256 and LA-MachXO640 Devices



**Table 2-5. PLL Signal Descriptions**

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from PLL output, clock net, routing/external pin or internal feedback from CLKINTFB port
RST	I	“1” to reset the input clock divider
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (No phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
LOCK	O	“1” indicates PLL LOCK to CLKI
CLKINTFB	O	Internal feedback source, CLKOP divider output before CLOKRTREE
DDAMODE	I	Dynamic Delay Enable. “1”: Pin control (dynamic), “0”: Fuse Control (static)
DDAIZR	I	Dynamic Delay Zero. “1”: delay = 0, “0”: delay = on
DDAILAG	I	Dynamic Delay Lag/Lead. “1”: Lag, “0”: Lead
DDAIDEL[2:0]	I	Dynamic Delay Input

For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

## sysMEM Memory

The LA-MachXO1200 and LA-MachXO2280 devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

### sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-6.

**Table 2-6. sysMEM Block Configurations**

Memory Mode	Configurations
Single Port	8,192 x 1
	4,096 x 2
	2,048 x 4
	1,024 x 9
	512 x 18
	256 x 36
True Dual Port	8,192 x 1
	4,096 x 2
	2,048 x 4
	1,024 x 9
	512 x 18
Pseudo Dual Port	8,192 x 1
	4,096 x 2
	2,048 x 4
	1,024 x 9
	512 x 18
	256 x 36
FIFO	8,192 x 1
	4,096 x 2
	2,048 x 4
	1,024 x 9
	512 x 18
	256 x 36

Table 2-10. Supported Output Standards

Output Standard	Drive	V <sub>CCIO</sub> (Typ.)
<b>Single-ended Interfaces</b>		
LVTTTL	4mA, 8mA, 12mA, 16mA	3.3
LVC MOS33	4mA, 8mA, 12mA, 14mA	3.3
LVC MOS25	4mA, 8mA, 12mA, 14mA	2.5
LVC MOS18	4mA, 8mA, 12mA, 14mA	1.8
LVC MOS15	4mA, 8mA	1.5
LVC MOS12	2mA, 6mA	1.2
LVC MOS33, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVC MOS25, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVC MOS18, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVC MOS15, Open Drain	4mA, 8mA	—
LVC MOS12, Open Drain	2mA, 6mA	—
PCI33 <sup>3</sup>	N/A	3.3
<b>Differential Interfaces</b>		
LVDS <sup>1,2</sup>	N/A	2.5
BLVDS, RS DS <sup>2</sup>	N/A	2.5
LVPECL <sup>2</sup>	N/A	3.3

1. LA-MachXO1200 and LA-MachXO2280 devices have dedicated LVDS buffers.
2. These interfaces can be emulated with external resistors in all devices.
3. Top Banks of LA-MachXO1200 and LA-MachXO2280 devices only.

## sysIO Buffer Banks

The number of Banks vary between the devices of this family. Eight Banks surround the two larger devices, the LA-MachXO1200 and LA-MachXO2280 (two Banks per side). The LA-MachXO640 has four Banks (one Bank per side). The smallest member of this family, the LA-MachXO256, has only two Banks.

Each sysIO buffer Bank is capable of supporting multiple I/O standards. Each Bank has its own I/O supply voltage (V<sub>CCIO</sub>) which allows it to be completely independent from the other Banks. Figure 2-18, Figure 2-18, Figure 2-20 and Figure 2-21 shows the sysIO Banks and their associated supplies for all devices.

Figure 2-20. LA-MachXO640 Banks

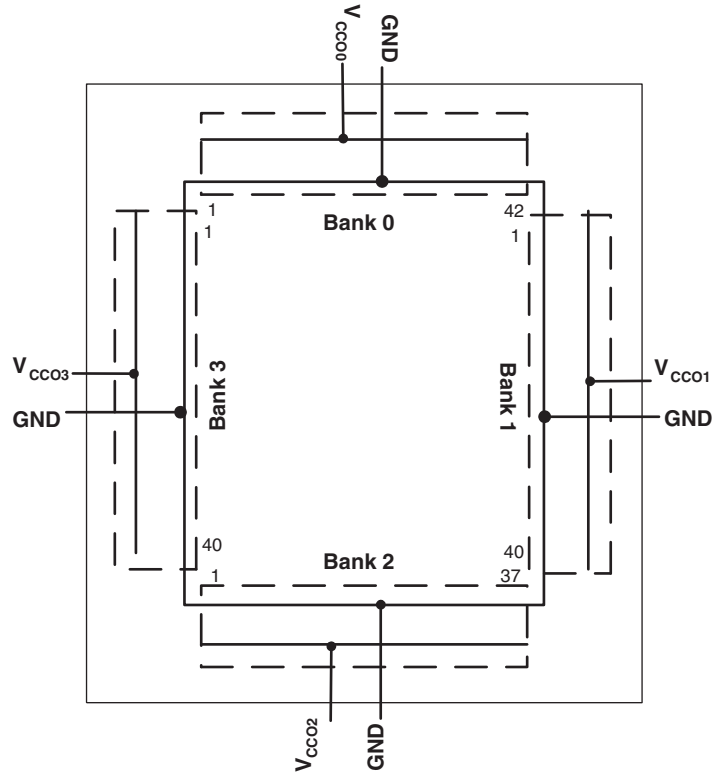
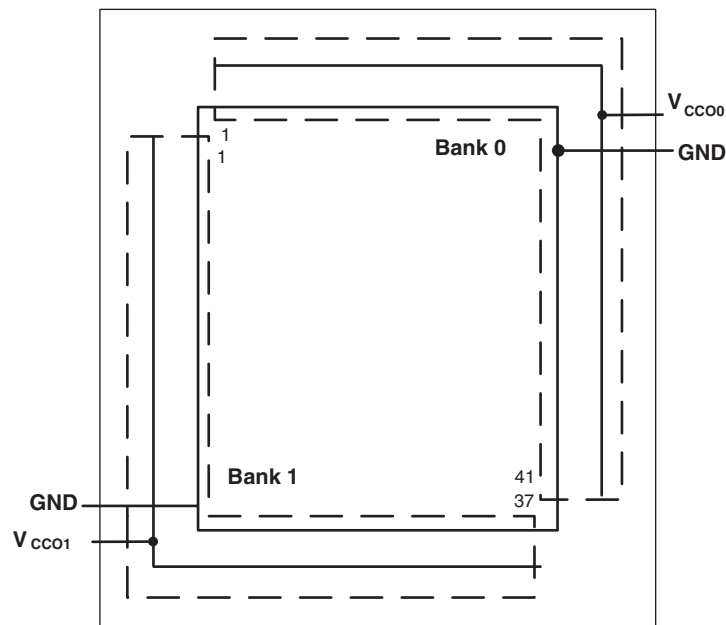


Figure 2-21. LA-MachXO256 Banks



## Hot Socketing

The LA-MachXO automotive devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration

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## Device Configuration

All LA-MachXO devices contain a test access port that can be used for device configuration and programming.

The non-volatile memory in the LA-MachXO can be configured in two different modes:

- In IEEE 1532 mode via the IEEE 1149.1 port. In this mode, the device is off-line and I/Os are controlled by BSCAN registers.
- In background mode via the IEEE 1149.1 port. This allows the device to remain operational in user mode while reprogramming takes place.

The SRAM configuration memory can be configured in three different ways:

- At power-up via the on-chip non-volatile memory.
- After a refresh command is issued via the IEEE 1149.1 port.
- In IEEE 1532 mode via the IEEE 1149.1 port.

Figure 2-22 provides a pictorial representation of the different programming modes available in the LA-MachXO devices. On power-up, the SRAM is ready to be configured with IEEE 1149.1 serial TAP port using IEEE 1532 protocols.

### Leave Alone I/O

When using IEEE 1532 mode for non-volatile memory programming, SRAM configuration, or issuing a refresh command, users may specify I/Os as high, low, tristated or held at current value. This provides excellent flexibility for implementing systems where reconfiguration or reprogramming occurs on-the-fly.

### TransFR (Transparent Field Reconfiguration)

TransFR (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. See Lattice technical note #TN1087, *Minimizing System Interruption During Configuration Using TransFR Technology*, for details.

### Security

The LA-MachXO automotive devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile memory spaces. Once set, the only way to clear the security bits is to erase the memory space.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

## AEC-Q100 Tested and Qualified

The Automotive Electronics Council (AEC) consists of two committees: the Quality Systems Committee and the Component Technical Committee. These committees are composed of representatives from sustaining and other associate members. The AEC Component Technical Committee is the standardization body for establishing standards for reliable, high quality electronic components. In particular, the AEC-Q100 specification “Stress Test for Qualification for Integrated Circuits” defines qualification and re-qualification requirements for electronic components. Components meeting these specifications are suitable for use in the harsh automotive environment without additional component-level qualification testing. Lattice's LA-ispMACH 4000V and LA-MachXO devices completed and passed the requirements of the AEC-Q100 specification.

### Supply Current (Sleep Mode)<sup>1, 2</sup>

Symbol	Parameter	Device	Typ. <sup>3</sup>	Max.	Units
I <sub>CC</sub>	Core Power Supply	LCMXO256C	12	25	μA
		LCMXO640C	12	25	μA
I <sub>CCAUX</sub>	Auxiliary Power Supply	LCMXO256C	1	15	μA
		LCMXO640C	1	25	μA
I <sub>CCIO</sub>	Bank Power Supply <sup>4</sup>	All LCMXO 'C' Devices	2	30	μA

1. Assumes all inputs are configured as LVCMOS and held at the V<sub>CCIO</sub> or GND.
2. Frequency = 0MHz.
3. T<sub>A</sub> = 25°C, power supplies at nominal voltage.
4. Per Bank.

### Supply Current (Standby)<sup>1, 2, 3, 4</sup>

#### Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. <sup>5</sup>	Units
I <sub>CC</sub>	Core Power Supply	LCMXO256C	7	mA
		LCMXO640C	9	mA
		LCMXO256E	4	mA
		LCMXO640E	6	mA
		LCMXO1200E	10	mA
		LCMXO2280E	12	mA
I <sub>CCAUX</sub>	Auxiliary Power Supply V <sub>CCAUX</sub> = 3.3V	LCMXO256E/C	5	mA
		LCMXO640E/C	7	mA
		LCMXO1200E	12	mA
		LCMXO2280E	13	mA
I <sub>CCIO</sub>	Bank Power Supply <sup>6</sup>	All devices	2	mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at V<sub>CCIO</sub> or GND.
3. Frequency = 0MHz.
4. User pattern = blank.
5. T<sub>J</sub> = 25°C, power supplies at nominal voltage.
6. Per Bank. V<sub>CCIO</sub> = 2.5V. Does not include pull-up/pull-down.



**sysIO Single-Ended DC Electrical Characteristics**

Input/Output Standard	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub> Max. (V)	V <sub>OH</sub> Min. (V)	I <sub>OL</sub> <sup>1</sup> (mA)	I <sub>OH</sub> <sup>1</sup> (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V <sub>CCIO</sub> - 0.4	16, 12, 8, 4	-14, -12, -8, -4
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
LVTTTL	-0.3	0.8	2.0	3.6	0.4	2.4	16	-16
					0.4	V <sub>CCIO</sub> - 0.4	12, 8, 4	-12, -8, -4
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V <sub>CCIO</sub> - 0.4	16, 12, 8, 4	-14, -12, -8, -4
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	0.35V <sub>CCIO</sub>	0.65V <sub>CCIO</sub>	3.6	0.4	V <sub>CCIO</sub> - 0.4	16, 12, 8, 4	-14, -12, -8, -4
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	0.35V <sub>CCIO</sub>	0.65V <sub>CCIO</sub>	3.6	0.4	V <sub>CCIO</sub> - 0.4	8, 4	-8, -4
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
LVCMOS 1.2 ("C" Version)	-0.3	0.42	0.78	3.6	0.4	V <sub>CCIO</sub> - 0.4	6, 2	-6, -2
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
LVCMOS 1.2 ("E" Version)	-0.3	0.35V <sub>CC</sub>	0.65V <sub>CC</sub>	3.6	0.4	V <sub>CCIO</sub> - 0.4	6, 2	-6, -2
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
PCI	-0.3	0.3V <sub>CCIO</sub>	0.5V <sub>CCIO</sub>	3.6	0.1V <sub>CCIO</sub>	0.9V <sub>CCIO</sub>	1.5	-0.5

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O Bank and the end of an I/O Bank, as shown in the logic signal connections table shall not exceed n \* 8mA. Where n is the number of I/Os between Bank GND connections or between the last GND in a Bank and the end of a Bank.

**LA-MachXO External Switching Characteristics<sup>1</sup>**

Over Recommended Operating Conditions

Parameter	Description	Device	-3		Units
			Min.	Max.	
<b>General I/O Pin Parameters (Using Global Clock without PLL)<sup>1</sup></b>					
t <sub>PD</sub>	Best Case t <sub>PD</sub> Through 1 LUT	LCMXO256	—	4.9	ns
		LCMXO640	—	4.9	ns
		LCMXO1200	—	5.1	ns
		LCMXO2280	—	5.1	ns
t <sub>CO</sub>	Best Case Clock to Output - From PFU	LCMXO256	—	5.6	ns
		LCMXO640	—	5.7	ns
		LCMXO1200	—	6.1	ns
		LCMXO2280	—	6.1	ns
t <sub>SU</sub>	Clock to Data Setup - To PFU	LCMXO256	1.8	—	ns
		LCMXO640	1.5	—	ns
		LCMXO1200	1.6	—	ns
		LCMXO2280	1.5	—	ns
t <sub>H</sub>	Clock to Data Hold - To PFU	LCMXO256	-0.3	—	ns
		LCMXO640	-0.1	—	ns
		LCMXO1200	0.0	—	ns
		LCMXO2280	-0.4	—	ns
f <sub>MAX_IO</sub>	Clock Frequency of I/O and PFU Register	LCMXO256	—	500	MHz
		LCMXO640	—	500	MHz
		LCMXO1200	—	500	MHz
		LCMXO2280	—	500	MHz
t <sub>SKEW_PRI</sub>	Global Clock Skew Across Device	LCMXO256	—	240	ps
		LCMXO640	—	240	ps
		LCMXO1200	—	260	ps
		LCMXO2280	—	260	ps

1. General timing numbers based on LVCMOS2.5V, 12 mA.  
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LA-MachXO Internal Timing Parameters<sup>1</sup>

Over Recommended Operating Conditions

Parameter	Description	-3		Units
		Min.	Max.	
<b>PFU/PFF Logic Mode Timing</b>				
t <sub>LUT4_PFU</sub>	LUT4 delay (A to D inputs to F output)	—	0.39	ns
t <sub>LUT6_PFU</sub>	LUT6 delay (A to D inputs to OFX output)	—	0.62	ns
t <sub>LSR_PFU</sub>	Set/Reset to output of PFU	—	1.26	ns
t <sub>SUM_PFU</sub>	Clock to Mux (M0,M1) input setup time	0.15	—	ns
t <sub>HM_PFU</sub>	Clock to Mux (M0,M1) input hold time	-0.07	—	ns
t <sub>SUD_PFU</sub>	Clock to D input setup time	0.18	—	ns
t <sub>HD_PFU</sub>	Clock to D input hold time	-0.04	—	ns
t <sub>CK2Q_PFU</sub>	Clock to Q delay, D-type register configuration	—	0.56	ns
t <sub>LE2Q_PFU</sub>	Clock to Q delay latch configuration	—	0.74	ns
t <sub>LD2Q_PFU</sub>	D to Q throughput delay when latch is enabled	—	0.77	ns
<b>PFU Dual Port Memory Mode Timing</b>				
t <sub>CORAM_PFU</sub>	Clock to Output	—	0.56	ns
t <sub>SUDATA_PFU</sub>	Data Setup Time	-0.25	—	ns
t <sub>HDATA_PFU</sub>	Data Hold Time	0.39	—	ns
t <sub>SUADDR_PFU</sub>	Address Setup Time	-0.65	—	ns
t <sub>HADDR_PFU</sub>	Address Hold Time	0.99	—	ns
t <sub>SUWREN_PFU</sub>	Write/Read Enable Setup Time	-0.30	—	ns
t <sub>HWREN_PFU</sub>	Write/Read Enable Hold Time	0.47	—	ns
<b>PIO Input/Output Buffer Timing</b>				
t <sub>IN_PIO</sub>	Input Buffer Delay	—	1.06	ns
t <sub>OUT_PIO</sub>	Output Buffer Delay	—	1.80	ns
<b>EBR Timing (1200 and 2280 Devices Only)</b>				
t <sub>CO_EBR</sub>	Clock to output from Address or Data with no output register	—	3.14	ns
t <sub>COO_EBR</sub>	Clock to output from EBR output Register	—	0.75	ns
t <sub>SUDATA_EBR</sub>	Setup Data to EBR Memory	-0.37	—	ns
t <sub>HDATA_EBR</sub>	Hold Data to EBR Memory	0.57	—	ns
t <sub>SUADDR_EBR</sub>	Setup Address to EBR Memory	-0.37	—	ns
t <sub>HADDR_EBR</sub>	Hold Address to EBR Memory	0.57	—	ns
t <sub>SUWREN_EBR</sub>	Setup Write/Read Enable to EBR Memory	-0.23	—	ns
t <sub>HWREN_EBR</sub>	Hold Write/Read Enable to EBR Memory	0.36	—	ns
t <sub>SUCE_EBR</sub>	Clock Enable Setup Time to EBR Output Register	0.27	—	ns
t <sub>HCE_EBR</sub>	Clock Enable Hold Time to EBR Output Register	-0.18	—	ns
t <sub>RSTO_EBR</sub>	Reset To Output Delay Time from EBR Output Register	—	1.44	ns
<b>PLL Parameters (1200 and 2280 Devices Only)</b>				
t <sub>RSTREC</sub>	Reset Recovery to Rising Clock	—	1.00	ns
t <sub>RSTSU</sub>	Reset Signal Setup Time	1.00	—	ns

1. Internal parameters are characterized but not tested on every device.  
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**LA-MachXO Family Timing Adders<sup>1, 2, 3</sup>**

Over Recommended Operating Conditions

Buffer Type	Description	-3	Units
<b>Input Adjusters</b>			
LVDS25 <sup>4</sup>	LVDS	0.61	ns
BLVDS25 <sup>4</sup>	BLVDS	0.61	ns
LVPECL33 <sup>4</sup>	LVPECL	0.59	ns
LVTTTL33	LVTTTL	0.01	ns
LVC MOS33	LVC MOS 3.3	0.01	ns
LVC MOS25	LVC MOS 2.5	0.00	ns
LVC MOS18	LVC MOS 1.8	0.10	ns
LVC MOS15	LVC MOS 1.5	0.19	ns
LVC MOS12	LVC MOS 1.2	0.56	ns
PCI33 <sup>4</sup>	PCI	0.01	ns
<b>Output Adjusters</b>			
LVDS25E	LVDS 2.5 E	-0.18	ns
LVDS25 <sup>4</sup>	LVDS 2.5	-0.30	ns
BLVDS25	BLVDS 2.5	-0.04	ns
LVPECL33	LVPECL 3.3	0.05	ns
LVTTTL33_4mA	LVTTTL 4mA drive	0.05	ns
LVTTTL33_8mA	LVTTTL 8mA drive	0.08	ns
LVTTTL33_12mA	LVTTTL 12mA drive	-0.01	ns
LVTTTL33_16mA	LVTTTL 16mA drive	0.70	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive	0.05	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive	0.08	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive	-0.01	ns
LVC MOS33_14mA	LVC MOS 3.3 14mA drive	0.70	ns
LVC MOS25_4mA	LVC MOS 2.5 4mA drive	0.07	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive	0.13	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive	0.00	ns
LVC MOS25_14mA	LVC MOS 2.5 14mA drive	0.47	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive	0.15	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive	0.06	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive	-0.08	ns
LVC MOS18_14mA	LVC MOS 1.8 14mA drive	0.09	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive	0.22	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive	0.07	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive	0.36	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive	0.07	ns
PCI33 <sup>4</sup>	PCI33	2.59	ns

1. Timing adders are characterized but not tested on every device.

2. LVC MOS timing is measured with the load specified in Switching Test Conditions table.

3. All other standards tested according to the appropriate specifications.

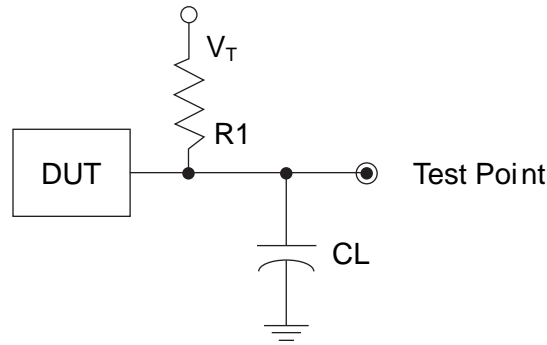
4. I/O standard only available in LCMXO1200 and LCMXO2280 devices.

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### Switching Test Conditions

Figure 3-6 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3-5.

**Figure 3-6. Output Test Load, LVTTTL and LVCMOS Standards**



**Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces**

Test Condition	R <sub>1</sub>	C <sub>L</sub>	Timing Ref.	V <sub>T</sub>
LVTTTL and LVCMOS settings (L -> H, H -> L)	∞	0pF	LVTTTL, LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = V <sub>CCIO</sub> /2	—
			LVCMOS 1.8 = V <sub>CCIO</sub> /2	—
			LVCMOS 1.5 = V <sub>CCIO</sub> /2	—
			LVCMOS 1.2 = V <sub>CCIO</sub> /2	—
LVTTTL and LVCMOS 3.3 (Z -> H)	188	0pF	1.5	V <sub>OL</sub>
LVTTTL and LVCMOS 3.3 (Z -> L)				V <sub>OH</sub>
Other LVCMOS (Z -> H)			V <sub>CCIO</sub> /2	V <sub>OL</sub>
Other LVCMOS (Z -> L)			V <sub>CCIO</sub> /2	V <sub>OH</sub>
LVTTTL + LVCMOS (H -> Z)			V <sub>OH</sub> - 0.15	V <sub>OL</sub>
LVTTTL + LVCMOS (L -> Z)			V <sub>OL</sub> - 0.15	V <sub>OH</sub>

Note: Output test conditions for all other interfaces are determined by the respective standards.

**Power Supply and NC**

Signal	100 TQFP <sup>1</sup>	144 TQFP <sup>1</sup>
VCC	LAMXO256/640: 35, 90 LAMXO1200/2280: 17, 35, 66, 91	21, 52, 93, 129
VCCIO0	LAMXO256: 60, 74, 92 LAMXO640: 80, 92 LAMXO1200/2280: 94	LAMXO640: 117, 135 LAMXO1200/2280: 135
VCCIO1	LAMXO256: 10, 24, 41 LAMXO640: 60, 74 LAMXO1200/2280: 80	LAMXO640: 82, 98 LAMXO1200/2280: 117
VCCIO2	LAMXO256: None LAMXO640: 29, 41 LAMXO1200/2280: 70	LAMXO640: 38, 63 LAMXO1200/2280: 98
VCCIO3	LAMXO256: None LAMXO640: 10, 24 LAMXO1200/2280: 56	LAMXO640: 10, 26 LAMXO1200/2280: 82
VCCIO4	LAMXO256/640: None LAMXO1200/2280: 44	LAMXO640: None LAMXO1200/2280: 63
VCCIO5	LAMXO256/640: None LAMXO1200/2280: 27	LAMXO640: None LAMXO1200/2280: 38
VCCIO6	LAMXO256/640: None LAMXO1200/2280: 20	LAMXO640: None LAMXO1200/2280: 26
VCCIO7	LAMXO256/640: None LAMXO1200/2280: 6	LAMXO640: None LAMXO1200/2280: 10
VCCAUX	LAMXO256/640: 88 LAMXO1200/2280: 36, 90	53, 128
GND <sup>2</sup>	LAMXO256: 40, 84, 62, 75, 93, 12, 25, 42 LAMXO640: 40, 84, 81, 93, 62, 75, 30, 42, 12, 25 LAMXO1200/2280: 9, 41, 59, 83, 100, 76, 50, 26	16, 59, 88, 123, 118, 136, 83, 99, 37, 64, 11, 27
NC <sup>3</sup>		

1. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.

2. All grounds must be electrically connected at the board level. For fpBGA and ftBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.

3. NC pins should not be connected to any active signals, VCC or GND.

**LA-MachXO256 and LA-MachXO640 Logic Signal Connections:  
100 TQFP (Cont.)**

Pin Number	LAMXO256				LAMXO640			
	Ball Function	Bank	Dual Function	Differential	Ball Function	Bank	Dual Function	Differential
83	PT4C	0		T	PT7A	0		
84	GND	-			GND	-		
85	PT4B	0	PCLK0_1**	C	PT6B	0	PCLK0_1**	
86	PT4A	0	PCLK0_0**	T	PT5B	0	PCLK0_0**	C
87	PT3D	0		C	PT5A	0		T
88	VCCAUX	-			VCCAUX	-		
89	PT3C	0		T	PT4F	0		
90	VCC	-			VCC	-		
91	PT3B	0		C	PT3F	0		
92	VCCIO0	0			VCCIO0	0		
93	GNDIO0	0			GNDIO0	0		
94	PT3A	0		T	PT3B	0		C
95	PT2F	0		C	PT3A	0		T
96	PT2E	0		T	PT2F	0		C
97	PT2D	0		C	PT2E	0		T
98	PT2C	0		T	PT2B	0		C
99	PT2B	0		C	PT2C	0		
100	PT2A	0		T	PT2A	0		T

\* NC for "E" devices.

\*\* Primary clock inputs are single-ended.

**LA-MachXO640, LA-MachXO1200 and LA-MachXO2280 Logic Signal Connections: 256 ftBGA (Cont.)**

LAMXO640					LAMXO1200					LAMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
J4	PL8A	3		T	J4	PL13A	6		T**	J4	PL16A	6		T**
J5	PL8B	3		C	J5	PL13B	6		C**	J5	PL16B	6		C**
R1	PL11A	3		T	R1	PL13C	6		T	R1	PL16C	6		T
R2	PL11B	3		C	R2	PL13D	6		C	R2	PL16D	6		C
-	-	-			-	-	-			GND	GND	-		
K5	NC				K5	PL14A	6	LLM0_PLLT_FB_A	T**	K5	PL17A	6	LLM0_PLLT_FB_A	T**
K4	NC				K4	PL14B	6	LLM0_PLLC_FB_A	C**	K4	PL17B	6	LLM0_PLLC_FB_A	C**
L5	PL10C	3		T	L5	PL14C	6		T	L5	PL17C	6		T
L4	PL10D	3		C	L4	PL14D	6		C	L4	PL17D	6		C
M5	NC				M5	PL15A	6	LLM0_PLLT_IN_A	T**	M5	PL18A	6	LLM0_PLLT_IN_A	T**
M4	NC				M4	PL15B	6	LLM0_PLLC_IN_A	C**	M4	PL18B	6	LLM0_PLLC_IN_A	C**
N4	PL11C	3		T	N4	PL16A	6		T	N4	PL19A	6		T
N3	PL11D	3		C	N3	PL16B	6		C	N3	PL19B	6		C
VCCIO3	VCCIO3	3			VCCIO6	VCCIO6	6			VCCIO6	VCCIO6	6		
GND	GNDIO3	3			GND	GNDIO6	6			GND	GNDIO6	6		
GND	GNDIO2	2			GND	GNDIO5	5			GND	GNDIO5	5		
VCCIO2	VCCIO2	2			VCCIO5	VCCIO5	5			VCCIO5	VCCIO5	5		
P4	TMS	2	TMS		P4	TMS	5	TMS		P4	TMS	5	TMS	
P2	NC				P2	PB2A	5		T	P2	PB2A	5		T
P3	NC				P3	PB2B	5		C	P3	PB2B	5		C
N5	NC				N5	PB2C	5		T	N5	PB2C	5		T
R3	TCK	2	TCK		R3	TCK	5	TCK		R3	TCK	5	TCK	
N6	NC				N6	PB2D	5		C	N6	PB2D	5		C
T2	PB2A	2		T	T2	PB3A	5		T	T2	PB3A	5		T
T3	PB2B	2		C	T3	PB3B	5		C	T3	PB3B	5		C
R4	PB2C	2		T	R4	PB3C	5		T	R4	PB3C	5		T
R5	PB2D	2		C	R5	PB3D	5		C	R5	PB3D	5		C
P5	PB3A	2		T	P5	PB4A	5		T	P5	PB4A	5		T
P6	PB3B	2		C	P6	PB4B	5		C	P6	PB4B	5		C
T5	PB3C	2		T	T5	PB4C	5		T	T5	PB4C	5		T
M6	TDO	2	TDO		M6	TDO	5	TDO		M6	TDO	5	TDO	
T4	PB3D	2		C	T4	PB4D	5		C	T4	PB4D	5		C
R6	PB4A	2		T	R6	PB5A	5		T	R6	PB5A	5		T
GND	GNDIO2	2			GND	GNDIO5	5			GND	GNDIO5	5		
VCCIO2	VCCIO2	2			VCCIO5	VCCIO5	5			VCCIO5	VCCIO5	5		
T6	PB4B	2		C	T6	PB5B	5		C	T6	PB5B	5		C
N7	TDI	2	TDI		N7	TDI	5	TDI		N7	TDI	5	TDI	
T8	PB4C	2		T	T8	PB5C	5		T	T8	PB6A	5		T
T7	PB4D	2		C	T7	PB5D	5		C	T7	PB6B	5		C
M7	NC				M7	PB6A	5		T	M7	PB7C	5		T
M8	NC				M8	PB6B	5		C	M8	PB7D	5		C
T9	VCCAUX	-			T9	VCCAUX	-			T9	VCCAUX	-		
R7	PB4E	2		T	R7	PB6C	5		T	R7	PB8C	5		T
R8	PB4F	2		C	R8	PB6D	5		C	R8	PB8D	5		C
-	-				VCCIO5	VCCIO5	5			VCCIO5	VCCIO5	5		
-	-				GND	GNDIO5	5			GND	GNDIO5	5		
P7	PB5C	2		T	P7	PB6E	5		T	P7	PB9A	4		T
P8	PB5D	2		C	P8	PB6F	5		C	P8	PB9B	4		C
N8	PB5A	2		T	N8	PB7A	4		T	N8	PB10E	4		T
N9	PB5B	2	PCLK2_1****	C	N9	PB7B	4	PCLK4_1****	C	N9	PB10F	4	PCLK4_1****	C
P10	PB7B	2		C	P10	PB7D	4		C	P10	PB10D	4		C
P9	PB7A	2		T	P9	PB7C	4		T	P9	PB10C	4		T
M9	PB6B	2	PCLK2_0****	C	M9	PB7F	4	PCLK4_0****	C	M9	PB10B	4	PCLK4_0****	C



**LA-MachXO640, LA-MachXO1200 and LA-MachXO2280 Logic Signal Connections: 256 ftBGA (Cont.)**

LAMXO640					LAMXO1200					LAMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
J13	PR8C	1		T	J13	PR11A	3		T**	J13	PR14A	3		T**
GND	GND	-			GND	GND	-			GND	GND	-		
K14	PR8B	1		C	K14	PR10D	3		C	K14	PR13D	3		C
J14	PR8A	1		T	J14	PR10C	3		T	J14	PR13C	3		T
K15	PR7D	1		C	K15	PR10B	3		C**	K15	PR13B	3		C**
J15	PR7C	1		T	J15	PR10A	3		T**	J15	PR13A	3		T**
-	-				GND	GNDIO3	3			GND	GNDIO3	3		
-	-				VCCIO3	VCCIO3	3			VCCIO3	VCCIO3	3		
K12	NC				K12	PR9D	3		C	K12	PR11D	3		C
J12	NC				J12	PR9C	3		T	J12	PR11C	3		T
J16	PR7B	1		C	J16	PR9B	3		C**	J16	PR11B	3		C**
H16	PR7A	1		T	H16	PR9A	3		T**	H16	PR11A	3		T**
H15	PR6B	1		C	H15	PR8D	2		C	H15	PR10D	2		C
G15	PR6A	1		T	G15	PR8C	2		T	G15	PR10C	2		T
H14	PR5D	1		C	H14	PR8B	2		C**	H14	PR10B	2		C**
G14	PR5C	1		T	G14	PR8A	2		T**	G14	PR10A	2		T**
GND	GNDIO1	1			GND	GNDIO2	2			GND	GNDIO2	2		
VCCIO1	VCCIO1	1			VCCIO2	VCCIO2	2			VCCIO2	VCCIO2	2		
H13	PR6D	1		C	H13	PR7D	2		C	H13	PR9D	2		C
H12	PR6C	1		T	H12	PR7C	2		T	H12	PR9C	2		T
G13	PR4D	1		C	G13	PR7B	2		C**	G13	PR9B	2		C**
G12	PR4C	1		T	G12	PR7A	2		T**	G12	PR9A	2		T**
G16	PR5B	1		C	G16	PR6D	2		C	G16	PR7D	2		C
F16	PR5A	1		T	F16	PR6C	2		T	F16	PR7C	2		T
F15	PR4B	1		C	F15	PR6B	2		C**	F15	PR7B	2		C**
E15	PR4A	1		T	E15	PR6A	2		T**	E15	PR7A	2		T**
E16	PR3B	1		C	E16	PR5D	2		C	E16	PR6D	2		C
D16	PR3A	1		T	D16	PR5C	2		T	D16	PR6C	2		T
VCCIO1	VCCIO1	1			VCCIO2	VCCIO2	2			VCCIO2	VCCIO2	2		
GND	GNDIO1	1			GND	GNDIO2	2			GND	GNDIO2	2		
D15	PR2D	1		C	D15	PR5B	2		C**	D15	PR6B	2		C**
C15	PR2C	1		T	C15	PR5A	2		T**	C15	PR6A	2		T**
C16	PR2B	1		C	C16	PR4D	2		C	C16	PR5D	2		C
B16	PR2A	1		T	B16	PR4C	2		T	B16	PR5C	2		T
F14	PR3D	1		C	F14	PR4B	2		C**	F14	PR5B	2		C**
E14	PR3C	1		T	E14	PR4A	2		T**	E14	PR5A	2		T**
-	-	-			-	-	-			GND	GND	-		
F12	NC				F12	PR3D	2		C	F12	PR4D	2		C
F13	NC				F13	PR3C	2		T	F13	PR4C	2		T
E12	NC				E12	PR3B	2		C**	E12	PR4B	2		C**
E13	NC				E13	PR3A	2		T**	E13	PR4A	2		T**
D13	NC				D13	PR2B	2		C	D13	PR3B	2		C**
D14	NC				D14	PR2A	2		T	D14	PR3A	2		T**
VCCIO0	VCCIO0	0			VCCIO2	VCCIO2	2			VCCIO2	VCCIO2	2		
GND	GNDIO0	0			GND	GNDIO2	2			GND	GNDIO2	2		
GND	GNDIO0	0			GND	GNDIO1	1			GND	GNDIO1	1		
VCCIO0	VCCIO0	0			VCCIO1	VCCIO1	1			VCCIO1	VCCIO1	1		
B15	NC				B15	PT11D	1		C	B15	PT16D	1		C
A15	NC				A15	PT11C	1		T	A15	PT16C	1		T
C14	NC				C14	PT11B	1		C	C14	PT16B	1		C
B14	NC				B14	PT11A	1		T	B14	PT16A	1		T
C13	PT9F	0		C	C13	PT10F	1		C	C13	PT15D	1		C
B13	PT9E	0		T	B13	PT10E	1		T	B13	PT15C	1		T

**LA-MachXO640, LA-MachXO1200 and LA-MachXO2280 Logic Signal Connections: 256 ftBGA (Cont.)**

LAMXO640					LAMXO1200					LAMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential	Ball Number	Ball Function	Bank	Dual Function	Differential
E11	NC				E11	PT10D	1		C	E11	PT15B	1		C
E10	NC				E10	PT10C	1		T	E10	PT15A	1		T
D12	PT9D	0		C	D12	PT10B	1		C	D12	PT14D	1		C
D11	PT9C	0		T	D11	PT10A	1		T	D11	PT14C	1		T
A14	PT7F	0		C	A14	PT9F	1		C	A14	PT14B	1		C
A13	PT7E	0		T	A13	PT9E	1		T	A13	PT14A	1		T
C12	PT8B	0		C	C12	PT9D	1		C	C12	PT13D	1		C
C11	PT8A	0		T	C11	PT9C	1		T	C11	PT13C	1		T
-	-				VCCIO1	VCCIO1	1			VCCIO1	VCCIO1	1		
-	-				GND	GNDIO1	1			GND	GNDIO1	1		
B12	PT7B	0		C	B12	PT9B	1		C	B12	PT12D	1		C
B11	PT7A	0		T	B11	PT9A	1		T	B11	PT12C	1		T
A12	PT7D	0		C	A12	PT8F	1		C	A12	PT12B	1		C
A11	PT7C	0		T	A11	PT8E	1		T	A11	PT12A	1		T
GND	GND	-			GND	GND	-			GND	GND	-		
B10	PT5D	0		C	B10	PT8D	1		C	B10	PT11B	1		C
B9	PT5C	0		T	B9	PT8C	1		T	B9	PT11A	1		T
D10	PT8D	0		C	D10	PT8B	1		C	D10	PT10F	1		C
D9	PT8C	0		T	D9	PT8A	1		T	D9	PT10E	1		T
-	-				VCCIO1	VCCIO1	1			VCCIO1	VCCIO1	1		
-	-				GND	GNDIO1	1			GND	GNDIO1	1		
C10	PT6D	0		C	C10	PT7F	1		C	C10	PT10D	1		C
C9	PT6C	0		T	C9	PT7E	1		T	C9	PT10C	1		T
A9	PT6B	0	PCLK0_1****	C	A9	PT7D	1	PCLK1_1****	C	A9	PT10B	1	PCLK1_1****	C
A10	PT6A	0		T	A10	PT7C	1		T	A10	PT10A	1		T
E9	PT9B	0		C	E9	PT7B	1		C	E9	PT9D	1		C
E8	PT9A	0		T	E8	PT7A	1		T	E8	PT9C	1		T
D7	PT5B	0	PCLK0_0****	C	D7	PT6F	0	PCLK1_0****	C	D7	PT9B	1	PCLK1_0****	C
D8	PT5A	0		T	D8	PT6E	0		T	D8	PT9A	1		T
VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0			VCCIO0	VCCIO0	0		
GND	GNDIO0	0			GND	GNDIO0	0			GND	GNDIO0	0		
C8	PT4F	0		C	C8	PT6D	0		C	C8	PT8D	0		C
B8	PT4E	0		T	B8	PT6C	0		T	B8	PT8C	0		T
A8	VCCAUX	-			A8	VCCAUX	-			A8	VCCAUX	-		
A7	PT4D	0		C	A7	PT6B	0		C	A7	PT7D	0		C
A6	PT4C	0		T	A6	PT6A	0		T	A6	PT7C	0		T
B7	PT4B	0		C	B7	PT5F	0		C	B7	PT7B	0		C
B6	PT4A	0		T	B6	PT5E	0		T	B6	PT7A	0		T
C6	PT3C	0		T	C6	PT5C	0		T	C6	PT6A	0		T
C7	PT3D	0		C	C7	PT5D	0		C	C7	PT6B	0		C
A5	PT3E	0		T	A5	PT5A	0		T	A5	PT6C	0		T
A4	PT3F	0		C	A4	PT5B	0		C	A4	PT6D	0		C
E7	NC				E7	PT4C	0		T	E7	PT6E	0		T
E6	NC				E6	PT4D	0		C	E6	PT6F	0		C
B5	PT3B	0		C	B5	PT3F	0		C	B5	PT5D	0		C
B4	PT3A	0		T	B4	PT3E	0		T	B4	PT5C	0		T
D5	PT2D	0		C	D5	PT3D	0		C	D5	PT5B	0		C
D6	PT2C	0		T	D6	PT3C	0		T	D6	PT5A	0		T
C4	PT2E	0		T	C4	PT4A	0		T	C4	PT4A	0		T
C5	PT2F	0		C	C5	PT4B	0		C	C5	PT4B	0		C
-	-	-			-	-	-			GND	GND	-		
D4	NC				D4	PT2D	0		C	D4	PT3D	0		C
D3	NC				D3	PT2C	0		T	D3	PT3C	0		T

**LA-MachXO2280 Logic Signal Connections: 324 ftBGA (Cont.)**

LAMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
G2	PL11A	6		T*
H2	PL11B	6		C*
L3	PL11C	6		T
L5	PL11D	6		C
H1	PL12A	6		T*
VCCIO6	VCCIO6	6		
GND	GNDIO6	6		
J2	PL12B	6		C*
L4	PL12C	6		T
L6	PL12D	6		C
K2	PL13A	6		T*
K1	PL13B	6		C*
J1	PL13C	6		T
VCC	VCC	-		
L2	PL13D	6		C
M5	PL14D	6		C
M3	PL14C	6	TSALL	T
L1	PL14B	6		C*
M2	PL14A	6		T*
M1	PL15A	6		T*
N1	PL15B	6		C*
M6	PL15C	6		T
M4	PL15D	6		C
VCCIO6	VCCIO6	6		
GND	GNDIO6	6		
P1	PL16A	6		T*
P2	PL16B	6		C*
N3	PL16C	6		T
N4	PL16D	6		C
GND	GND	-		
T1	PL17A	6	LLM0_PLLT_FB_A	T*
R1	PL17B	6	LLM0_PLLC_FB_A	C*
P3	PL17C	6		T
N5	PL17D	6		C
R3	PL18A	6	LLM0_PLLT_IN_A	T*
R2	PL18B	6	LLM0_PLLC_IN_A	C*
P4	PL19A	6		T
N6	PL19B	6		C
U1	PL20A	6		T
VCCIO6	VCCIO6	6		
GND	GNDIO6	6		
GND	GNDIO5	5		
VCCIO5	VCCIO5	5		

**LA-MachXO2280 Logic Signal Connections: 324 ftBGA (Cont.)**

LAMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
V10	PB9B	4		C
N10	PB9C	4		T
R10	PB9D	4		C
P10	PB10F	4	PCLK4_1**	C
T10	PB10E	4		T
U10	PB10D	4		C
V11	PB10C	4		T
U11	PB10B	4	PCLK4_0**	C
VCCIO4	VCCIO4	4		
GND	GNDIO4	4		
T11	PB10A	4		T
U12	PB11A	4		T
R11	PB11B	4		C
GND	GND	-		
T12	PB11C	4		T
P11	PB11D	4		C
V12	PB12A	4		T
V13	PB12B	4		C
R12	PB12C	4		T
N11	PB12D	4		C
U13	PB12E	4		T
VCCIO4	VCCIO4	4		
GND	GNDIO4	4		
V14	PB12F	4		C
T13	PB13A	4		T
P12	PB13B	4		C
R13	PB13C	4		T
N12	PB13D	4		C
V15	PB14A	4		T
U14	PB14B	4		C
V16	PB14C	4		T
GND	GND	-		
T14	PB14D	4		C
U15	PB15A	4		T
V17	PB15B	4		C
P13	NC	-		
T15	PB15D	4		
U16	PB16A	4		T
V18	PB16B	4		C
N13	PB16C	4		T
R14	PB16D	4		C
VCCIO4	VCCIO4	4		
GND	GNDIO4	4		

**LA-MachXO2280 Logic Signal Connections: 324 ftBGA (Cont.)**

LAMXO2280				
Ball Number	Ball Function	Bank	Dual Function	Differential
J13	PR10C	2		T
M18	PR10B	2		C*
L18	PR10A	2		T*
GND	GNDIO2	2		
VCCIO2	VCCIO2	2		
H16	PR9D	2		C
H14	PR9C	2		T
K18	PR9B	2		C*
J18	PR9A	2		T*
J17	PR8D	2		C
VCC	VCC	-		
H18	PR8C	2		T
H17	PR8B	2		C*
G17	PR8A	2		T*
H13	PR7D	2		C
H15	PR7C	2		T
G18	PR7B	2		C*
F18	PR7A	2		T*
G14	PR6D	2		C
G16	PR6C	2		T
VCCIO2	VCCIO2	2		
GND	GNDIO2	2		
E18	PR6B	2		C*
F17	PR6A	2		T*
G13	PR5D	2		C
G15	PR5C	2		T
E17	PR5B	2		C*
E16	PR5A	2		T*
GND	GND	-		
F15	PR4D	2		C
E15	PR4C	2		T
D17	PR4B	2		C*
D18	PR4A	2		T*
B18	PR3D	2		C
C18	PR3C	2		T
C16	PR3B	2		C*
D16	PR3A	2		T*
C17	PR2B	2		C
D15	PR2A	2		T
VCCIO2	VCCIO2	2		
GND	GNDIO2	2		
GND	GNDIO1	1		
VCCIO1	VCCIO1	1		