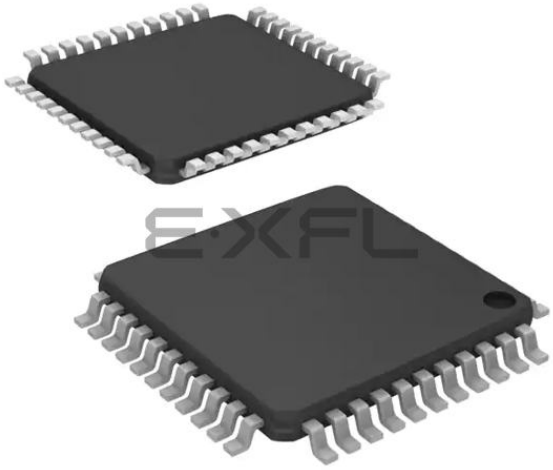

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	ECANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f45k80t-i-pt

5.7 Reset State of Registers

Most registers are unaffected by a Reset. Their status is unknown on a Power-on Reset and unchanged by all other Resets. The other registers are forced to a "Reset state" depending on the type of Reset that occurred.

Most registers are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. Status bits from the RCON register, $\overline{RI}$, $\overline{TO}$, $\overline{PD}$, $\overline{CM}$, $\overline{POR}$ and $\overline{BOR}$, are set or cleared differently in different Reset situations, as indicated in Table 5-3. These bits are used in software to determine the nature of the Reset.

Table 5-4 describes the Reset states for all of the Special Function Registers. These are categorized by Power-on and Brown-out Resets, Master Clear and WDT Resets and WDT wake-ups.

TABLE 5-3: STATUS BITS, THEIR SIGNIFICANCE AND THE INITIALIZATION CONDITION FOR RCON REGISTER

Condition	Program Counter(1)	RCON Register							STKPTR Register	
		SBOREN	$\overline{CM}$	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$	STKFUL	STKUNF
Power-on Reset	0000h	1	1	1	1	1	0	0	0	0
RESET Instruction	0000h	u(2)	u	0	u	u	u	u	u	u
Brown-out Reset	0000h	u(2)	1	1	1	1	u	0	u	u
$\overline{MCLR}$ Reset during Power-Managed Run modes	0000h	u(2)	u	u	1	u	u	u	u	u
$\overline{MCLR}$ Reset during Power-Managed Idle modes and Sleep mode	0000h	u(2)	u	u	1	0	u	u	u	u
WDT Time-out during Full Power or Power-Managed Run modes	0000h	u(2)	u	u	0	u	u	u	u	u
$\overline{MCLR}$ Reset during Full-Power execution	0000h	u(2)	u	u	u	u	u	u	u	u
Stack Full Reset (STVREN = 1)	0000h	u(2)	u	u	u	u	u	u	1	u
Stack Underflow Reset (STVREN = 1)	0000h	u(2)	u	u	u	u	u	u	u	1
Stack Underflow Error (not an actual Reset, STVREN = 0)	0000h	u(2)	u	u	u	u	u	u	u	1
WDT Time-out during Power-Managed Idle or Sleep modes	PC + 2	u(2)	u	u	0	0	u	u	u	u
Interrupt Exit from Power-Managed modes	PC + 2	u(2)	u	u	u	0	u	u	u	u

Legend: u = unchanged

Note 1: When the wake-up is due to an interrupt and the GIEH or GIEL bits are set, the PC is loaded with the interrupt vector (008h or 0018h).

2: Reset state is '1' for POR and unchanged for all other Resets when software BOR is enabled (BOREN<1:0>, Configuration bits = 01 and SBOREN = 1); otherwise, the Reset state is '0'.

8.3 Reading the Data EEPROM Memory

To read a data memory location, the user must write the address to the EEADRH:EEADR register pair, clear the EEPGD control bit (EECON1<7>) and then set control bit, RD (EECON1<0>). The data is available after one instruction cycle, in the EEDATA register. It can be read after one NOP instruction. EEDATA will hold this value until another read operation or until it is written to by the user (during a write operation).

The basic process is shown in Example 8-1.

8.4 Writing to the Data EEPROM Memory

To write an EEPROM data location, the address must first be written to the EEADRH:EEADR register pair and the data written to the EEDATA register. The sequence in Example 8-2 must be followed to initiate the write cycle.

The write will not begin if this sequence is not exactly followed (write 55h to EECON2, write 0AAh to EECON2, then set WR bit) for each byte. It is strongly recommended that interrupts be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable writes. This mechanism prevents accidental writes to data EEPROM due to unexpected code execution (i.e., runaway programs). The WREN bit should be kept clear at all times, except when updating the EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, EECON1, EEADRH:EEADR and EEDATA cannot be modified. The WR bit will be inhibited from being set unless the WREN bit is set. The WREN bit must be set on a previous instruction. Both WR and WREN cannot be set with the same instruction.

At the completion of the write cycle, the WR bit is cleared in hardware and the EEPROM Interrupt Flag bit (EEIF) is set. The user may either enable this interrupt or poll this bit; EEIF must be cleared by software.

8.5 Write Verify

Depending on the application, good programming practice may dictate that the value written to the memory should be verified against the original value. This should be used in applications where excessive writes can stress bits near the specification limit.

Note:	Self-write execution to Flash and EEPROM memory cannot be done while running in LP Oscillator (low-power) mode. Executing a self-write will put the device into High-Power mode.

TABLE 11-5: PORTC FUNCTIONS (CONTINUED)

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RC7/CANRX/ RX1/DT1/ CCP4	RC7	0	O	DIG	LATC<7> data output.
		1	I	ST	PORTC<7> data input.
	CANRX(2)	1	I	ST	CAN bus RX.
	RX1(1)	1	I	ST	Asynchronous serial receive data input (EUSARTx module).
	DT1(1)	1	O	DIG	Synchronous serial data output (EUSARTx module); takes priority over port data.
		1	I	ST	Synchronous serial data input (EUSARTx module); user must configure as an input.
	CCP4	0	O	DIG	CCP4 compare/PWM output; takes priority over port data.
		1	I	ST	CCP4 capture input.

Legend: O = Output; I = Input; I^2C = I^2C/SMBus; ANA = Analog Signal; DIG = CMOS Output; ST = Schmitt Trigger Buffer Input; x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

Note 1: The pin assignment for 28, 40 and 44-pin devices (PIC18F2XK80 and PIC18F4XK80).

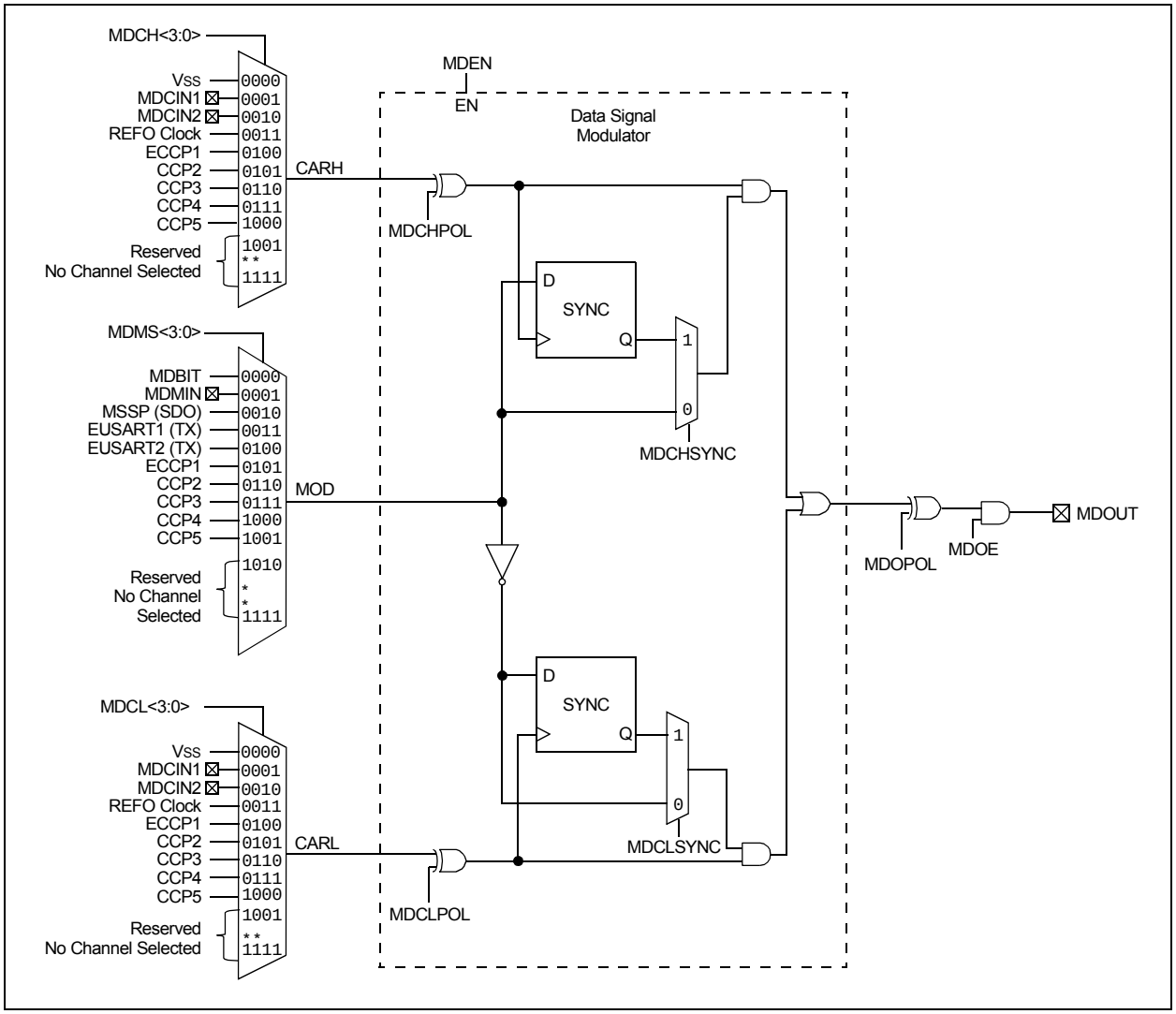
2: The alternate pin assignment for CANRX and CANTX on 28, 40 and 44-pin devices (PIC18F4XK80) when the CANMX Configuration bit is set.

TABLE 11-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
LATC	LATC7	LATBC6	LATC5	LATCB4	LATC3	LATC2	LATC1	LATC0
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
ODCON	SSPOD	CCP5OD	CCP4OD	CCP3OD	CCP2OD	CCP1OD	U2OD	U1OD

Legend: Shaded cells are not used by PORTC.

FIGURE 12-1: SIMPLIFIED BLOCK DIAGRAM OF THE DATA SIGNAL MODULATOR



For more details on selecting the optimum C1 and C2 for a given crystal, see the crystal manufacture's applications information. The optimum value depends in part on the amount of parasitic capacitance in the circuit, which is often unknown. For that reason, it is highly recommended that thorough testing and validation of the oscillator be performed after values have been selected.

14.5.1 USING SOSC AS A CLOCK SOURCE

The SOSC oscillator is also available as a clock source in power-managed modes. By setting the clock select bits, SCS<1:0> (OSCCON<1:0>), to '01', the device switches to SEC_RUN mode and both the CPU and peripherals are clocked from the SOSC oscillator. If the IDLEN bit (OSCCON<7>) is cleared and a SLEEP instruction is executed, the device enters SEC_IDLE mode. Additional details are available in **Section 4.0 "Power-Managed Modes"**.

Whenever the SOSC oscillator is providing the clock source, the SOSC System Clock Status flag, SOSCRUN (OSCCON2<6>), is set. This can be used to determine the controller's current clocking mode. It can also indicate the clock source currently being used by the Fail-Safe Clock Monitor.

If the Clock Monitor is enabled and the SOSC oscillator fails while providing the clock, polling the SOCSRUN bit will indicate whether the clock is being provided by the SOSC oscillator or another source.

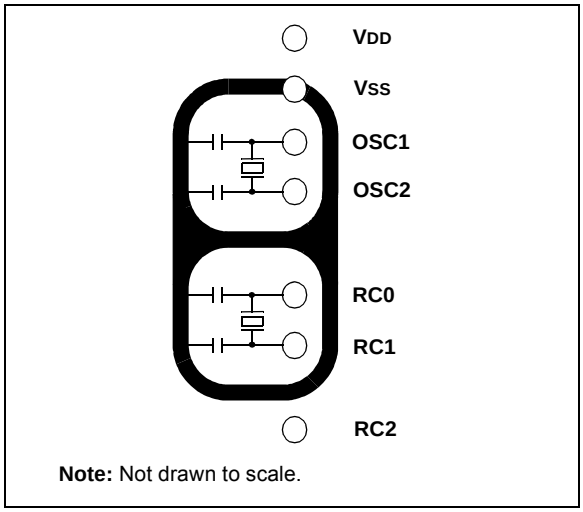
14.5.2 SOSC OSCILLATOR LAYOUT CONSIDERATIONS

The SOSC oscillator circuit draws very little power during operation. Due to the low-power nature of the oscillator, it may also be sensitive to rapidly changing signals in close proximity. This is especially true when the oscillator is configured for extremely Low-Power mode, SOSCSEL<1:0> (CONFIG1L<4:3>) = 01.

The oscillator circuit, displayed in Figure 14-2, should be located as close as possible to the microcontroller. There should be no circuits passing within the oscillator circuit boundaries other than VSS or VDD.

If a high-speed circuit must be located near the oscillator, it may help to have a grounded guard ring around the oscillator circuit. The guard, as displayed in Figure 14-3, could be used on a single-sided PCB or in addition to a ground plane. (Examples of a high-speed circuit include the ECCP1 pin, in Output Compare or PWM mode, or the primary oscillator, using the OSC2 pin.)

FIGURE 14-3: OSCILLATOR CIRCUIT WITH GROUNDED GUARD RING



Note: Not drawn to scale.

In the Low Drive Level mode, SOSCSEL<1:0> = 01, it is critical that RC2 I/O pin signals be kept away from the oscillator circuit. Configuring RC2 as a digital output, and toggling it, can potentially disturb the oscillator circuit, even with a relatively good PCB layout. If possible, either leave RC2 unused or use it as an input pin with a slew rate limited signal source. If RC2 must be used as a digital output, it may be necessary to use the Higher Drive Level Oscillator mode (SOSCSEL<1:0> = 11) with many PCB layouts.

Even in the Higher Drive Level mode, careful layout procedures should still be followed when designing the oscillator circuit.

In addition to dV/dt induced noise considerations, it is important to ensure that the circuit board is clean. Even a very small amount of conductive, soldering flux residue can cause PCB leakage currents that can overwhelm the oscillator circuit.

14.6 Timer1 Interrupt

The TMR1 register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The Timer1 interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit, TMR1IF (PIR1<0>). This interrupt can be enabled or disabled by setting or clearing the Timer1 Interrupt Enable bit, TMR1IE (PIE1<0>).

16.1 Timer3 Gate Control Register

The Timer3 Gate Control register (T3GCON), provided in Register 14-2, is used to control the Timer3 gate.

REGISTER 16-2: T3GCON: TIMER3 GATE CONTROL REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-x	R/W-0	R/W-0
TMR3GE	T3GPOL	T3GTM	T3GSPM	T3GGO/$\overline{\text{T3DONE}}$	T3GVAL	T3GSS1	T3GSS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TMR3GE:** Timer3 Gate Enable bit

If TMR3ON = 0:
This bit is ignored.

If TMR3ON = 1:
1 = Timer3 counting is controlled by the Timer3 gate function
0 = Timer3 counts regardless of Timer3 gate function

bit 6 **T3GPOL:** Timer3 Gate Polarity bit

1 = Timer3 gate is active-high (Timer3 counts when gate is high)
0 = Timer3 gate is active-low (Timer3 counts when gate is low)

bit 5 **T3GTM:** Timer3 Gate Toggle Mode bit

1 = Timer3 Gate Toggle mode is enabled.
0 = Timer3 Gate Toggle mode is disabled and toggle flip-flop is cleared
Timer3 gate flip-flop toggles on every rising edge.

bit 4 **T3GSPM:** Timerx Gate Single Pulse Mode bit

1 = Timer3 Gate Single Pulse mode is enabled and is controlling Timer3 gate
0 = Timer3 Gate Single Pulse mode is disabled

bit 3 **T3GGO/$\overline{\text{T3DONE}}$:** Timer3 Gate Single Pulse Acquisition Status bit

1 = Timer3 Gate Single Pulse mode acquisition is ready, waiting for an edge
0 = Timer3 Gate Single Pulse mode acquisition has completed or has not been started
This bit is automatically cleared when T3GSPM is cleared.

bit 2 **T3GVAL:** Timer3 Gate Current State bit

Indicates the current state of the Timerx gate that could be provided to TMR3H:TMR3L. Unaffected by Timerx Gate Enable (TMR3GE) bit.

bit 1-0 **T3GSS<1:0>:** Timer3 Gate Source Select bits

11 = Comparator 2 output
10 = Comparator 1 output
01 = TMR4 to match PR4 output
00 = Timer3 gate pin
Watchdog Timer oscillator is turned on if TMR3GE = 1, regardless of the state of TMR3ON.

Note 1: Programming the T3GCON prior to T3CON is recommended.

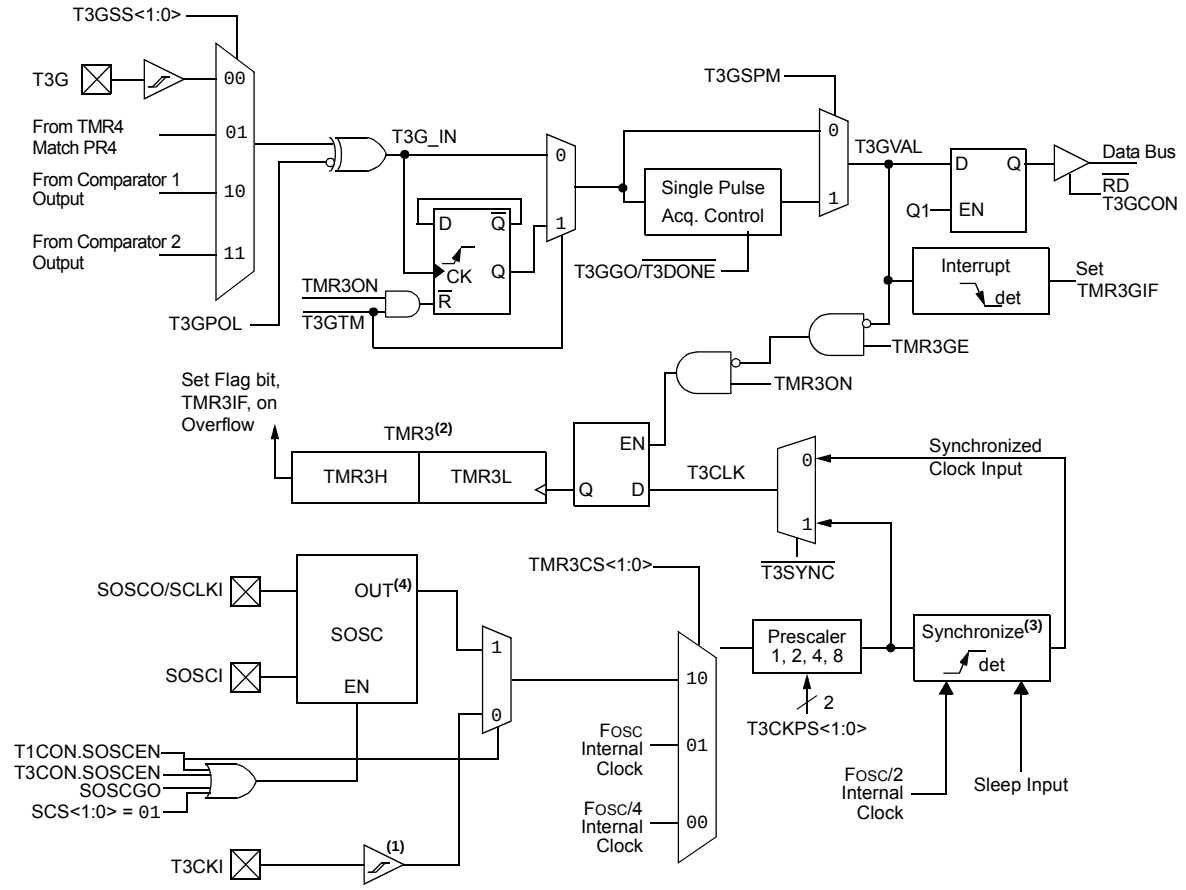
16.2 Timer3 Operation

Timer3 can operate in these modes:

- Timer
- Synchronous Counter
- Asynchronous Counter
- Timer with Gated Control

The operating mode is determined by the clock select bits, TMR3CSx (T3CON<7:6>). When the TMR3CSx bits are cleared (= 00), Timer3 increments on every internal instruction cycle (FOSC/4). When TMR3CSx = 01, the Timer3 clock source is the system clock (FOSC), and when it is '10', Timer3 works as a counter from the external clock from the T3CKI pin (on the rising edge after the first falling edge) or the SOSC oscillator.

FIGURE 16-1: TIMER3 BLOCK DIAGRAM



Note 1: ST Buffer is high-speed type when using T3CKI.
2: Timer3 registers increment on rising edge.
3: Synchronization does not operate while in Sleep.
4: The output of SOSC is determined by the SOSCSEL<1:0> Configuration bits.

16.5 Timer3 Gates

Timer3 can be configured to count freely or the count can be enabled and disabled using the Timer3 gate circuitry. This is also referred to as the Timer3 gate count enable.

The Timer3 gate can also be driven by multiple selectable sources.

16.5.1 TIMER3 GATE COUNT ENABLE

The Timer3 Gate Enable mode is enabled by setting the TMR3GE bit (TxGCON<7>). The polarity of the Timer3 Gate Enable mode is configured using the T3GPOL bit (T3GCON<6>).

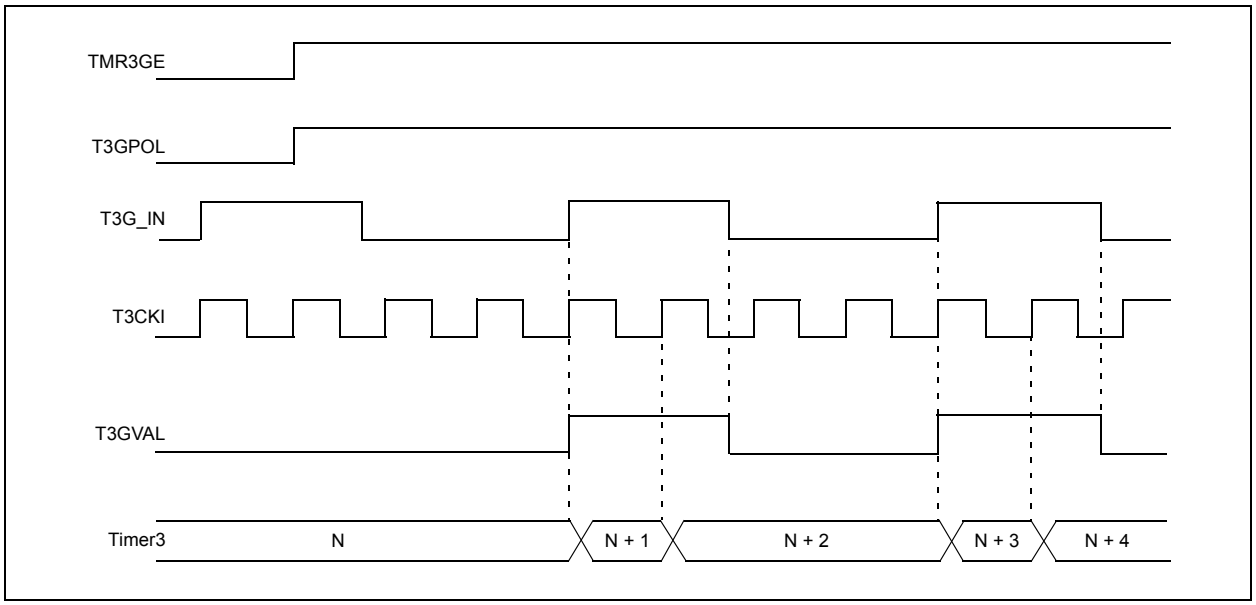
When Timer3 Gate Enable mode is enabled, Timer3 will increment on the rising edge of the Timer3 clock source. When Timer3 Gate Enable mode is disabled, no incrementing will occur and Timer3 will hold the current count. See Figure 16-2 for timing details.

TABLE 16-1: TIMER3 GATE ENABLE SELECTIONS

T3CLK(†)	T3GPOL (T3GCON<6>)	T3G Pin	Timer3 Operation
↑	0	0	Counts
↑	0	1	Holds Count
↑	1	0	Holds Count
↑	1	1	Counts

† The clock on which TMR3 is running. For more information, see T3CLK in Figure 16-1.

FIGURE 16-2: TIMER3 GATE COUNT ENABLE MODE



16.5.4 TIMER3 GATE SINGLE PULSE MODE

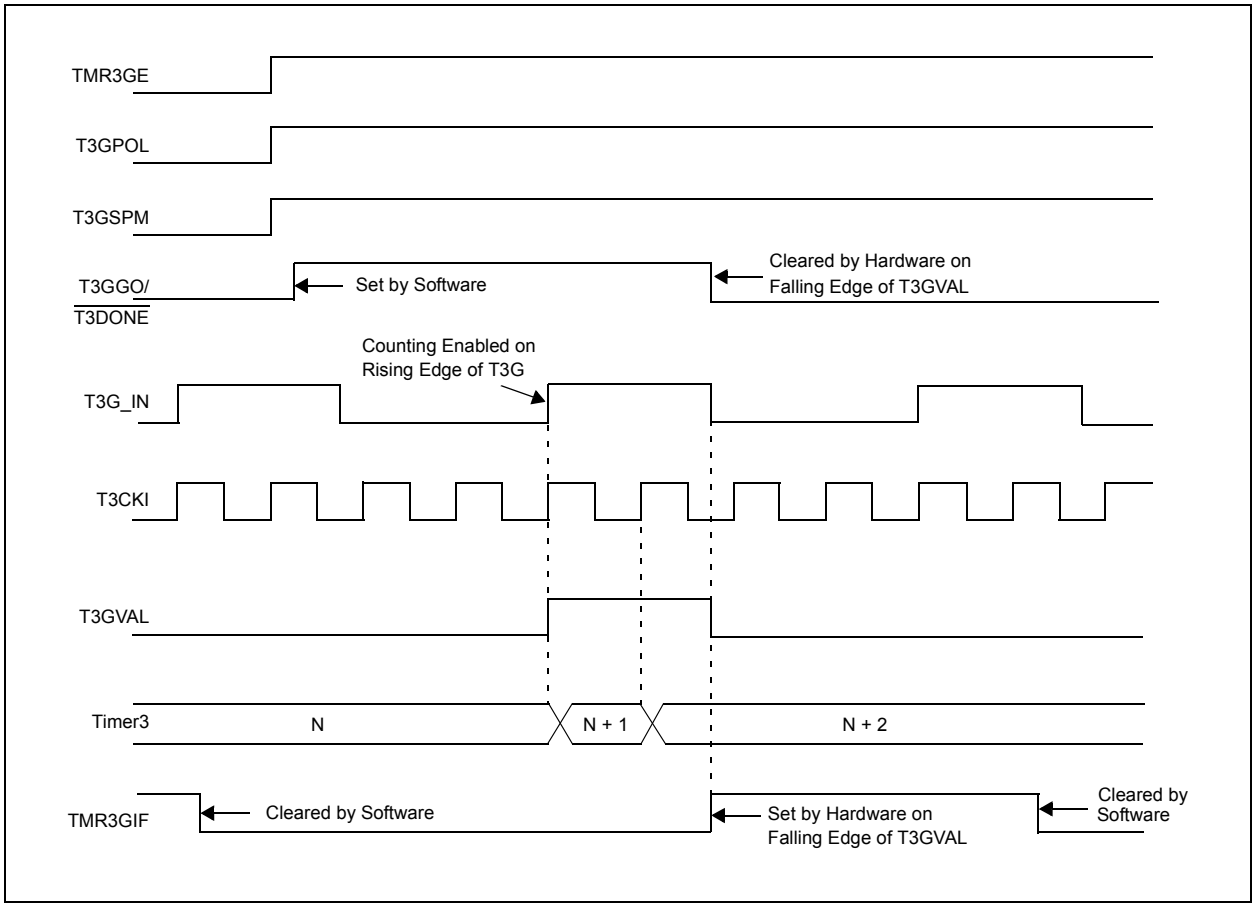
When Timer3 Gate Single Pulse mode is enabled, it is possible to capture a single pulse gate event. Timer3 Gate Single Pulse mode is first enabled by setting the T3GSPM bit (T3GCON<4>). Next, the T3GGO/$\overline{\text{T3DONE}}$ bit (T3GCON<3>) must be set.

The Timer3 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the T3GGO/$\overline{\text{T3DONE}}$ bit will automatically be cleared. No other gate events will be allowed to increment Timer3 until the T3GGO/$\overline{\text{T3DONE}}$ bit is once again set in software.

Clearing the T3GSPM bit will also clear the T3GGO/$\overline{\text{T3DONE}}$ bit. (For timing details, see Figure 16-4.)

Simultaneously enabling the Toggle mode and the Single Pulse mode will permit both sections to work together. This allows the cycle times on the Timer3 gate source to be measured. (For timing details, see Figure 16-5.)

FIGURE 16-4: TIMER3 GATE SINGLE PULSE MODE

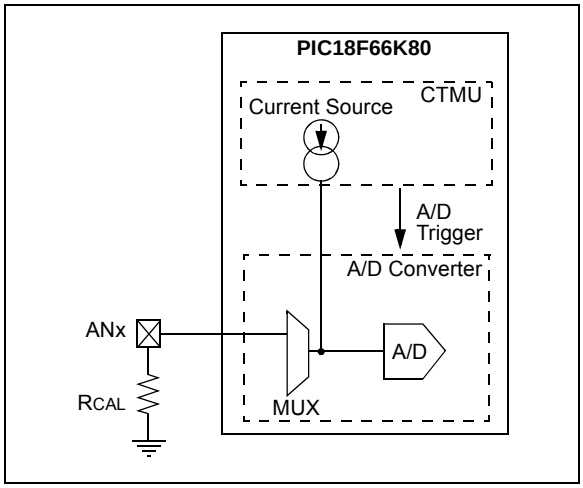


The CTMU current source may be trimmed with the trim bits in CTMUICON, using an iterative process to get the exact current desired. Alternatively, the nominal value without adjustment may be used. That value may be stored by software, for use in all subsequent capacitive or time measurements.

To calculate the optimal value for RCAL, the nominal current must be chosen.

For example, if the A/D Converter reference voltage is 3.3V, use 70% of full scale (or 2.31V) as the desired approximate voltage to be read by the A/D Converter. If the range of the CTMU current source is selected to be 0.55 μA, the resistor value needed is calculated as RCAL = 2.31V/0.55 μA, for a value of 4.2 MΩ. Similarly, if the current source is chosen to be 5.5 μA, RCAL would be 420,000Ω, and 42,000Ω if the current source is set to 55 μA.

FIGURE 18-2: CTMU CURRENT SOURCE CALIBRATION CIRCUIT



A value of 70% of full-scale voltage is chosen to make sure that the A/D Converter is in a range that is well above the noise floor. If an exact current is chosen to incorporate the trimming bits from CTMUICON, the resistor value of RCAL may need to be adjusted accordingly. RCAL also may be adjusted to allow for available resistor values. RCAL should be of the highest precision available, in light of the precision needed for the circuit that the CTMU will be measuring. A recommended minimum would be 0.1% tolerance.

The following examples show a typical method for performing a CTMU current calibration.

- Example 18-1 demonstrates how to initialize the A/D Converter and the CTMU.

  This routine is typical for applications using both modules.

- Example 18-2 demonstrates one method for the actual calibration routine.

  This method manually triggers the A/D Converter to demonstrate the entire step-wise process. It is also possible to automatically trigger the conversion by setting the CTMU's CTTRIG bit (CTMUCONH<0>).

19.2 Capture Mode

In Capture mode, the CCPRxH:CCPRxL register pair captures the 16-bit value of the Timer register selected in the CCPTMRS when an event occurs on the CCPx pin. An event is defined as one of the following:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

Note:	For CCP2 only, the Capture mode can use the CCP2 input pin as the capture trigger for CCP2 or the input can function as a time-stamp through the CAN module. The CAN module provides the necessary control and trigger signals.

The event is selected by the mode select bits, CCPxM<3:0> (CCPxCON<3:0>). When a capture is made, the interrupt request flag bit, CCPxIF (PIR4<x>), is set; it must be cleared in software. If another capture occurs before the value in CCPRx is read, the old captured value is overwritten by the new captured value.

Figure 19-1 shows the Capture mode block diagram.

19.2.1 CCP PIN CONFIGURATION

In Capture mode, the appropriate CCPx pin should be configured as an input by setting the corresponding TRIS direction bit.

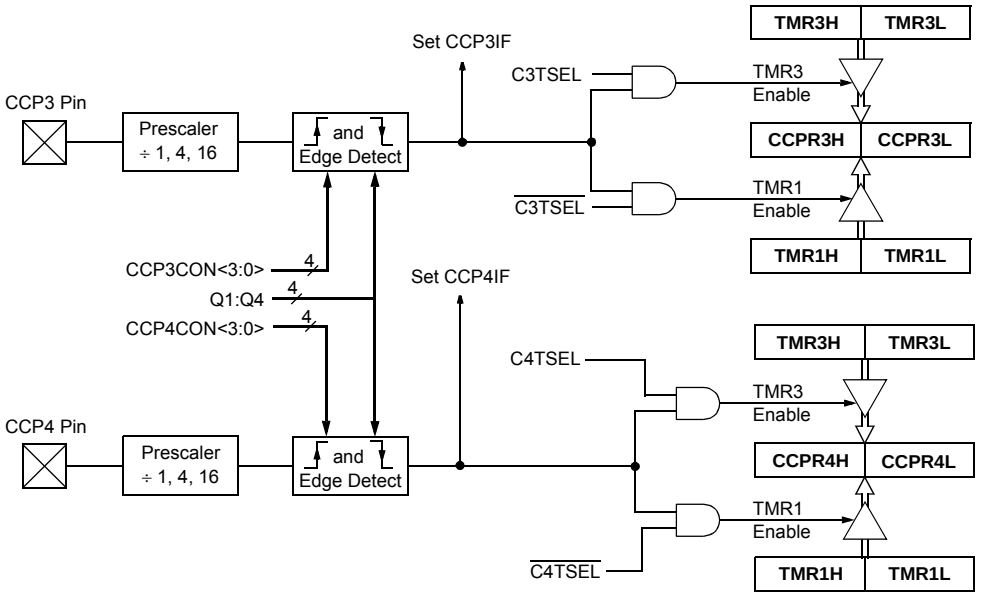
19.2.2 TIMER1/3 MODE SELECTION

For the available timers (1/3) to be used for the capture feature, the used timers must be running in Timer mode or Synchronized Counter mode. In Asynchronous Counter mode, the capture operation may not work.

The timer to be used with each CCP module is selected in the CCPTMRS register. (See **Section 19.1.1 "CCP Modules and Timer Resources"**.)

Details of the timer assignments for the CCP modules are given in Table 19-2.

FIGURE 19-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



Note: This block diagram uses CCP3 and CCP4, and their appropriate timers as an example. For details on all of the CCP modules and their timer assignments, see Table 19-2.

REGISTER 20-1: CCP1CON: ENHANCED CAPTURE/COMPARE/PWM1 CONTROL

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **P1M<1:0>:** Enhanced PWM Output Configuration bits

If CCP1M<3:2> = 00, 01, 10:

xx = P1A assigned as capture/compare input/output; P1B, P1C and P1D assigned as port pins

If CCP1M<3:2> = 11:

00 = Single output: P1A, P1B, P1C and P1D are controlled by steering (see **Section 20.4.7 "Pulse Steering Mode"**)

01 = Full-bridge output forward: P1D is modulated; P1A is active; P1B, P1C is inactive

10 = Half-bridge output: P1A, P1B are modulated with dead-band control; P1C and P1D are assigned as port pins

11 = Full-bridge output reverse: P1B is modulated; P1C is active; P1A and P1D are inactive

bit 5-4 **DC1B<1:0>**: PWM Duty Cycle bit 1 and bit 0

Capture mode:

Unused.

Compare mode:

Unused.

PWM mode:

These bits are the two LSbs of the 10-bit PWM duty cycle. The eight MSbs of the duty cycle are found in CCPR1L.

bit 3-0 **CCP1M<3:0>**: ECCP1 Mode Select bits

0000 = Capture/Compare/PWM off (resets ECCP1 module)

0001 = Reserved

0010 = Compare mode: Toggle output on match

0011 = Capture mode

0100 = Capture mode: Every falling edge

0101 = Capture mode: Every rising edge

0110 = Capture mode: Every fourth rising edge

0111 = Capture mode: Every 16th rising edge

1000 = Compare mode: Initialize ECCP1 pin low, set output on compare match (set CCP1IF)

1001 = Compare mode: Initialize ECCP1 pin high, clear output on compare match (set CCP1IF)

1010 = Compare mode: Generate software interrupt only, ECCP1 pin reverts to I/O state

1011 = Compare mode: Trigger special event (ECCP1 resets TMR1 or TMR3, starts A/D conversion, sets CCP1IF bit)

1100 = PWM mode: P1A and P1C are active-high; P1B and P1D are active-high

1101 = PWM mode: P1A and P1C are active-high; P1B and P1D are active-low

1110 = PWM mode: P1A and P1C are active-low; P1B and P1D are active-high

1111 = PWM mode: P1A and P1C are active-low; P1B and P1D are active-low

21.4.6 MASTER MODE

Master mode is enabled by setting and clearing the appropriate SSPMx bits in SSPCON1 and by setting the SSPEN bit. In Master mode, the SCL and SDA lines are manipulated by the MSSP hardware if the TRIS bits are set.

Master mode of operation is supported by interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I^2C bus may be taken when the P bit is set, or the bus is Idle, with both the S and P bits clear.

In Firmware Controlled Master mode, user code conducts all I^2C bus operations based on Start and Stop bit conditions.

Once Master mode is enabled, the user has six options.

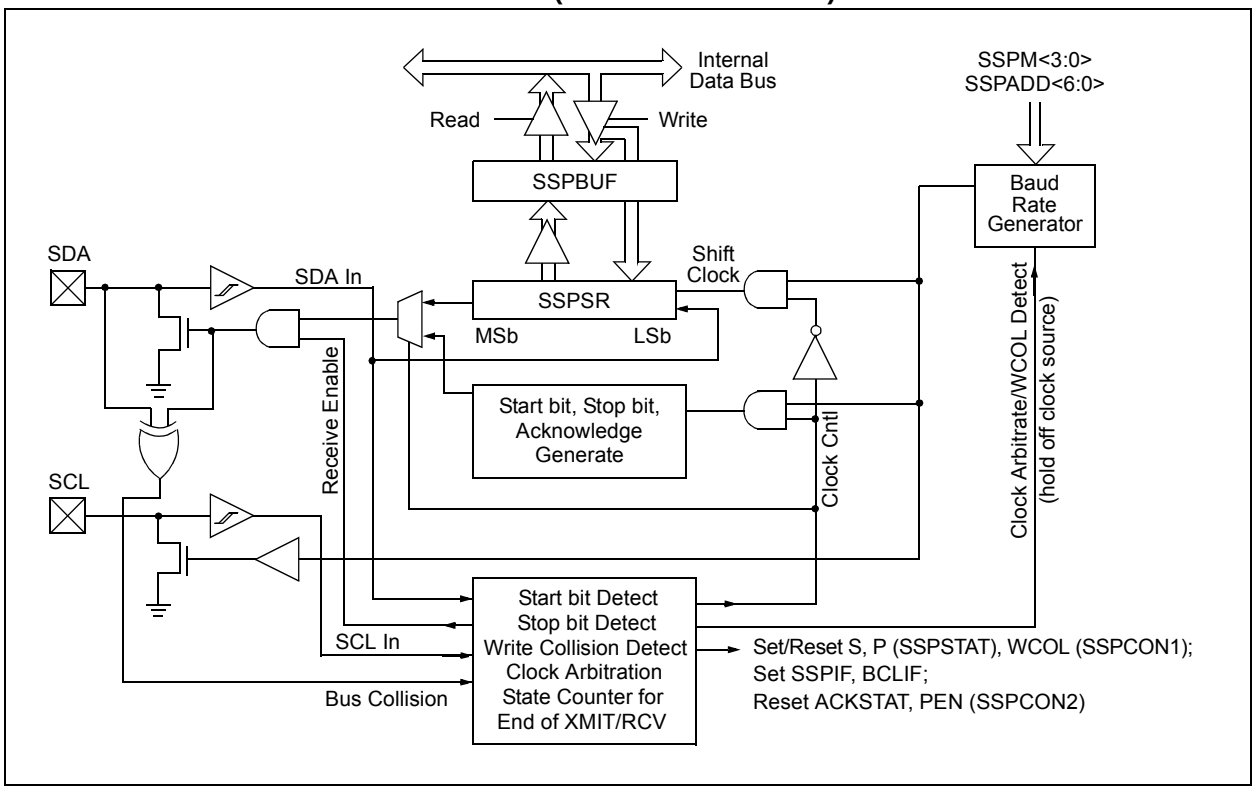
1. Assert a Start condition on SDA and SCL.
2. Assert a Repeated Start condition on SDA and SCL.
3. Write to the SSPBUF register initiating transmission of data/address.
4. Configure the I^2C port to receive data.
5. Generate an Acknowledge condition at the end of a received byte of data.
6. Generate a Stop condition on SDA and SCL.

Note:	The MSSP module, when configured in I^2C Master mode, does not allow queueing of events. For instance, the user is not allowed to initiate a Start condition and immediately write the SSPBUF register to initiate transmission before the Start condition is complete. In this case, the SSPBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPBUF did not occur.

The following events will cause the MSSP Interrupt Flag bit, SSPIF, to be set (and MSSP interrupt, if enabled):

- Start condition
- Stop condition
- Data transfer byte transmitted/received
- Acknowledge transmitted
- Repeated Start

FIGURE 21-18: MSSP BLOCK DIAGRAM (I^2C™ MASTER MODE)



21.4.17.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

a) A low level is sampled on SDA when SCL goes from a low level to a high level.

b) SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1'.

When the user deasserts SDA and the pin is allowed to float high, the BRG is loaded with SSPADD<6:0> and counts down to 0. The SCL pin is then deasserted and when sampled high, the SDA pin is sampled.

If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 21-31). If SDA is sampled high, the BRG is reloaded and begins counting. If SDA goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

If SCL goes from high-to-low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition (see Figure 21-32).

If, at the end of the BRG time-out, both SCL and SDA are still high, the SDA pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated Start condition is complete.

FIGURE 21-31: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

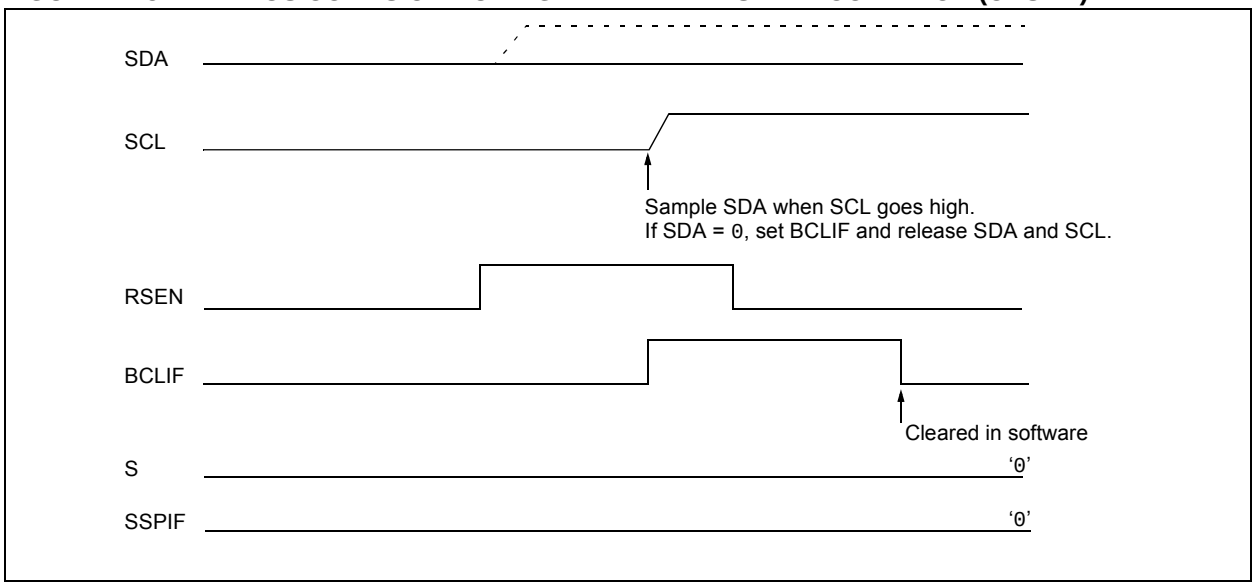


FIGURE 21-32: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)

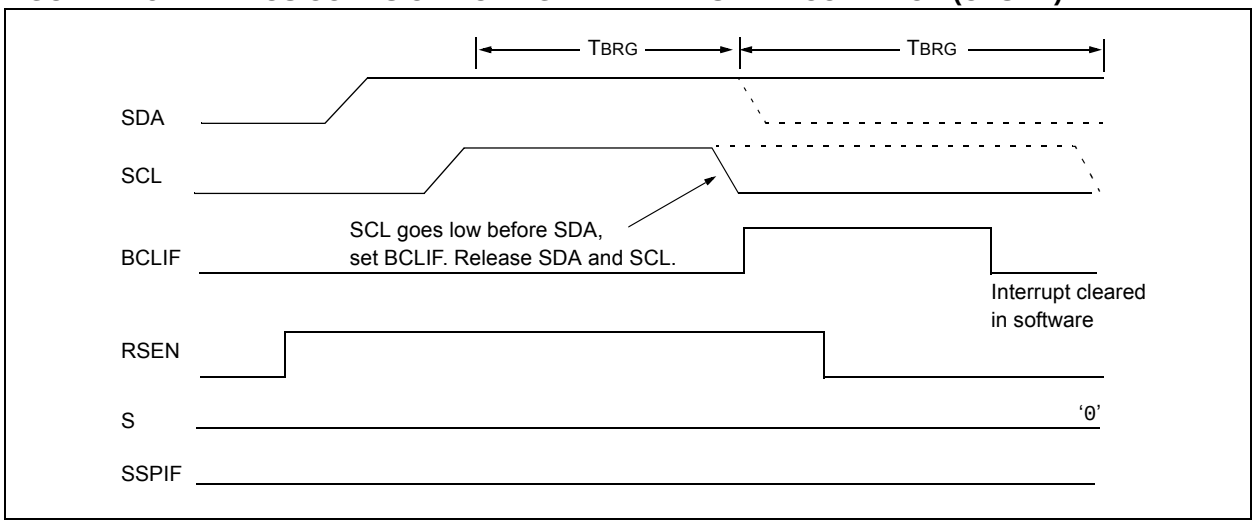
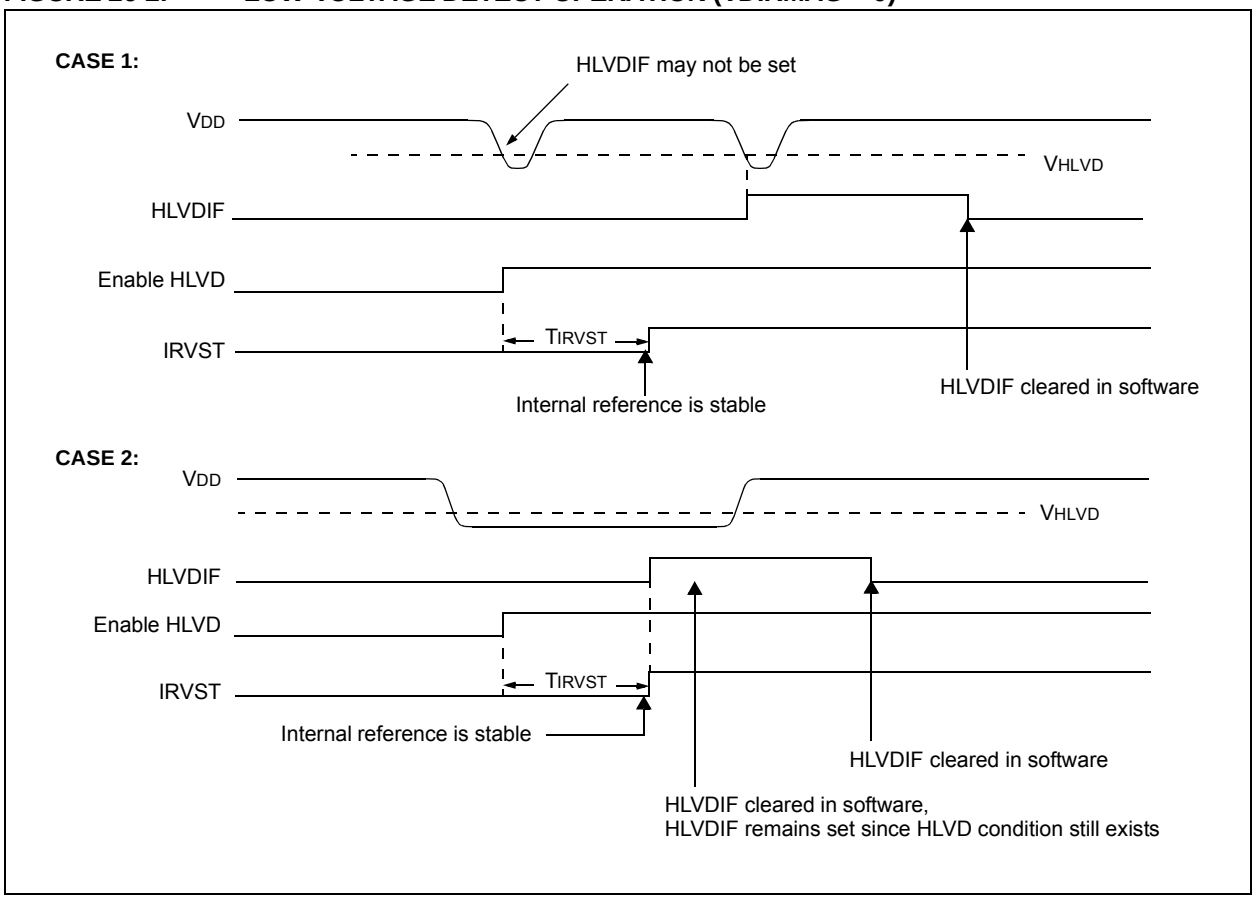


TABLE 22-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSPIF	TMR1GIF	TMR2IF	TMR1IF
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSPIE	TMR1GIE	TMR2IE	TMR1IE
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSPIP	TMR1GIP	TMR2IP	TMR1IP
PIR3	—	—	RC2IF	TX2IF	CTMUIF	CCP2IF	CCP1IF	—
PIE3	—	—	RC2IE	TX2IE	CTMUIE	CCP2IE	CCP1IE	—
IPR3	—	—	RC2IP	TX2IP	CTMUIP	CCP2IP	CCP1IP	—
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
TXREG1	EUSART1 Transmit Register							
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
BAUDCON1	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN
SPBRGH1	EUSART1 Baud Rate Generator Register High Byte							
SPBRG1	EUSART1 Baud Rate Generator Register Low Byte							
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
TXREG2	EUSART2 Transmit Register							
TXSTA2	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
BAUDCON2	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN
SPBRGH2	EUSART2 Baud Rate Generator Register High Byte							
SPBRG2	EUSART2 Baud Rate Generator Register Low Byte							
PMD0	CCP5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD	UART2MD	UART1MD	SSPMD
ODCON	SSPOD	CCP5OD	CCP4OD	CCP3OD	CCP2OD	CCP1OD	U2OD	U1OD

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.

FIGURE 26-2: LOW-VOLTAGE DETECT OPERATION (VDIRMAG = 0)



REGISTER 27-50: MSEL2: MASK SELECT REGISTER 2(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FIL11_1	FIL11_0	FIL10_1	FIL10_0	FIL9_1	FIL9_0	FIL8_1	FIL8_0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **FIL11_<1:0>:** Filter 11 Select bits 1 and 0
11 = No mask
10 = Filter 15
01 = Acceptance Mask 1
00 = Acceptance Mask 0

bit 5-4 **FIL10_<1:0>:** Filter 10 Select bits 1 and 0
11 = No mask
10 = Filter 15
01 = Acceptance Mask 1
00 = Acceptance Mask 0

bit 3-2 **FIL9_<1:0>:** Filter 9 Select bits 1 and 0
11 = No mask
10 = Filter 15
01 = Acceptance Mask 1
00 = Acceptance Mask 0

bit 1-0 **FIL8_<1:0>:** Filter 8 Select bits 1 and 0
11 = No mask
10 = Filter 15
01 = Acceptance Mask 1
00 = Acceptance Mask 0

Note 1: This register is available in Mode 1 and 2 only.

31.2 DC Characteristics: Power-Down and Supply Current PIC18F66K80 Family (Industrial/Extended) (Continued)

PIC18F66K80 Family (Industrial/Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD) Cont.(2,3)						
	PIC18**LF**XXK80	75	160	µA	-40°C	VDD = 1.8V(4) Regulator Disabled	FOSC = 4 MHz (**PRI_IDLE** mode, EC oscillator)
		75	160	µA	+25°C		
		75	160	µA	+60°C		
		76	170	µA	+85°C		
		82	180	µA	+125°C		
	PIC18**LF**XXK80	148	300	µA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		148	300	µA	+25°C		
		148	300	µA	+60°C		
		150	400	µA	+85°C		
		157	460	µA	+125°C		
	PIC18**F**XXK80	187	320	µA	-40°C	VDD = 3.3V(5) Regulator Enabled	
		204	320	µA	+25°C		
		212	320	µA	+60°C		
		218	420	µA	+85°C		
		230	480	µA	+125°C		
	PIC18**F**XXK80	230	500	µA	-40°C	VDD = 5V(5) Regulator Enabled	
		230	500	µA	+25°C		
		230	500	µA	+60°C		
		240	600	µA	+85°C		
		250	700	µA	+125°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to VDD or VSS, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;

$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: For LF devices, $\overline{RETEN}$ (CONFIG1L<0>) = 1.

5: For F devices, SRETEN (WDTCON<4>) = 1 and $\overline{RETEN}$ (CONFIG1L<0>) = 0.

FIGURE 31-8: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

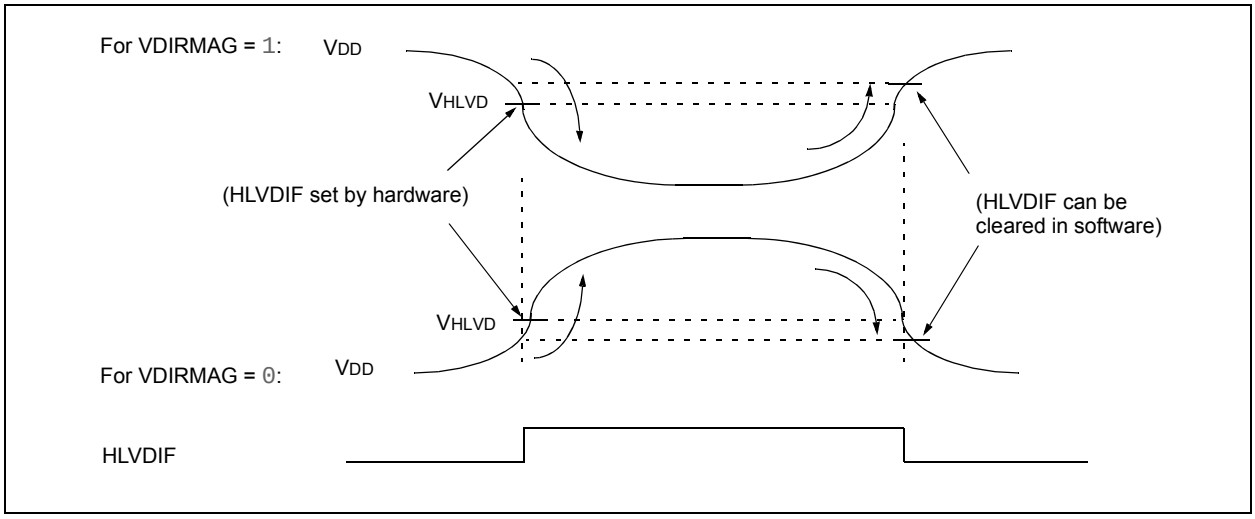
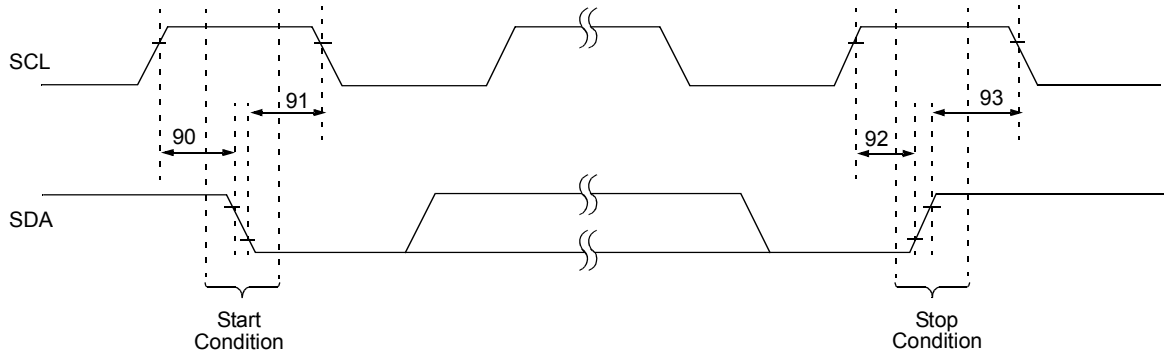


TABLE 31-12: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +85°C for industrial
-40°C ≤ TA ≤ +125°C for extended

Param No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
D420		HLVD Voltage on VDD Transition High-to-Low	HLVDL<3:0> = 0000	1.80	1.85	1.90	V	
			HLVDL<3:0> = 0001	2.03	2.08	2.13	V	
			HLVDL<3:0> = 0010	2.24	2.29	2.35	V	
			HLVDL<3:0> = 0011	2.40	2.46	2.53	V	
			HLVDL<3:0> = 0100	2.50	2.56	2.62	V	
			HLVDL<3:0> = 0101	2.70	2.77	2.84	V	
			HLVDL<3:0> = 0110	2.82	2.89	2.97	V	
			HLVDL<3:0> = 0111	2.95	3.02	3.10	V	
			HLVDL<3:0> = 1000	3.24	3.32	3.41	V	
			HLVDL<3:0> = 1001	3.42	3.50	3.59	V	
			HLVDL<3:0> = 1010	3.61	3.70	3.79	V	
			HLVDL<3:0> = 1011	3.82	3.91	4.10	V	
			HLVDL<3:0> = 1100	4.06	4.16	4.26	V	
			HLVDL<3:0> = 1101	4.33	4.44	4.55	V	
			HLVDL<3:0> = 1110	4.64	4.75	4.87	V	

FIGURE 31-17: MSSP I²C™ BUS START/STOP BITS TIMING WAVEFORMS



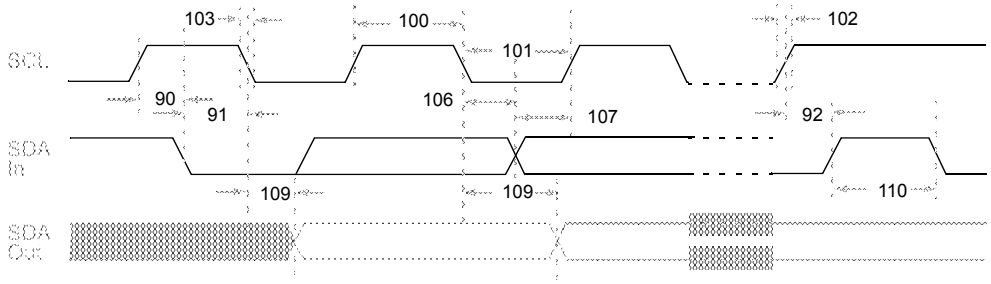
Note: Refer to Figure 31-3 for load conditions.

TABLE 31-21: MSSP I²C™ BUS START/STOP BITS REQUIREMENTS

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
90	TSU:STA	Start Condition Setup Time	100 kHz mode	2(Tosc)(BRG + 1)	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	2(Tosc)(BRG + 1)	—		
			1 MHz mode(1)	2(Tosc)(BRG + 1)	—		
91	THD:STA	Start Condition Hold Time	100 kHz mode	2(Tosc)(BRG + 1)	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	2(Tosc)(BRG + 1)	—		
			1 MHz mode(1)	2(Tosc)(BRG + 1)	—		
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	2(Tosc)(BRG + 1)	—	ns	
			400 kHz mode	2(Tosc)(BRG + 1)	—		
			1 MHz mode(1)	2(Tosc)(BRG + 1)	—		
93	THD:STO	Stop Condition Hold Time	100 kHz mode	2(Tosc)(BRG + 1)	—	ns	
			400 kHz mode	2(Tosc)(BRG + 1)	—		
			1 MHz mode(1)	2(Tosc)(BRG + 1)	—		

Note 1: Maximum pin capacitance = 10 pF for all I²C™ pins.

FIGURE 31-18: MSSP I²C™ BUS DATA TIMING



Note: Refer to Figure 31-3 for load conditions.