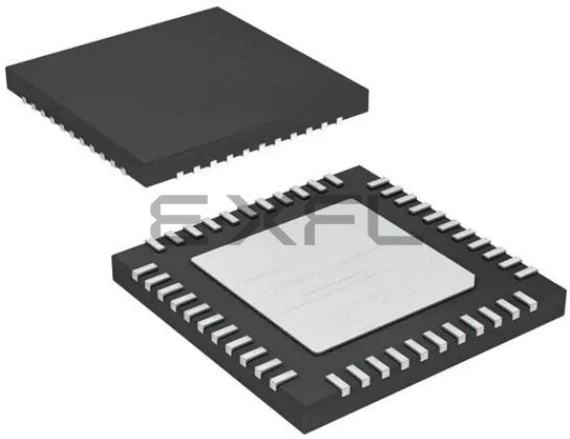

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	ECANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.6K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 11x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f46k80-h-ml

TABLE 1-6: PIC18F6XK80 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Num	Pin Type	Buffer Type	Description
$\overline{\text{MCLR}}$/RE3	28			
$\overline{\text{MCLR}}$		I	ST	Master Clear (input) or programming voltage (input). This pin is an active-low Reset to the device.
RE3		I	ST	General purpose, input only pin.
OSC1/CLKIN/RA7	46			
OSC1		I	ST	Oscillator crystal input.
CLKIN		I	CMOS	External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7		I/O	ST/ CMOS	General purpose I/O pin.
OSC2/CLKOUT/RA6	47			
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKOUT		O	—	In certain oscillator modes, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	ST/ CMOS	General purpose I/O pin.

Legend: I^2C™ = I^2C/SMBus input buffer
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output

TABLE 1-6: PIC18F6XK80 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Num	Pin Type	Buffer Type	Description
				PORTB is a bidirectional I/O port.
RB0/AN10/FLT0/INT0	13			
RB0		I/O	ST/ CMOS	Digital I/O.
AN10		I	Analog	Analog Input 10.
FLT0		I	ST	Enhanced PWM Fault input for ECCP1.
INT0		I	ST	External Interrupt 0.
RB1/AN8/CTDIN/INT1	14			
RB1		I/O	ST/ CMOS	Digital I/O.
AN8		I	Analog	Analog Input 8.
CTDIN		I	ST	CTMU pulse delay input.
INT1		I	ST	External Interrupt 1.
RB2/CANTX/CTED1/ INT2	15			
RB2		I/O	ST/ CMOS	Digital I/O.
CANTX		O	CMOS	CAN bus TX.
CTED1		I	ST	CTMU Edge 1 input.
INT2		I	ST	External Interrupt 2.
RB3/CANRX/CTED2/ INT3	16			
RB3		I/O	ST/ CMOS	Digital I/O.
CANRX		I	ST	CAN bus RX.
CTED2		I	ST	CTMU Edge 2 input.
INT3		I	ST	External Interrupt 3.
RB4/AN9/CTPLS/KBI0	20			
RB4		I/O	ST/ CMOS	Digital I/O.
AN9		I	Analog	Analog Input 9.
CTPLS		O	ST	CTMU pulse generator output.
KBI0		I	ST	Interrupt-on-change pin.
RB5/T0CKI/T3CKI/CCP5/ KBI1	21			
RB5		I/O	ST/ CMOS	Digital I/O.
T0CKI		I	ST	Timer0 external clock input.
T3CKI		I	ST	Timer3 external clock input.
CCP5		I/O	ST/ CMOS	Capture 5 input/Compare 5 output/PWM5 output.
KBI1		I	ST	Interrupt-on-change pin.

Legend: I^2C™ = I^2C/SMBus input buffer
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output

TABLE 1-6: PIC18F6XK80 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Num	Pin Type	Buffer Type	Description
				PORTG is a bidirectional I/O port.
RG0/RX1/DT1	6			
RG0		I/O	ST/ CMOS	Digital I/O.
RX1		I	ST	EUSART asynchronous receive.
DT1		I/O	ST	EUSART synchronous data. (See related TX2/CK2.)
RG1/CANTX2	7			
RG1		I/O	ST/ CMOS	Digital I/O.
CANTX2		O	CMOS	CAN bus complimentary transmit output or CAN bus time clock.
RG2/T3CKI	11			
RG2		I/O	ST/ CMOS	Digital I/O.
T3CKI		I	ST	Timer3 clock input.
RG3/TX1/CK1	12			
RG3		I/O	ST/ CMOS	Digital I/O.
TX1		O	CMOS	EUSART asynchronous transmit.
CK1		I/O	ST	EUSART synchronous clock. (See related RX2/DT2.)
RG4/T0CKI	18			
RG4		I/O	ST/ CMOS	Digital I/O.
T0CKI		I	ST	Timer0 external clock input.

Legend: I^2C™ = I^2C/SMBus input buffer
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output

TABLE 6-2: PIC18F66K80 FAMILY REGISTER FILE SUMMARY (CONTINUED)

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR on page
EA3h	B2EIDH	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	97
EA2h	B2SIDL	SID2	SID1	SID0	SRR	EXID	—	EID17	EID16	97
EA1h	B2SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	97
EA0h	B2CON	TXBIF	TXABT	TXLARB	TXERR	TXREQ	—	TXPRI1	TXPRI0	97
E9Fh	CANCON_RO8	CANCON_RO8								97
E9Eh	CANSTAT_RO8	CANSTAT_RO8								97
E9Dh	B1D7	B1D77	B1D76	B1D75	B1D71	B1D73	B1D72	B1D71	B1D70	97
E9Ch	B1D6	B1D67	B1D66	B1D65	B1D61	B1D63	B1D62	B1D61	B1D60	97
E9Bh	B1D5	B1D57	B1D56	B1D55	B1D51	B1D53	B1D52	B1D51	B1D50	97
E9Ah	B1D4	B1D47	B1D46	B1D45	B1D41	B1D43	B1D42	B1D41	B1D40	97
E99h	B1D3	B1D37	B1D36	B1D35	B1D31	B1D33	B1D32	B1D31	B1D30	97
E98h	B1D2	B1D27	B1D26	B1D25	B1D21	B1D23	B1D22	B1D21	B1D20	97
E97h	B1D1	B1D17	B1D16	B1D15	B1D11	B1D13	B1D12	B1D11	B1D10	97
E96h	B1D0	B1D07	B1D06	B1D05	B1D01	B1D03	B1D02	B1D01	B1D00	97
E95h	B1DLC	—	TXRTR	—	—	DLC3	DLC2	DLC1	DLC0	97
E94h	B1EIDL	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	97
E93h	B1EIDH	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	97
E92h	B1SIDL	SID2	SID1	SID0	SRR	EXID	—	EID17	EID16	97
E91h	B1SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	97
E90h	B1CON	TXBIF	TXABT	TXLARB	TXERR	TXREQ	RTREN	TXPRI1	TXPRI0	97
E90h	B1CON	RXFUL	RXM1	RXRTRRO	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0	97
E8Fh	CANCON_RO9	CANCON_RO9								97
E8Eh	CANSTAT_RO9	CANSTAT_RO9								97
E8Dh	B0D7	B0D77	B0D76	B0D75	B0D70	B0D73	B0D72	B0D71	B0D70	97
E8Ch	B0D6	B0D67	B0D66	B0D65	B0D60	B0D63	B0D62	B0D61	B0D60	97
E8Bh	B0D5	B0D57	B0D56	B0D55	B0D50	B0D53	B0D52	B0D51	B0D50	97
E8Ah	B0D4	B0D47	B0D46	B0D45	B0D40	B0D43	B0D42	B0D41	B0D40	97
E89h	B0D3	B0D37	B0D36	B0D35	B0D30	B0D33	B0D32	B0D31	B0D30	97
E88h	B0D2	B0D27	B0D26	B0D25	B0D20	B0D23	B0D22	B0D21	B0D20	98
E87h	B0D1	B0D17	B0D16	B0D15	B0D10	B0D13	B0D12	B0D11	B0D10	98
E86h	B0D0	B0D07	B0D06	B0D05	B0D00	B0D03	B0D02	B0D01	B0D00	98
E85h	B0DLC	—	RXRTR	RB1	RB0	DLC3	DLC2	DLC1	DLC0	98
E84h	B0EIDL	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	98
E83h	B0EIDH	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	98
E82h	B0SIDL	SID2	SID1	SID0	SRR	EXID	—	EID17	EID16	98
E81h	B0SIDH	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	98
E80h	B0CON	TXBIF	TXABT	TXLARB	TXERR	TXREQ	RTREN	TXPRI1	TXPRI0	98
E80h	B0CON	RTXFUL	RXM1	RXRTRRO	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0	98
E7Fh	TXBIE	—	—	—	CAN TX Buffer Interrupt Enable			—	—	98
E7Eh	BIE0	CAN Buffer Interrupt Enable								98
E7Dh	BSEL0	Mode Select Register 0						—	—	98
E7Ch	MSEL3	CAN Mask Select Register 3								98
E7Bh	MSEL2	CAN Mask Select Register 2								98
E7Ah	MSEL1	CAN Mask Select Register 1								98
E79h	MSEL0	CAN Mask Select Register 0								98
E78h	RXFBCON7	CAN Buffer 15/14 Pointer Register								98
E77h	RXFBCON6	CAN Buffer 13/12 Pointer Register								98
E76h	RXFBCON5	CAN Buffer 11/10 Pointer Register								98
E75h	RXFBCON4	CAN Buffer 9/8 Pointer Register								98
E74h	RXFBCON3	CAN Buffer 7/6 Pointer Register								98
E73h	RXFBCON2	CAN Buffer 5/4 Pointer Register								98

10.4 IPR Registers

The IPR registers contain the individual priority bits for the peripheral interrupts. Due to the number of peripheral interrupt sources, there are six Peripheral Interrupt Priority registers (IPR1 through IPR6). Using the priority bits requires that the Interrupt Priority Enable (IPEN) bit (RCON<7>) be set.

REGISTER 10-14: IPR1: PERIPHERAL INTERRUPT PRIORITY REGISTER 1

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PSPIP	ADIP	RC1IP	TX1IP	SSPIP	TMR1GIP	TMR2IP	TMR1IP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **PSPIP:** Parallel Slave Port Read/Write Interrupt Priority bit
1 = High priority
0 = Low priority

bit 6 **ADIP:** A/D Converter Interrupt Priority bit
1 = High priority
0 = Low priority

bit 5 **RC1IP:** EUSARTx Receive Interrupt Priority bit
1 = High priority
0 = Low priority

bit 4 **TX1IP:** EUSARTx Transmit Interrupt Priority bit
1 = High priority
0 = Low priority

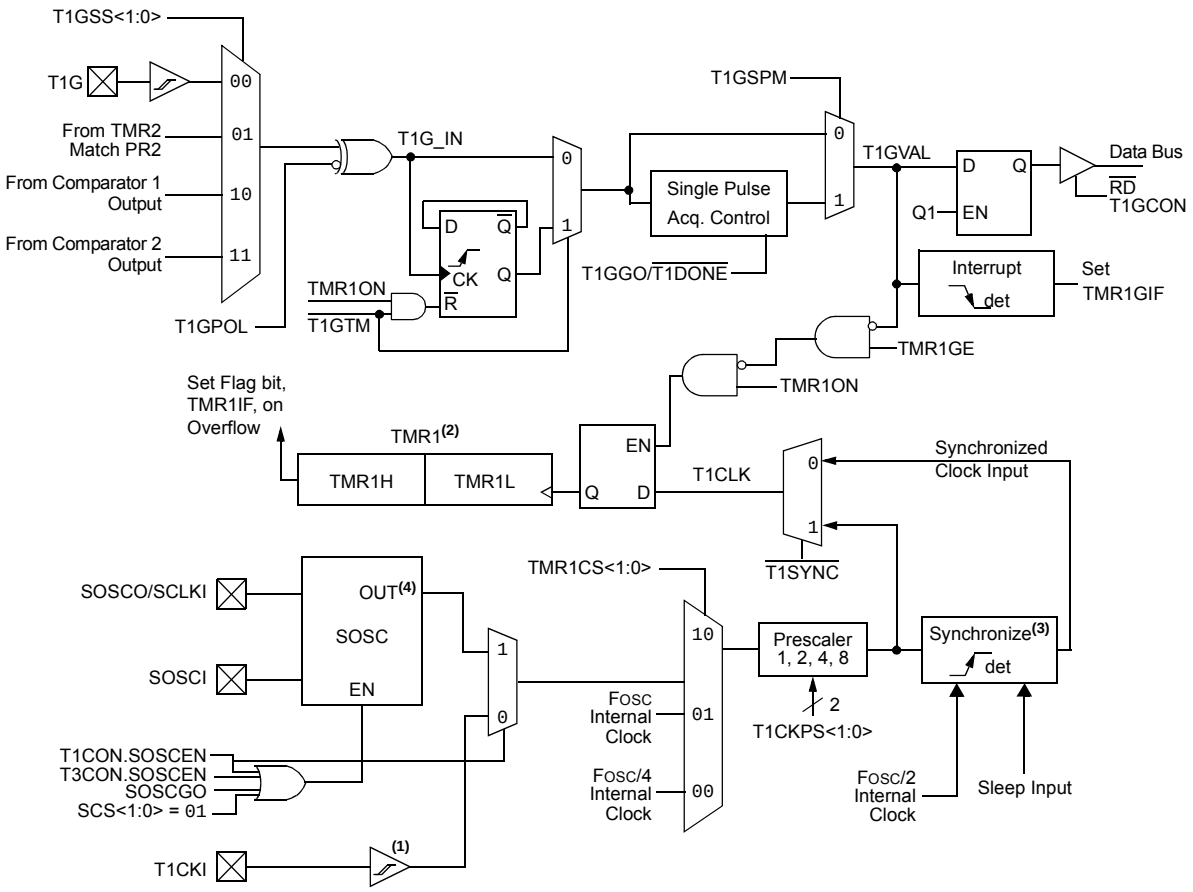
bit 3 **SSPIP:** Master Synchronous Serial Port Interrupt Priority bit
1 = High priority
0 = Low priority

bit 2 **TMR1GIP:** Timer1 Gate Interrupt Priority bit
1 = High priority
0 = Low priority

bit 1 **TMR2IP:** TMR2 to PR2 Match Interrupt Priority bit
1 = High priority
0 = Low priority

bit 0 **TMR1IP:** TMR1 Overflow Interrupt Priority bit
1 = High priority
0 = Low priority

FIGURE 14-1: TIMER1 BLOCK DIAGRAM



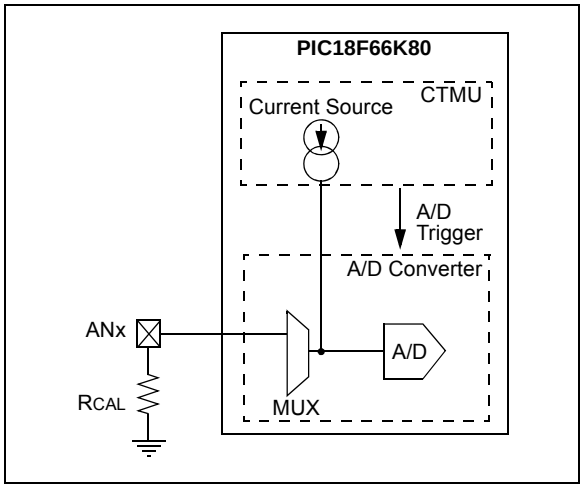
Note 1: ST Buffer is high-speed type when using T1CKI.
2: Timer1 register increments on rising edge.
3: Synchronize does not operate while in Sleep.
4: The output of SOSC is determined by the SOSCSEL<1:0> Configuration bits.

The CTMU current source may be trimmed with the trim bits in CTMUICON, using an iterative process to get the exact current desired. Alternatively, the nominal value without adjustment may be used. That value may be stored by software, for use in all subsequent capacitive or time measurements.

To calculate the optimal value for RCAL, the nominal current must be chosen.

For example, if the A/D Converter reference voltage is 3.3V, use 70% of full scale (or 2.31V) as the desired approximate voltage to be read by the A/D Converter. If the range of the CTMU current source is selected to be 0.55 μA, the resistor value needed is calculated as RCAL = 2.31V/0.55 μA, for a value of 4.2 MΩ. Similarly, if the current source is chosen to be 5.5 μA, RCAL would be 420,000Ω, and 42,000Ω if the current source is set to 55 μA.

FIGURE 18-2: CTMU CURRENT SOURCE CALIBRATION CIRCUIT



A value of 70% of full-scale voltage is chosen to make sure that the A/D Converter is in a range that is well above the noise floor. If an exact current is chosen to incorporate the trimming bits from CTMUICON, the resistor value of RCAL may need to be adjusted accordingly. RCAL also may be adjusted to allow for available resistor values. RCAL should be of the highest precision available, in light of the precision needed for the circuit that the CTMU will be measuring. A recommended minimum would be 0.1% tolerance.

The following examples show a typical method for performing a CTMU current calibration.

- Example 18-1 demonstrates how to initialize the A/D Converter and the CTMU.

  This routine is typical for applications using both modules.

- Example 18-2 demonstrates one method for the actual calibration routine.

  This method manually triggers the A/D Converter to demonstrate the entire step-wise process. It is also possible to automatically trigger the conversion by setting the CTMU's CTTRIG bit (CTMUCONH<0>).

20.4.2.1 Direction Change in Full-Bridge Mode

In the Full-Bridge mode, the P1M1 bit in the CCP1CON register allows users to control the forward/reverse direction. When the application firmware changes this direction control bit, the module will change to the new direction on the next PWM cycle.

A direction change is initiated in software by changing the P1M1 bit of the CCP1CON register. The following sequence occurs prior to the end of the current PWM period:

- The modulated outputs (P1B and P1D) are placed in their inactive state.
- The associated unmodulated outputs (P1A and P1C) are switched to drive in the opposite direction.
- PWM modulation resumes at the beginning of the next period.

For an illustration of this sequence, see Figure 20-10.

The Full-Bridge mode does not provide a dead-band delay. As one output is modulated at a time, a dead-band delay is generally not required. There is a situation where a dead-band delay is required. This situation occurs when both of the following conditions are true:

- The direction of the PWM output changes when the duty cycle of the output is at or near 100%.
- The turn-off time of the power switch, including the power device and driver circuit, is greater than the turn-on time.

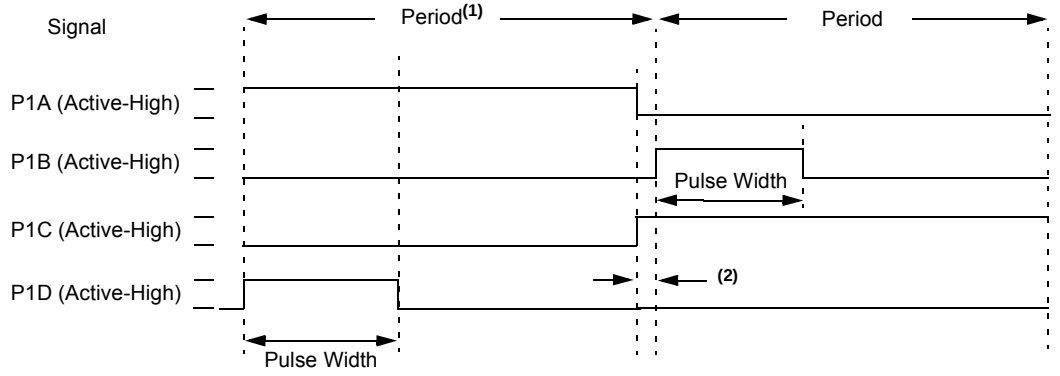
Figure 20-11 shows an example of the PWM direction changing from forward to reverse, at a near 100% duty cycle. In this example, at time, t1, the P1A and P1D outputs become inactive, while the P1C output becomes active. Since the turn-off time of the power devices is longer than the turn-on time, a shoot-through current will flow through power devices, QC and QD (see Figure 20-8), for the duration of ‘t’. The same phenomenon will occur to power devices, QA and QB, for PWM direction change from reverse to forward.

If changing PWM direction at high duty cycle is required for an application, two possible solutions for eliminating the shoot-through current are:

- Reduce PWM duty cycle for one PWM period before changing directions.
- Use switch drivers that can drive the switches off faster than they can drive them on.

Other options to prevent shoot-through current may exist.

FIGURE 20-10: EXAMPLE OF PWM DIRECTION CHANGE



Note 1: The direction bit, P1M1 of the CCP1CON register, is written any time during the PWM cycle.

2: When changing directions, the P1A and P1C signals switch before the end of the current PWM cycle. The modulated P1B and P1D signals are inactive at this time. The length of this time is: (1/FOSC) • TMR2 Prescale Value.

21.4.14 SLEEP OPERATION

While in Sleep mode, the I^2C module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

21.4.15 EFFECTS OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

21.4.16 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I^2C bus may be taken when the P bit (SSPSTAT<4>) is set, or the bus is Idle, with both the S and P bits clear. When the bus is busy, enabling the MSSP interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed in hardware with the result placed in the BCLIF bit.

The states where arbitration can be lost are:

- Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

21.4.17 MULTI -MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a '1' on SDA, by letting SDA float high, and another master asserts a '0'. When the SCL pin floats high, data should be stable. If the expected data on SDA is a '1' and the data sampled on the SDA pin = 0, then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCLIF, and reset the I^2C port to its Idle state (Figure 21-27).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDA and SCL lines are deasserted and the SSPBUF can be written to. When the user services the bus collision Interrupt Service Routine and if the I^2C bus is free, the user can resume communication by asserting a Start condition.

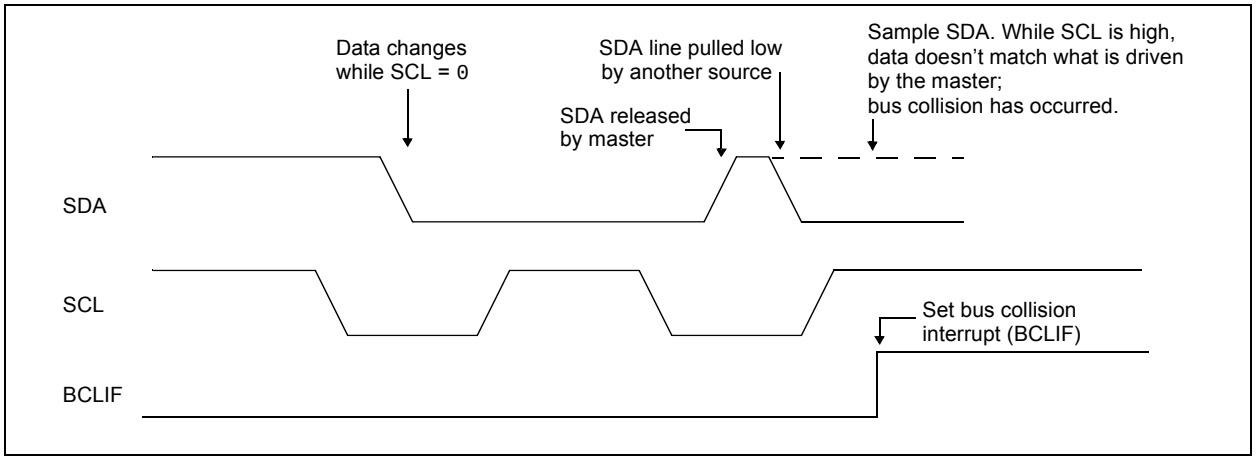
If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDA and SCL lines are deasserted and the respective control bits in the SSPCON2 register are cleared. When the user services the bus collision Interrupt Service Routine, and if the I^2C bus is free, the user can resume communication by asserting a Start condition.

The master will continue to monitor the SDA and SCL pins. If a Stop condition occurs, the SSPIF bit will be set.

A write to the SSPBUF will start the transmission of data at the first data bit regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I^2C bus can be taken when the P bit is set in the SSPSTAT register, or the bus is Idle and the S and P bits are cleared.

FIGURE 21-27: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE



22.2 Baud Rate Generator (BRG)

The BRG is a dedicated, 8-bit or 16-bit generator that supports both the Asynchronous and Synchronous modes of the EUSARTx. By default, the BRG operates in 8-bit mode; setting the BRG16 bit (BAUDCONx<3>) selects 16-bit mode.

The SPBRGHx:SPBRGx register pair controls the period of a free-running timer. In Asynchronous mode, bits, BRGH (TXSTAx<2>) and BRG16 (BAUDCONx<3>), also control the baud rate. In Synchronous mode, BRGH is ignored. Table 22-2 shows the formula for computation of the baud rate for different EUSARTx modes which only apply in Master mode (internally generated clock).

Given the desired baud rate and FOSC, the nearest integer value for the SPBRGHx:SPBRGx registers can be calculated using the formulas in Table 22-2. From this, the error in baud rate can be determined. An example calculation is shown in Example 22-1. Typical baud rates and error values for the various Asynchronous modes are shown in Table 22-3. It may be advantageous to use the high baud rate (BRGH = 1) or the 16-bit BRG to reduce the baud rate error, or achieve a slow baud rate for a fast oscillator frequency.

Writing a new value to the SPBRGHx:SPBRGx registers causes the BRG timer to be reset (or cleared). This ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

22.2.1 OPERATION IN POWER-MANAGED MODES

The device clock is used to generate the desired baud rate. When one of the power-managed modes is entered, the new clock source may be operating at a different frequency. This may require an adjustment to the value in the SPBRGHx:SPBRGx register pair.

22.2.2 SAMPLING

The data on the RXx pin (either RC7/CANRX/RX1/DT1 or RB7/PGD/T3G/RX2/DT2/KBI3) is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RXx pin.

TABLE 22-2: BAUD RATE FORMULAS

Configuration Bits			BRG/EUSARTx Mode	Baud Rate Formula
SYNC	BRG16	BRGH		
0	0	0	8-bit/Asynchronous	FOSC/[64 (n + 1)]
0	0	1	8-bit/Asynchronous	FOSC/[16 (n + 1)]
0	1	0	16-bit/Asynchronous	
0	1	1	16-bit/Asynchronous	FOSC/[4 (n + 1)]
1	0	x	8-bit/Synchronous	
1	1	x	16-bit/Synchronous	

Legend: x = Don't care, n = value of SPBRGHx:SPBRGx register pair

22.3.4.2 Special Considerations Using the WUE Bit

The timing of WUE and RCxIF events may cause some confusion when it comes to determining the validity of received data. As noted, setting the WUE bit places the EUSARTx in an Idle mode. The wake-up event causes a receive interrupt by setting the RCxIF bit. The WUE bit is cleared after this when a rising edge is seen on RXx/DTx. The interrupt condition is then cleared by reading the RCREGx register. Ordinarily, the data in RCREGx will be dummy data and should be discarded.

The fact that the WUE bit has been cleared (or is still set) and the RCxIF flag is set should not be used as an indicator of the integrity of the data in RCREGx. Users should consider implementing a parallel method in firmware to verify received data integrity.

To assure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.

FIGURE 22-8: AUTO-WAKE-UP BIT (WUE) TIMINGS DURING NORMAL OPERATION

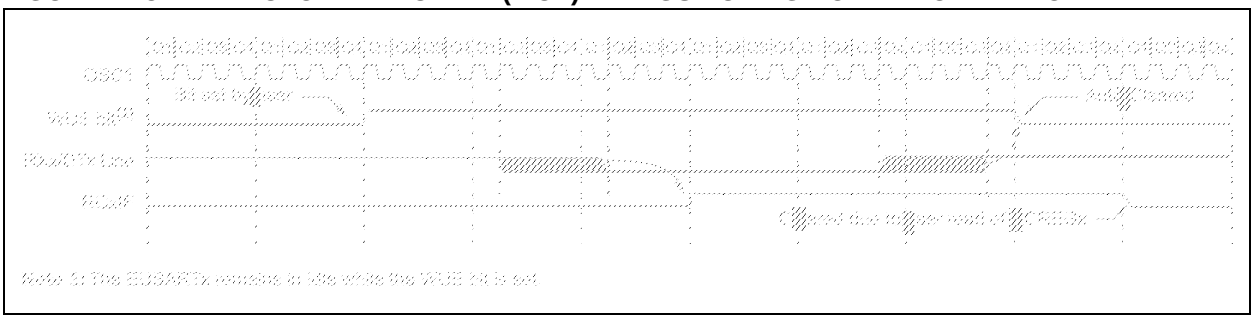
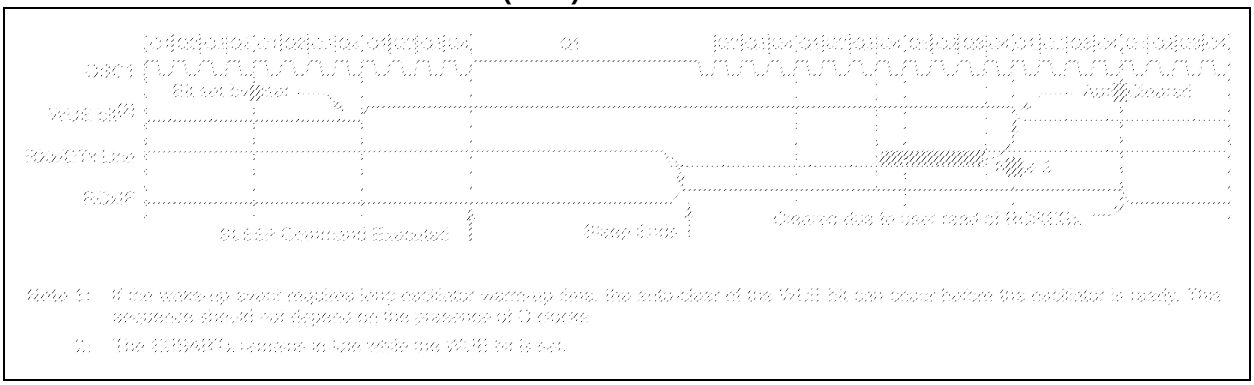


FIGURE 22-9: AUTO-WAKE-UP BIT (WUE) TIMINGS DURING SLEEP



23.8 Use of the Special Event Triggers

A/D conversion can be started by the Special Event Trigger of any of these modules:

- CCP2 – Requires CCP2M<3:0> bits (CCP2CON<3:0>) set at '1011'(†)
- ECCP1
- CTMU – Requires the setting of the CTTRIG bit (CTMUCONH<0>)
- Timer1

To start an A/D conversion:

- The A/D module must be enabled (ADON = 1)
- The appropriate analog input channel selected
- The minimum acquisition period set one of these ways:
  - Timing provided by the user
  - Selection made of an appropriate TACQ time

With these conditions met, the trigger sets the GO/$\overline{\text{DONE}}$ bit and the A/D acquisition starts.

If the A/D module is not enabled (ADON = 0), the module ignores the Special Event Trigger.

Note:	With an ECCP1 or CCP2 trigger, Timer1 or Timer3 is cleared. The timers reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH:ADRESL to the desired location). If the A/D module is not enabled, the Special Event Trigger is ignored by the module, but the timer's counter resets.

23.9 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined, in part, by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the ACQT<2:0> and ADCS<2:0> bits in ADCON2 should be updated in accordance with the power-managed mode clock that will be used.

After the power-managed mode is entered (either of the power-managed Run modes), an A/D acquisition or conversion may be started. Once an acquisition or conversion is started, the device should continue to be clocked by the same power-managed mode clock source until the conversion has been completed. If desired, the device may be placed into the corresponding power-managed Idle mode during the conversion.

If the power-managed mode clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires that the A/D RC clock be selected. If bits, ACQT<2:0>, are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the SLEEP instruction and entry into Sleep mode. The IDLEN and SCS<1:0> bits in the OSCCON register must have already been cleared prior to starting the conversion.

REGISTER 24-2: CMSTAT: COMPARATOR STATUS REGISTER

R-x	R-x	U-0	U-0	U-0	U-0	U-0	U-0
CMP2OUT	CMP1OUT	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **CMP2OUT:CMP1OUT:** Comparator x Status bits

If CPOL (CMxCON<5>)= 0 (non-inverted polarity):

1 = Comparator x's VIN+ > VIN-

0 = Comparator x's VIN+ < VIN-

If CPOL = 1 (inverted polarity):

1 = Comparator x's VIN+ < VIN-

0 = Comparator x's VIN+ > VIN-

bit 4-0 **Unimplemented:** Read as '0'

REGISTER 27-49: MSEL1: MASK SELECT REGISTER 1(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
FIL7_1	FIL7_0	FIL6_1	FIL6_0	FIL5_1	FIL5_0	FIL4_1	FIL4_0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **FIL7_<1:0>:** Filter 7 Select bits 1 and 0
- 11 = No mask
- 10 = Filter 15
- 01 = Acceptance Mask 1
- 00 = Acceptance Mask 0

bit 5-4 **FIL6_<1:0>:** Filter 6 Select bits 1 and 0
- 11 = No mask
- 10 = Filter 15
- 01 = Acceptance Mask 1
- 00 = Acceptance Mask 0

bit 3-2 **FIL5_<1:0>:** Filter 5 Select bits 1 and 0
- 11 = No mask
- 10 = Filter 15
- 01 = Acceptance Mask 1
- 00 = Acceptance Mask 0

bit 1-0 **FIL4_<1:0>:** Filter 4 Select bits 1 and 0
- 11 = No mask
- 10 = Filter 15
- 01 = Acceptance Mask 1
- 00 = Acceptance Mask 0

Note 1: This register is available in Mode 1 and 2 only.

REGISTER 27-58: IPR5: PERIPHERAL INTERRUPT PRIORITY REGISTER 5

Mode 0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	IRXIP	WAKIP	ERRIP	TXB2IP	TXB1IP(1)	TXB0IP(1)	RXB1IP	RXB0IP

Mode 1,2	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	IRXIP	WAKIP	ERRIP	TXBnIP	TXB1IP(1)	TXB0IP(1)	RXBnIP	FIFOWMIP
	bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IRXIP:** CAN Bus Error Message Received Interrupt Priority bit
1 = High priority
0 = Low priority

bit 6 **WAKIP:** CAN Bus Activity Wake-up Interrupt Priority bit
1 = High priority
0 = Low priority

bit 5 **ERRIP:** CAN Module Error Interrupt Priority bit
1 = High priority
0 = Low priority

bit 4 When CAN is in Mode 0:
TXB2IP: CAN Transmit Buffer 2 Interrupt Priority bit
1 = High priority
0 = Low priority
When CAN is in Mode 1 or 2:
TXBnIP: CAN Transmit Buffer Interrupt Priority bit
1 = High priority
0 = Low priority

bit 3 **TXB1IP:** CAN Transmit Buffer 1 Interrupt Priority bit(1)
1 = High priority
0 = Low priority

bit 2 **TXB0IP:** CAN Transmit Buffer 0 Interrupt Priority bit(1)
1 = High priority
0 = Low priority

bit 1 When CAN is in Mode 0:
RXB1IP: CAN Receive Buffer 1 Interrupt Priority bit
1 = High priority
0 = Low priority
When CAN is in Mode 1 or 2:
RXBnIP: CAN Receive Buffer Interrupts Priority bit
1 = High priority
0 = Low priority

bit 0 When CAN is in Mode 0:
RXB0IP: CAN Receive Buffer 0 Interrupt Priority bit
1 = High priority
0 = Low priority
When CAN is in Mode 1:
Unimplemented: Read as '0'
When CAN is in Mode 2:
FIFOWMIP: FIFO Watermark Interrupt Priority bit
1 = High priority
0 = Low priority

Note 1: In CAN Mode 1 and 2, these bits are forced to '0'.

REGISTER 27-59: TXBIE: TRANSMIT BUFFERS INTERRUPT ENABLE REGISTER(1)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	—	TXB2IE(2)	TXB1IE(2)	TXB0IE(2)	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-2 **TXB2IE:TXB0IE:** Transmit Buffer 2-0 Interrupt Enable bits(2)
1 = Transmit buffer interrupt is enabled
0 = Transmit buffer interrupt is disabled

bit 1-0 **Unimplemented:** Read as '0'

Note 1: This register is available in Mode 1 and 2 only.
2: TXBnIE in PIE5 register must be set to get an interrupt.

REGISTER 27-60: BIE0: BUFFER INTERRUPT ENABLE REGISTER 0(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
B5IE(2)	B4IE(2)	B3IE(2)	B2IE(2)	B1IE(2)	B0IE(2)	RXB1IE(2)	RXB0IE(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **B<5:0>IE:** Programmable Transmit/Receive Buffer 5-0 Interrupt Enable bits(2)
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1-0 **RXB<1:0>IE:** Dedicated Receive Buffer 1-0 Interrupt Enable bits(2)
1 = Interrupt is enabled
0 = Interrupt is disabled

Note 1: This register is available in Mode 1 and 2 only.
2: Either TXBnIE or RXBnIE, in the PIE5 register, must be set to get an interrupt.

28.3 On-Chip Voltage Regulator

All of the PIC18F66K80 family devices power their core digital logic at a nominal 3.3V. For designs that are required to operate at a higher typical voltage, such as 5V, all family devices incorporate two on-chip regulators that allows the device to run its core logic from VDD. Those regulators are:

- Normal on-chip regulator
- Ultra Low-Power, on-chip regulator

The hardware configuration of these regulators are the same and are explained in **Section 28.3.1 "Regulator Enable Mode (PIC18FXXKXX devices)"**. The regulators' only differences relate to when the device enters Sleep, as explained in **Section 28.3.1 "Regulator Enable Mode (PIC18FXXKXX devices)"**.

28.3.1 REGULATOR ENABLE MODE (PIC18FXXKXX DEVICES)

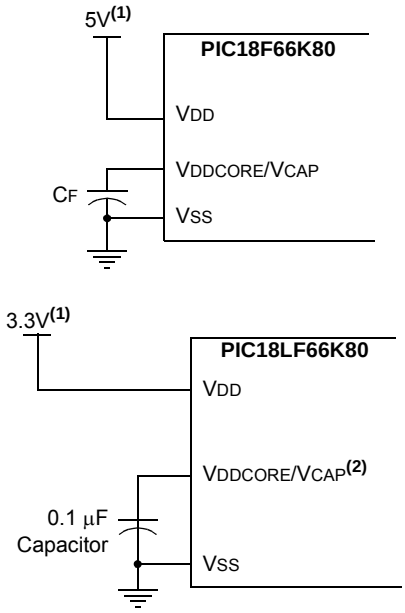
On PIC18FXXKXX devices, the regulator is enabled and a low-ESR filter capacitor must be connected to the VDDCORE/VCAP pin (see Figure 28-2). This helps maintain the regulator's stability. The recommended value for the filter capacitor is given in **Section 31.1 "DC Characteristics: Supply Voltage PIC18F66K80 Family (Industrial/Extended)"**.

28.3.2 REGULATOR DISABLE MODE (PIC18LFXXKXX DEVICES)

On PIC18**LF**XXKXX devices, the regulator is disabled and the power to the core is supplied directly by VDD. The voltage levels for VDD must not exceed the specified VDDCORE levels. A 0.1 μF capacitor should be connected to the VDDCORE/VCAP pin.

On the PIC18FXXKXX devices, the overall voltage budget is very tight. The regulator should operate the device down to 1.8V. When VDD drops below 3.3V, the regulator no longer regulates, but the output voltage follows the input until VDD reaches 1.8V. Below this voltage, the output of the regulator output may drop to 0V.

FIGURE 28-2: CONNECTIONS FOR THE F AND LF PARTS



Note 1: These are typical operating voltages. For the full operating ranges of VDD and VDDCORE, see **Section 31.1 "DC Characteristics: Supply Voltage PIC18F66K80 Family (Industrial/Extended)"**.

2: When the regulator is disabled, VDDCORE/VCAP must be connected to a 0.1 μF capacitor.

XORWF **Exclusive OR W with f**

Syntax: XORWF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (W) .XOR. (f) → dest

Status Affected: N, Z

Encoding:

0001	10da	ffff	ffff

Description: Exclusive OR the contents of W with register 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in the register 'f' (default).

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: `XORWF REG, 1, 0`

Before Instruction
REG = AFh
W = B5h
After Instruction
REG = 1Ah
W = B5h

31.2 DC Characteristics: Power-Down and Supply Current PIC18F66K80 Family (Industrial/Extended) (Continued)

PIC18F66K80 Family (Industrial/Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD) Cont.(2,3)						
	PIC18**LF**XXK80	330	480	µA	-40°C	VDD = 1.8V(4) Regulator Disabled	FOSC = 4 MHz (**RC_IDLE** mode, Internal HF-INTOSC)
		330	480	µA	+25°C		
		330	480	µA	+60°C		
		340	500	µA	+85°C		
		350	540	µA	+125°C		
	PIC18**LF**XXK80	522	720	µA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		522	720	µA	+25°C		
		522	720	µA	+60°C		
		540	740	µA	+85°C		
		550	780	µA	+125°C		
	PIC18**F**XXK80	540	760	µA	-40°C	VDD = 3.3V(5) Regulator Enabled	
		540	760	µA	+25°C		
		540	760	µA	+60°C		
		560	780	µA	+85°C		
		580	810	µA	+125°C		
	PIC18**F**XXK80	600	1250	µA	-40°C	VDD = 5V(5) Regulator Enabled	
		600	1250	µA	+25°C		
		600	1250	µA	+60°C		
		610	1300	µA	+85°C		
		620	1340	µA	+125°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to VDD or VSS, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;

$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

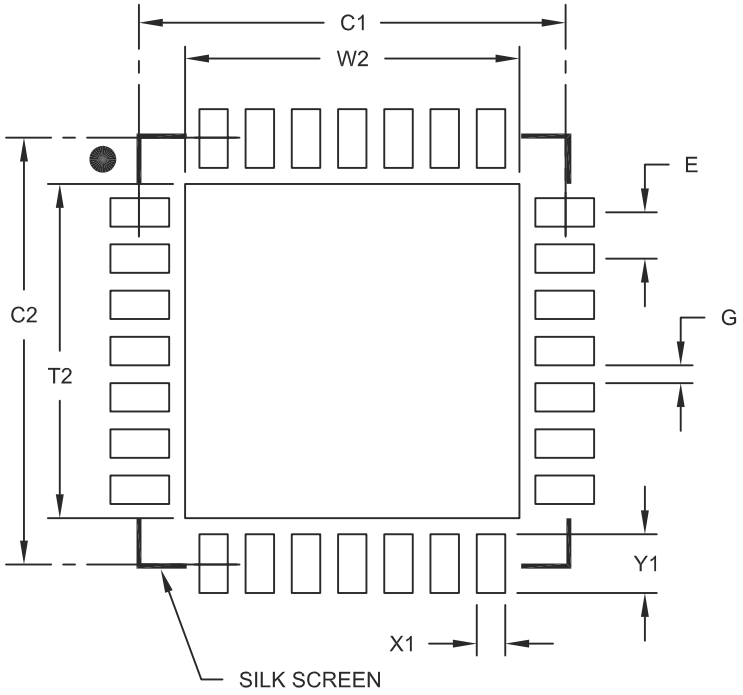
3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: For LF devices, $\overline{RETEN}$ (CONFIG1L<0>) = 1.

5: For F devices, SRETEN (WDTCON<4>) = 1 and $\overline{RETEN}$ (CONFIG1L<0>) = 0.

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (X28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A