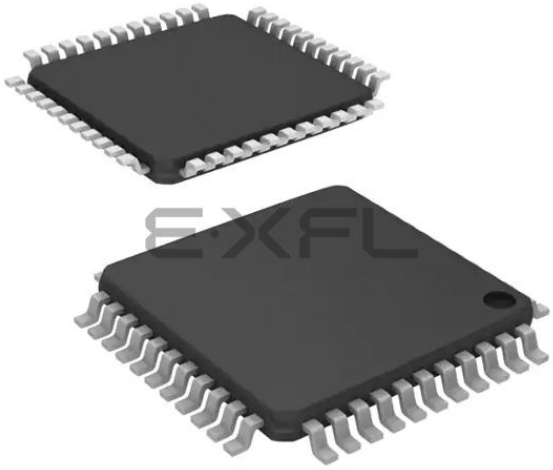

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	ECANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.6K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 11x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f46k80-h-pt

TABLE 1-5: PIC18F4XK80 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PDIP	QFN/ TQFP			
					PORTA is a bidirectional I/O port.
RA0/CVREF/AN0/ULPWU	2	19			
RA0			I/O	ST/ CMOS	General purpose I/O pin.
CVREF			O	Analog	Comparator reference voltage output.
AN0			I	Analog	Analog Input 0.
ULPWU			I	Analog	Ultra Low-Power Wake-up input.
RA1/AN1/C1INC	3	20			
RA1			I/O	ST/ CMOS	Digital I/O.
AN1			I	Analog	Analog Input 1.
C1INC			I	Analog	Comparator 1 Input C.
RA2/VREF-/AN2/C2INC	4	21			
RA2			I/O	ST/ CMOS	Digital I/O.
VREF-			I	Analog	A/D reference voltage (low) input.
AN2			I	Analog	Analog Input 2.
C2INC			I	Analog	Comparator 2 Input C.
RA3/VREF+/AN3	5	22			
RA3			I/O	ST/ CMOS	Digital I/O.
VREF+			I	Analog	A/D reference voltage (high) input.
AN3			I	Analog	Analog Input 3.
RA5/AN4/HLVDIN/T1CKI/ $\overline{SS}$	7	24			
RA5			I/O	ST/ CMOS	Digital I/O.
AN4			I	Analog	Analog Input 4.
HLVDIN			I	Analog	High/Low-Voltage Detect input.
T1CKI			I	ST	Timer1 clock input.
$\overline{SS}$			I	ST	SPI slave select input.

Legend: I^2C™ = I^2C/SMBus input buffer
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output

TABLE 1-5: PIC18F4XK80 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PDIP	QFN/ TQFP			
					PORTC is a bidirectional I/O port.
RC0/SOSCO/SCLKI	15	32			
RC0			I/O	ST/ CMOS	Digital I/O.
SOSCO			I	ST	SOSC oscillator output.
SCLKI			I	ST	Digital SOSC input.
RC1/SOSCI	16	35			
RC1			I/O	ST/ CMOS	Digital I/O.
SOSCI			I	CMOS	SOSC oscillator input.
RC2/T1G/CCP2	17	36			
RC2			I/O	ST/ CMOS	Digital I/O.
T1G			I	ST	Timer1 external clock gate input.
CCP2			I/O	ST/ CMOS	Capture 2 input/Compare 2 output/PWM2 output.
RC3/REFO/SCL/SCK	18	37			
RC3			I/O	ST/ CMOS	Digital I/O.
REFO			O	CMOS	Reference clock out.
SCL			I/O	I^2C	Synchronous serial clock input/output for I^2C mode.
SCK			I/O	ST	Synchronous serial clock input/output for SPI mode.
RC4/SDA/SDI	23	42			
RC4			I/O	ST/ CMOS	Digital I/O.
SDA			I/O	I^2C	I^2C data input/output.
SDI			I	ST	SPI data in.
RC5/SDO	24	43			
RC5			I/O	ST/ CMOS	Digital I/O.
SDO			O	CMOS	SPI data out.
RC6/CANTX/TX1/CK1/ CCP3	25	44			
RC6			I/O	ST/ CMOS	Digital I/O.
CANTX			O	CMOS	CAN bus TX.
TX1			O	CMOS	EUSART synchronous transmit.
CK1			I/O	ST	EUSART synchronous clock. (See related RX2/DT2.)
CCP3			I/O	ST	Capture 3 input/Compare 3 output/PWM3 output.

Legend: I^2C™ = I^2C/SMBus input buffer
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output

2.0 GUIDELINES FOR GETTING STARTED WITH PIC18FXXKXX MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC18F66K80 family family of 8-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Power Supply Pins"**)
- All AVDD and AVSS pins, regardless of whether or not the analog device features are used
  (see **Section 2.2 "Power Supply Pins"**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.3 "Master Clear (MCLR) Pin"**)
- ENVREG (if implemented) and VCAP/VDDCORE pins
  (see **Section 2.4 "Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)"**)

These pins must also be connected if they are being used in the end application:

- PGC/PGD pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP Pins"**)
- OSCI and OSCO pins when an external oscillator source is used
  (see **Section 2.6 "External Oscillator Pins"**)

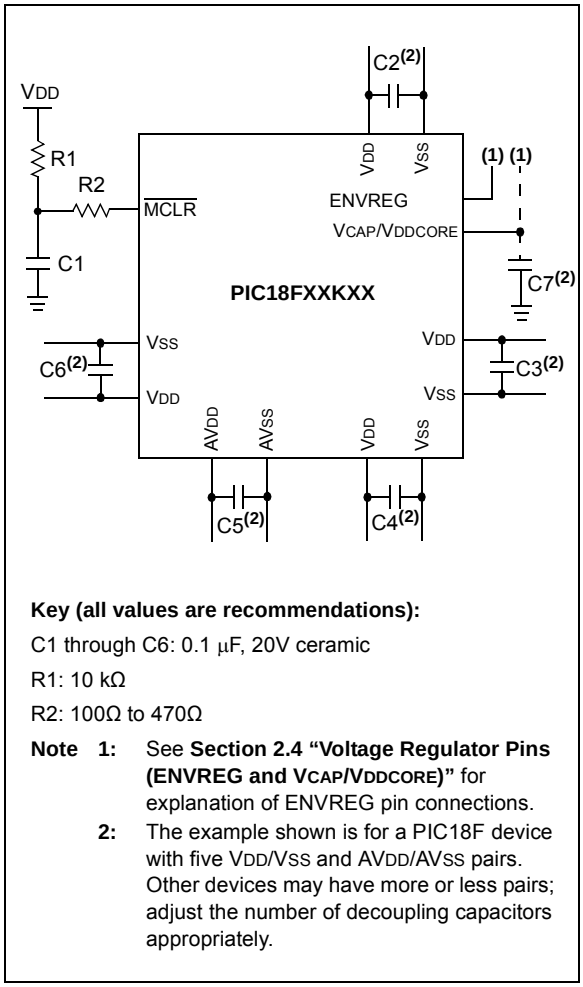
Additionally, the following pins may be required:

- VREF+/VREF- pins are used when external voltage reference for analog modules is implemented

Note:	The AVDD and AVSS pins must always be connected, regardless of whether any of the analog modules are being used.

The minimum mandatory connections are shown in Figure 2-1.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS



Key (all values are recommendations):

C1 through C6: 0.1 μF, 20V ceramic

R1: 10 kΩ

R2: 100Ω to 470Ω

Note 1: See **Section 2.4 "Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)"** for explanation of ENVREG pin connections.

2: The example shown is for a PIC18F device with five VDD/VSS and AVDD/AVSS pairs. Other devices may have more or less pairs; adjust the number of decoupling capacitors appropriately.

4.6 Exiting Idle and Sleep Modes

An exit from Sleep mode or any of the Idle modes is triggered by an interrupt, a Reset or a WDT time-out. This section discusses the triggers that cause exits from power-managed modes. The clocking subsystem actions are discussed in each of the power-managed modes (see **Section 4.2 "Run Modes", Section 4.3 "Sleep Mode"** and **Section 4.4 "Idle Modes"**).

4.6.1 EXIT BY INTERRUPT

Any of the available interrupt sources can cause the device to exit from an Idle mode or Sleep mode to a Run mode. To enable this functionality, an interrupt source must be enabled by setting its enable bit in one of the INTCONx or PIEx registers. The exit sequence is initiated when the corresponding interrupt flag bit is set.

On all exits from Idle or Sleep modes by interrupt, code execution branches to the interrupt vector if the GIE/GIEH bit (INTCON<7>) is set. Otherwise, code execution continues or resumes without branching (see **Section 10.0 "Interrupts"**).

4.6.2 EXIT BY WDT TIME-OUT

A WDT time-out will cause different actions depending on which power-managed mode the device is in when the time-out occurs.

If the device is not executing code (all Idle modes and Sleep mode), the time-out will result in an exit from the power-managed mode (see **Section 4.2 "Run Modes"** and **Section 4.3 "Sleep Mode"**). If the device is executing code (all Run modes), the time-out will result in a WDT Reset (see **Section 28.2 "Watchdog Timer (WDT)"**).

Executing a SLEEP or CLRWDT instruction clears the WDT timer and postscaler, loses the currently selected clock source (if the Fail-Safe Clock Monitor is enabled) and modifies the IRCFx bits in the OSCCON register (if the internal oscillator block is the device clock source).

4.6.3 EXIT BY RESET

Normally, the device is held in Reset by the Oscillator Start-up Timer (OST) until the primary clock becomes ready. At that time, the OSTS bit is set and the device begins executing code. If the internal oscillator block is the new clock source, the HFIOFS/MFIOFS bits are set instead.

The exit delay time from Reset to the start of code execution depends on both the clock sources before and after the wake-up, and the type of oscillator, if the new clock source is the primary clock. Exit delays are summarized in Table 4-4.

Code execution can begin before the primary clock becomes ready. If either the Two-Speed Start-up (see **Section 28.4 "Two-Speed Start-up"**) or Fail-Safe Clock Monitor (see **Section 28.5 "Fail-Safe Clock Monitor"**) is enabled, the device may begin execution as soon as the Reset source has cleared. Execution is clocked by the INTOSC multiplexer driven by the internal oscillator block. Execution is clocked by the internal oscillator block until either the primary clock becomes ready or a power-managed mode is entered before the primary clock becomes ready; the primary clock is then shut down.

4.6.4 EXIT WITHOUT AN OSCILLATOR START-UP DELAY

Certain exits from power-managed modes do not invoke the OST at all. The two cases are:

- When in PRI_IDLE mode, where the primary clock source is not stopped
- When the primary clock source is not any of the LP, XT, HS or HSPLL modes

In these instances, the primary clock source either does not require an oscillator start-up delay, since it is already running (PRI_IDLE), or normally, does not require an oscillator start-up delay (RC, EC and INTIO Oscillator modes). However, a fixed delay of interval, TCSD, following the wake event is still required when leaving Sleep and Idle modes to allow the CPU to prepare for execution. Instruction execution resumes on the first clock cycle following this delay.

11.8 PORTG, TRISG and LATG Registers

PORTG is a 5-bit wide, bidirectional port. The corresponding Data Direction and Output Latch registers are TRISG and LATG.

Note:	PORTG is only available on 64-pin devices.

PORTG is multiplexed with EUSARTx and CCP, ECCP, Analog, Comparator and Timer input functions (Table 11-13). When operating as I/O, all PORTG pins have Schmitt Trigger input buffers. The open-drain functionality for the EUARTx can be configured using ODCON.

Each of the PORTG pins has a weak internal pull-up. A single control bit can turn off all the pull-ups. This is performed by clearing bit, RGPU (PADCFG1<4>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on any device Reset.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTG pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. The user should refer to the corresponding peripheral section for the correct TRIS bit settings. The pin override value is not loaded into the TRIS register. This allows read-modify-write of the TRIS register without concern due to peripheral overrides.

EXAMPLE 11-7: INITIALIZING PORTG

```
CLRF    PORTG           ; Initialize PORTG by
                        ; clearing output
                        ; data latches
CLRF    LATG            ; Alternate method
                        ; to clear output
                        ; data latches
MOVLW   04h             ; Value used to
                        ; initialize data
                        ; direction
MOVWF   TRISG           ; Set RG1:RG0 as
                        ; outputs
                        ; RG2 as input
                        ; RG4:RG3 as inputs
```

TABLE 11-13: PORTG FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RG0/RX1/DT1	RG0	0	O	DIG	LATG<0> data output.
		1	I	ST	PORTG<0> data input.
	RX1	1	I	ST	Asynchronous serial receive data input (EUSARTx module).
	DT1	0	O	DIG	Synchronous serial data output (EUSARTx module); takes priority over port data.
		1	I	ST	Synchronous serial data input (EUSARTx module); user must configure as an input.
RG1/CANTX	RG1	0	O	DIG	LATG<1> data output.
		1	I	ST	PORTG<1> data input.
	CANTX	0	O	DIG	CAN bus TX.
RG2/T3CKI	RG2	0	O	DIG	LATG<2> data output.
		1	I	ST	PORTG<2> data input.
	T3CKI(2)	x	I	ST	Timer3 clock input.
RG3/TX1/CK1	RG3	0	O	DIG	LATG<3> data output.
		1	I	ST	PORTG<3> data input.
	TX1	0	O	DIG	Asynchronous serial data output (EUSARTx module); takes priority over port data.
	CK1	0	O	DIG	Synchronous serial clock output (EUSARTx module); user must configure as an input.
		1	I	ST	Synchronous serial clock input (EUSARTx module); user must configure as an input.
RG4/T0CKI	RG4	0	O	DIG	LATG<4> data output.
		1	I	ST	PORTG<4> data input.
	T0CKI(1)	x	I	ST	Timer0 clock input.

Legend: O = Output; I = Input; ANA = Analog Signal; DIG = CMOS Output; ST = Schmitt Trigger Buffer Input; x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

Note 1: This is the alternate pin assignment for T0CKI on 64-pin devices when the T0CKMX Configuration bit is cleared.

2: This is the default pin assignment for T3CKI on 64-pin devices when the T3CKMX Configuration bit is set.

REGISTER 12-3: MDCARH: MODULATION HIGH CARRIER CONTROL REGISTER

R/W-0	R/W-x	R/W-x	U-0	R/W-x	R/W-x	R/W-x	R/W-x
MDCHODIS	MDCHPOL	MDCHSYNC	—	MDCH3(1)	MDCH2(1)	MDCH1(1)	MDCH0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **MDCHODIS:** Modulator High Carrier Output Disable bit
1 = Output signal driving the peripheral output pin (selected by MDCH<3:0>) is disabled
0 = Output signal driving the peripheral output pin (selected by MDCH<3:0>) is enabled

bit 6 **MDCHPOL:** Modulator High Carrier Polarity Select bit
1 = Selected high carrier signal is inverted
0 = Selected high carrier signal is not inverted

bit 5 **MDCHSYNC:** Modulator High Carrier Synchronization Enable bit
1 = Modulator waits for a falling edge on the high time carrier signal before allowing a switch to the low time carrier
0 = Modulator output is not synchronized to the high time carrier signal(1)

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **MDCH<3:0>** Modulator Data High Carrier Selection bits(1)
1111-1001 = Reserved
1000 = CCP5 output (PWM Output mode only)
0111 = CCP4 output (PWM Output mode only)
0110 = CCP3 output (PWM Output mode only)
0101 = CCP2 output (PWM Output mode only)
0100 = ECCP1 output (PWM Output mode only)
0011 = Reference clock module signal
0010 = MDCIN2 port pin
0001 = MDCIN1 port pin
0000 = VSS

Note 1: Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

REGISTER 12-4: MDCARL: MODULATION LOW CARRIER CONTROL REGISTER

R/W-0	R/W-x	R/W-x	U-0	R/W-x	R/W-x	R/W-x	R/W-x
MDCLODIS	MDCLPOL	MDCLSYNC	—	MDCL3(1)	MDCL2(1)	MDCL1(1)	MDCL0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **MDCLODIS:** Modulator Low Carrier Output Disable bit
- 1 = Output signal driving the peripheral output pin (selected by MDCL<3:0> of the MDCARL register) is disabled
- 0 = Output signal driving the peripheral output pin (selected by MDCL<3:0> of the MDCARL register) is enabled

bit 6 **MDCLPOL:** Modulator Low Carrier Polarity Select bit
- 1 = Selected low carrier signal is inverted
- 0 = Selected low carrier signal is not inverted

bit 5 **MDCLSYNC:** Modulator Low Carrier Synchronization Enable bit
- 1 = Modulator waits for a falling edge on the low time carrier signal before allowing a switch to the high time carrier
- 0 = Modulator output is not synchronized to the low time carrier signal(1)

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **MDCL<3:0>** Modulator Data High Carrier Selection bits(1)
- 1111-1001 = Reserved
- 1000 = CCP5 output (PWM Output mode only)
- 0111 = CCP4 output (PWM Output mode only)
- 0110 = CCP3 output (PWM Output mode only)
- 0101 = CCP2 output (PWM Output mode only)
- 0100 = ECCP1 output (PWM Output mode only)
- 0011 = Reference clock module signal
- 0010 = MDCIN2 port pin
- 0001 = MDCIN1 port pin
- 0000 = Vss

Note 1: Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

TABLE 12-1: SUMMARY OF REGISTERS ASSOCIATED WITH DATA SIGNAL MODULATOR MODE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MDCARH	MDCHODIS	MDCHPOL	MDCHSYNC	—	MDCH3	MDCH2	MDCH1	MDCH0
MDCARL	MDCLODIS	MDCLPOL	MDCLSYNC	—	MDCL3	MDCL2	MDCL1	MDCL0
MDCON	MDEN	MDOE	MDSLR	MDOPOL	MDO	—	—	MDBIT
MDSRC	MDSODIS	—	—	—	MDSRC3	MDSRC2	MDSRC1	MDSRC0
PMD2	—	—	—	—	MODMD	ECANMD	CMP2MD	CMP1MD

Legend: — = unimplemented, read as '0'. Shaded cells are not used in the Data Signal Modulator mode.

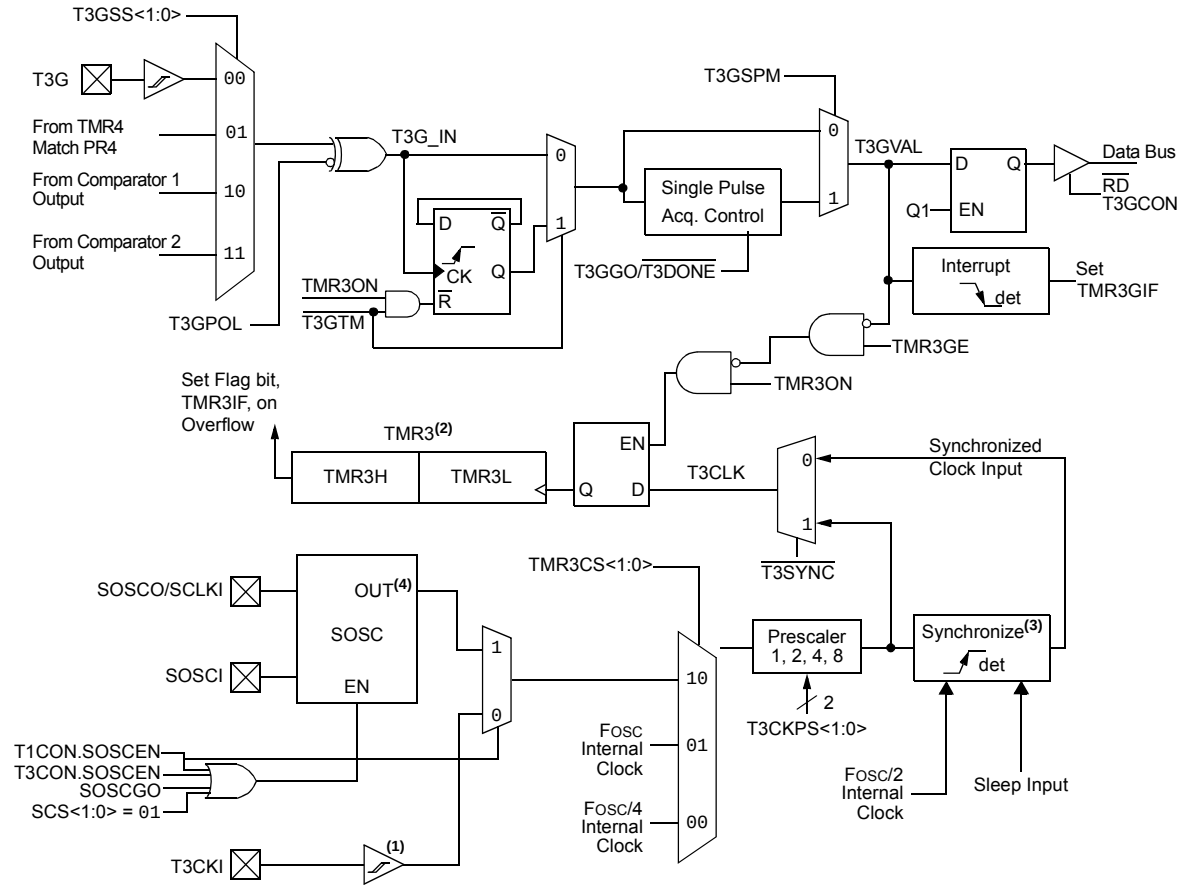
16.2 Timer3 Operation

Timer3 can operate in these modes:

- Timer
- Synchronous Counter
- Asynchronous Counter
- Timer with Gated Control

The operating mode is determined by the clock select bits, TMR3CSx (T3CON<7:6>). When the TMR3CSx bits are cleared (= 00), Timer3 increments on every internal instruction cycle (FOSC/4). When TMR3CSx = 01, the Timer3 clock source is the system clock (FOSC), and when it is '10', Timer3 works as a counter from the external clock from the T3CKI pin (on the rising edge after the first falling edge) or the SOSC oscillator.

FIGURE 16-1: TIMER3 BLOCK DIAGRAM



Note 1: ST Buffer is high-speed type when using T3CKI.
2: Timer3 registers increment on rising edge.
3: Synchronization does not operate while in Sleep.
4: The output of SOSC is determined by the SOSCSEL<1:0> Configuration bits.

REGISTER 21-4: SSPCON1: MSSP CONTROL REGISTER 1 (I²C™ MODE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN(1)	CKP	SSPM3(2)	SSPM2(2)	SSPM1(2)	SSPM0(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **WCOL:** Write Collision Detect bit

In Master Transmit mode:
1 = A write to the SSPBUF register was attempted while the I²C conditions were not valid for a transmission to be started (must be cleared in software)
0 = No collision

In Slave Transmit mode:
1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

In Receive mode (Master or Slave modes):
This is a "don't care" bit.

bit 6 **SSPOV:** Receive Overflow Indicator bit

In Receive mode:
1 = A byte is received while the SSPBUF register is still holding the previous byte (must be cleared in software)
0 = No overflow

In Transmit mode:
This is a "don't care" bit in Transmit mode.

bit 5 **SSPEN:** Master Synchronous Serial Port Enable bit(1)
1 = Enables the serial port and configures the SDA and SCL pins as the serial port pins
0 = Disables serial port and configures these pins as I/O port pins

bit 4 **CKP:** SCK Release Control bit

In Slave mode:
1 = Releases clock
0 = Holds clock low (clock stretch), used to ensure data setup time

In Master mode:
Unused in this mode.

bit 3-0 **SSPM<3:0>:** Master Synchronous Serial Port Mode Select bits(2)
1111 = I²C Slave mode, 10-bit address with Start and Stop bit interrupts enabled
1110 = I²C Slave mode, 7-bit address with Start and Stop bit interrupts enabled
1011 = I²C Firmware Controlled Master mode (slave Idle)
1001 = Load SSPMSK register at SSPADD SFR address(3,4)
1000 = I²C Master mode, clock = FOSC/(4 * (SSPADD + 1))
0111 = I²C Slave mode, 10-bit address
0110 = I²C Slave mode, 7-bit address

Note 1: When enabled, the SDA and SCL pins must be configured as inputs.
2: Bit combinations not specifically listed here are either reserved or implemented in SPI mode only.
3: When SSPM<3:0> = 1001, any reads or writes to the SSPADD SFR address actually access the SSPMSK register.
4: This mode is only available when 7-Bit Address Masking mode is selected (MSSPMSK Configuration bit is '1').

21.4.6.1 I²C™ Master Mode Operation

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or with a Repeated Start condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmitter mode, serial data is output through SDA while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/Write (R/$\overline{W}$) bit. In this case, the R/$\overline{W}$ bit will be logic '0'. Serial data is transmitted, 8 bits at a time. After each byte is transmitted, an Acknowledge bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/$\overline{W}$ bit. In this case, the R/$\overline{W}$ bit will be logic '1'. Thus, the first byte transmitted is a 7-bit slave address, followed by a '1' to indicate the receive bit. Serial data is received via SDA, while SCL outputs the serial clock. Serial data is received, 8 bits at a time. After each byte is received, an Acknowledge bit is transmitted. Start and Stop conditions indicate the beginning and end of transmission.

The Baud Rate Generator, used for the SPI mode operation, is used to set the SCL clock frequency for either 100 kHz, 400 kHz or 1 MHz I²C operation. See **Section 21.4.7 "Baud Rate"** for more details.

A typical transmit sequence would go as follows:

1. The user generates a Start condition by setting the Start Enable bit, SEN (SSPCON2<0>).
2. SSPIF is set. The MSSP module will wait the required start time before any other operation takes place.
3. The user loads the SSPBUF with the slave address to transmit.
4. Address is shifted out the SDA pin until all 8 bits are transmitted.
5. The MSSP module shifts in the ACK bit from the slave device and writes its value into the SSPCON2 register (SSPCON2<6>).
6. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPIF bit.
7. The user loads the SSPBUF with eight bits of data.
8. Data is shifted out the SDA pin until all 8 bits are transmitted.
9. The MSSP module shifts in the ACK bit from the slave device and writes its value into the SSPCON2 register (SSPCON2<6>).
10. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPIF bit.
11. The user generates a Stop condition by setting the Stop Enable bit, PEN (SSPCON2<2>).
12. Interrupt is generated once the Stop condition is complete.

22.3 EUSARTx Asynchronous Mode

The Asynchronous mode of operation is selected by clearing the SYNC bit (TXSTAx<4>). In this mode, the EUSARTx uses standard Non-Return-to-Zero (NRZ) format (one Start bit, eight or nine data bits and one Stop bit). The most common data format is 8 bits. An on-chip, dedicated 8-bit/16-bit Baud Rate Generator can be used to derive standard baud rate frequencies from the oscillator.

The EUSARTx transmits and receives the LSb first. The EUSARTx's transmitter and receiver are functionally independent but use the same data format and baud rate. The Baud Rate Generator produces a clock, either x16 or x64 of the bit shift rate, depending on the BRGH and BRG16 bits (TXSTAx<2> and BAUDCONx<3>). Parity is not supported by the hardware but can be implemented in software and stored as the 9th data bit.

When operating in Asynchronous mode, the EUSARTx module consists of the following important elements:

- Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver
- Auto-Wake-up on Sync Break Character
- 12-Bit Break Character Transmit
- Auto-Baud Rate Detection

22.3.1 EUSARTx ASYNCHRONOUS TRANSMITTER

The EUSARTx transmitter block diagram is shown in Figure 22-3. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The Shift register obtains its data from the Read/Write Transmit Buffer register, TXREGx. The TXREGx register is loaded with data in software. The TSR register is not loaded until the Stop bit has been transmitted from the previous load. As soon as the Stop bit is transmitted, the TSR is loaded with new data from the TXREGx register (if available).

Once the TXREGx register transfers the data to the TSR register (occurs in one TCY), the TXREGx register is empty and the TXxIF flag bit is set. This interrupt can be enabled or disabled by setting or clearing the interrupt enable bit, TXxIE. TXxIF will be set regardless of the state of TXxIE; it cannot be cleared in software. TXxIF is also not cleared immediately upon loading TXREGx, but becomes valid in the second instruction cycle following the load instruction. Polling TXxIF immediately following a load of TXREGx will return invalid results.

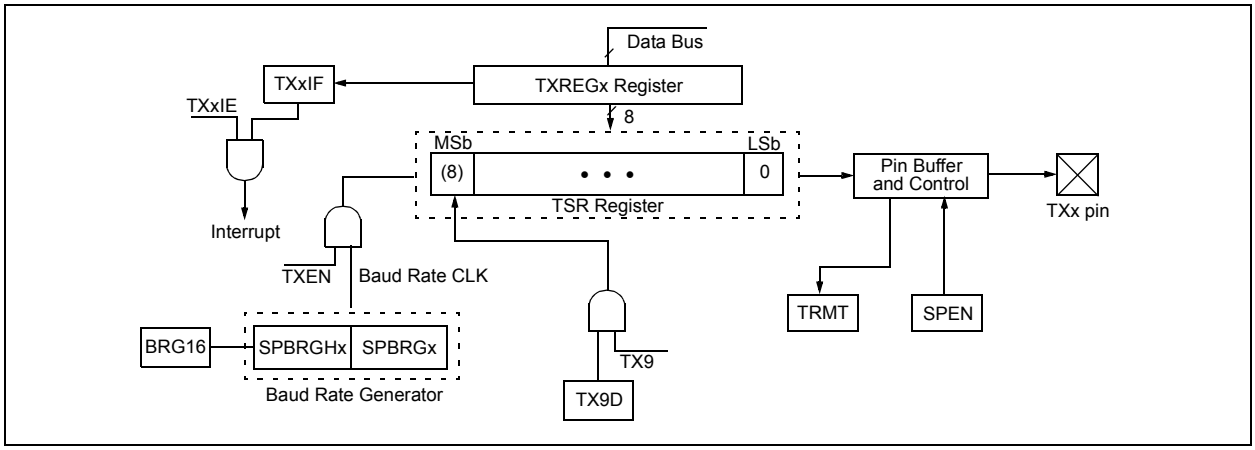
While TXxIF indicates the status of the TXREGx register; another bit, TRMT (TXSTAx<1>), shows the status of the TSR register. TRMT is a read-only bit which is set when the TSR register is empty. No interrupt logic is tied to this bit so the user has to poll this bit in order to determine if the TSR register is empty.

Note 1:	The TSR register is not mapped in data memory, so it is not available to the user.
2:	Flag bit, TXxIF, is set when enable bit, TXEN, is set.

To set up an Asynchronous Transmission:

1. Initialize the SPBRGHx:SPBRGx registers for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
2. Enable the asynchronous serial port by clearing bit, SYNC, and setting bit, SPEN.
3. If interrupts are desired, set enable bit, TXxIE.
4. If 9-bit transmission is desired, set transmit bit, TX9. Can be used as address/data bit.
5. Enable the transmission by setting bit, TXEN, which will also set bit, TXxIF.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
7. Load data to the TXREGx register (starts transmission).
8. If using interrupts, ensure that the GIE and PEIE bits (INTCON<7:6>) are set.

FIGURE 22-3: EUSARTx TRANSMIT BLOCK DIAGRAM



REGISTER 24-2: CMSTAT: COMPARATOR STATUS REGISTER

R-x	R-x	U-0	U-0	U-0	U-0	U-0	U-0
CMP2OUT	CMP1OUT	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **CMP2OUT:CMP1OUT:** Comparator x Status bits

If CPOL (CMxCON<5>)= 0 (non-inverted polarity):

1 = Comparator x's VIN+ > VIN-

0 = Comparator x's VIN+ < VIN-

If CPOL = 1 (inverted polarity):

1 = Comparator x's VIN+ < VIN-

0 = Comparator x's VIN+ > VIN-

bit 4-0 **Unimplemented:** Read as '0'

26.6 Operation During Sleep

When enabled, the HLVD circuitry continues to operate during Sleep. If the device voltage crosses the trip point, the HLVDIF bit will be set and the device will wake-up from Sleep. Device execution will continue from the interrupt vector address if interrupts have been globally enabled.

26.7 Effects of a Reset

A device Reset forces all registers to their Reset state. This forces the HLVD module to be turned off.

TABLE 26-1: REGISTERS ASSOCIATED WITH HIGH/LOW-VOLTAGE DETECT MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLVDCON	VDIRMAG	BGVST	IRVST	HLVDEN	HLVDL3	HLVDL2	HLVDL1	HLVDL0
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
PIR2	OSCFIF	—	—	—	BCLIF	HLVDIF	TMR3IF	TMR3GIF
PIE2	OSCFIE	—	—	—	BCLIE	HLVDIE	TMR3IE	TMR3GIE
IPR2	OSCFIP	—	—	—	BCLIP	HLVDIP	TMR3IP	TMR3GIP
TRISA	TRISA7(1)	TRISA6(1)	TRISA5	—	TRISA3	TRISA2	TRISA1	TRISA0

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the HLVD module.

Note 1: PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

27.2 CAN Module Registers

Note:	Not all CAN registers are available in the Access Bank.

There are many control and data registers associated with the CAN module. For convenience, their descriptions have been grouped into the following sections:

- Control and Status Registers
- Dedicated Transmit Buffer Registers
- Dedicated Receive Buffer Registers
- Programmable TX/RX and Auto RTR Buffers
- Baud Rate Control Registers
- I/O Control Register
- Interrupt Status and Control Registers

Detailed descriptions of each register and their usage are described in the following sections.

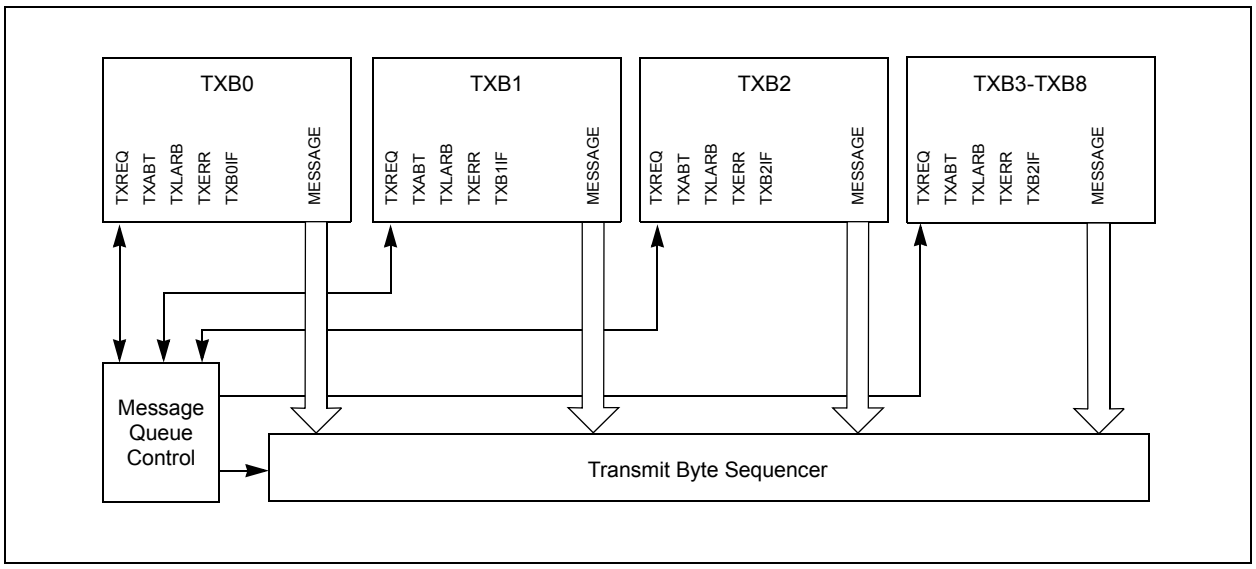
27.2.1 CAN CONTROL AND STATUS REGISTERS

The registers described in this section control the overall operation of the CAN module and show its operational status.

27.6.3 TRANSMIT PRIORITY

Transmit priority is a prioritization within the PIC18F66K80 family devices of the pending transmittable messages. This is independent from, and not related to, any prioritization implicit in the message arbitration scheme built into the CAN protocol. Prior to sending the Start-of-Frame (SOF), the priority of all buffers that are queued for transmission is compared. The transmit buffer with the highest priority will be sent first. If two buffers have the same priority setting, the buffer with the highest buffer number will be sent first. There are four levels of transmit priority. If the TXP bits for a particular message buffer are set to '11', that buffer has the highest possible priority. If the TXP bits for a particular message buffer are set to '00', that buffer has the lowest possible priority.

FIGURE 27-2: TRANSMIT BUFFERS



REGISTER 28-11: CONFIG7L: CONFIGURATION REGISTER 7 LOW (BYTE ADDRESS 30000Ch)

U-0	U-0	U-0	U-0	R/C-1	R/C-1	R/C-1	R/C-1
—	—	—	—	EBTR3	EBTR2	EBTR1	EBTR0
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **EBTR3:** Table Read Protection bit
1 = Block 3 is not protected from table reads executed in other blocks(1)
0 = Block 3 is protected from table reads executed in other blocks(1)

bit 2 **EBTR2**: Table Read Protection bit
1 = Block 2 is not protected from table reads executed in other blocks(1)
0 = Block 2 is protected from table reads executed in other blocks(1)

bit 1 **EBTR1:** Table Read Protection bit
1 = Block 1 is not protected from table reads executed in other blocks(1)
0 = Block 1 is protected from table reads executed in other blocks(1)

bit 0 **EBTR0:** Table Read Protection bit
1 = Block 0 is not protected from table reads executed in other blocks(1)
0 = Block 0 is protected from table reads executed in other blocks(1)

Note 1: For the memory size of the blocks, see Figure 28-6.

TABLE 29-2: PIC18F66K80 FAMILY INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	16-Bit Instruction Word		Status Affected	Notes
			MSb	LSb		
BYTE-ORIENTED OPERATIONS						
ADDWF f, d, a	Add WREG and f	1	0010 01da	ffff ffff	C, DC, Z, OV, N	1, 2
ADDWFC f, d, a	Add WREG and Carry bit to f	1	0010 00da	ffff ffff	C, DC, Z, OV, N	1, 2
ANDWF f, d, a	AND WREG with f	1	0001 01da	ffff ffff	Z, N	1,2
CLRF f, a	Clear f	1	0110 101a	ffff ffff	Z	2
COMF f, d, a	Complement f	1	0001 11da	ffff ffff	Z, N	1, 2
CPFSEQ f, a	Compare f with WREG, Skip =	1 (2 or 3)	0110 001a	ffff ffff	None	4
CPFSGT f, a	Compare f with WREG, Skip >	1 (2 or 3)	0110 010a	ffff ffff	None	4
CPFSLT f, a	Compare f with WREG, Skip <	1 (2 or 3)	0110 000a	ffff ffff	None	1, 2
DECF f, d, a	Decrement f	1	0000 01da	ffff ffff	C, DC, Z, OV, N	1, 2, 3, 4
DECFSZ f, d, a	Decrement f, Skip if 0	1 (2 or 3)	0010 11da	ffff ffff	None	1, 2, 3, 4
DCFSNZ f, d, a	Decrement f, Skip if Not 0	1 (2 or 3)	0100 11da	ffff ffff	None	1, 2
INCF f, d, a	Increment f	1	0010 10da	ffff ffff	C, DC, Z, OV, N	1, 2, 3, 4
INCFSZ f, d, a	Increment f, Skip if 0	1 (2 or 3)	0011 11da	ffff ffff	None	4
INFSNZ f, d, a	Increment f, Skip if Not 0	1 (2 or 3)	0100 10da	ffff ffff	None	1, 2
IORWF f, d, a	Inclusive OR WREG with f	1	0001 00da	ffff ffff	Z, N	1, 2
MOVF f, d, a	Move f	1	0101 00da	ffff ffff	Z, N	1
MOVFF f_s, f_d	Move f_s (source) to 1st word f_d (destination) 2nd word	2	1100 ffff 1111 ffff	ffff ffff ffff ffff	None	
MOVWF f, a	Move WREG to f	1	0110 111a	ffff ffff	None	
MULWF f, a	Multiply WREG with f	1	0000 001a	ffff ffff	None	1, 2
NEGF f, a	Negate f	1	0110 110a	ffff ffff	C, DC, Z, OV, N	
RLCF f, d, a	Rotate Left f through Carry	1	0011 01da	ffff ffff	C, Z, N	1, 2
RLNCF f, d, a	Rotate Left f (No Carry)	1	0100 01da	ffff ffff	Z, N	
RRCF f, d, a	Rotate Right f through Carry	1	0011 00da	ffff ffff	C, Z, N	
RRNCF f, d, a	Rotate Right f (No Carry)	1	0100 00da	ffff ffff	Z, N	
SETF f, a	Set f	1	0110 100a	ffff ffff	None	1, 2
SUBFWB f, d, a	Subtract f from WREG with Borrow	1	0101 01da	ffff ffff	C, DC, Z, OV, N	
SUBWF f, d, a	Subtract WREG from f	1	0101 11da	ffff ffff	C, DC, Z, OV, N	1, 2
SUBWFB f, d, a	Subtract WREG from f with Borrow	1	0101 10da	ffff ffff	C, DC, Z, OV, N	
SWAPF f, d, a	Swap Nibbles in f	1	0011 10da	ffff ffff	None	4
TSTFSZ f, a	Test f, Skip if 0	1 (2 or 3)	0110 011a	ffff ffff	None	1, 2
XORWF f, d, a	Exclusive OR WREG with f	1	0001 10da	ffff ffff	Z, N	

Note 1: When a PORT register is modified as a function of itself (e.g., `MOVF PORTB, 1, 0`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as an input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned.

3: If the Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

4: Some instructions are two-word instructions. The second word of these instructions will be executed as a NOP unless the first word of the instruction retrieves the information embedded in these 16 bits. This ensures that all program memory locations have a valid instruction.

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