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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	ECANbus, I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.6K × 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf46k80-i-pt

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	Pin N	umber					
Pin Name	QFN	SSOP/ SPDIP /SOIC	Pin Type	Buffer Type	Description		
					PORTA is a bidirectional I/O port.		
RA0/CVREF/AN0/ULPWU	27	2					
RA0			I/O	ST/ CMOS	General purpose I/O pin.		
CVREF			0	Analog	Comparator reference voltage output.		
AN0			I	Analog	Analog Input 0.		
ULPWU			I.	Analog	Ultra Low-Power Wake-up input.		
RA1/AN1	28	3					
RA1			I/O	ST/ CMOS	Digital I/O.		
AN1			I.	Analog	Analog Input 1.		
RA2/VREF-/AN2	1	4					
RA2			I/O	ST/ CMOS	Digital I/O.		
VREF-			I	Analog	A/D reference voltage (low) input.		
AN2			Ι	Analog	Analog Input 2.		
RA3/VREF+/AN3	2	5					
RA3			I/O	ST/ CMOS	Digital I/O.		
VREF+			Ι	Analog	A/D reference voltage (high) input.		
AN3			I	Analog	Analog Input 3.		
RA5/AN4/C2INB/HLVDIN/ T1CKI/SS/CTMUI	4	7					
RA5			I/O	ST/ CMOS	Digital I/O.		
AN4			I	Analog	Analog Input 4.		
C2INB			I	Analog	Comparator 2 Input B.		
HLVDIN			Ι	Analog	High/Low-Voltage Detect input.		
T1CKI			I	ST	Timer1 clock input.		
SS			I	ST	SPI slave select input.		
CTMUI					CTMU pulse generator charger for the C2INB.		
Legend: CMOS = CMOS	S comp	atible in	out or o	output	I^2C^{TM} = I^2C/SMB us input buffer		
ST = Schmi I = Input	itt Trigg	er input	with C	MOS lev	els Analog = Analog input O = Output		

TABLE 1-4:	PIC18F2XK80 I/O DESCRIPTIONS (CONTINUED)
------------	--

Ρ

= Power

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Pin Name	Pin Num	Pin Type	Buffer Type	Description			
Vss	8		Р				
Vss				Ground reference for logic and I/O pins.			
Vss	26		Р				
Vss				Ground reference for logic and I/O pins.			
Avss	42		Р				
Avss				Ground reference for analog modules.			
Vss	43		Р				
Vss				Ground reference for logic and I/O pins.			
Vss	56		Р				
Vss				Ground reference for logic and I/O pins.			
Avdd	9		Р				
Avdd				Positive supply for analog modules.			
VDD	10		Р				
Vdd				Positive supply for logic and I/O pins.			
Vdd	25		Р				
Vdd				Positive supply for logic and I/O pins.			
VDDCORE/VCAP	33		Р				
VDDCORE				External filter capacitor connection.			
VCAP				External filter capacitor connection.			
Avdd	40		Р				
Avdd				Positive supply for analog modules.			
Vdd	41		Р				
Vdd				Positive supply for logic and I/O pins.			
VDD	57		Р				
Vdd				Positive supply for logic and I/O pins.			
Legend: $I^2C^{TM} = I^2C/SI$ ST = Schmitt I = Input P = Power	MBus ir t Trigge	nput buff r input w	er /ith CMC	CMOS = CMOS compatible input or output Analog = Analog input O = Output			

TABLE 1-6:	PIC18F6XK80 PINOUT I/O DESCRIPTIONS ((CONTINUED)
		/

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
ROON		ROSSLP	ROSEL ⁽¹⁾	RODIV3	RODIV2	RODIV1	RODIV0				
bit 7							bit 0				
Legend:	L.:4		L 14	ll llaimealan							
R = Readable		vv = vvritable	DIL	0 = 0	nented bit, rea	ted bit, read as '0'					
-n = value at	PUR	I = BILIS SEL		0 = Bit is cie	ared	x = Bit is unki	IOWN				
bit 7	ROON: Refe	rence Oscillato	r Output Enab	le bit							
	1 = Referenc 0 = Referenc	e oscillator out e oscillator out	put is available put is disabled	e on REFO pin							
bit 6	Unimplemen	ted: Read as '	0'								
bit 5	ROSSLP: Re	eference Oscilla	ator Output Sto	op in Sleep bit							
	1 = Referenc 0 = Referenc	e oscillator con e oscillator is d	tinues to run ii isabled in Slee	n Sleep ep							
bit 4	ROSEL: Refe	erence Oscillate	or Source Sele	ect bit ⁽¹⁾							
	1 = Primary c 0 = System c	scillator (EC or lock is used as	HS) is used a the base cloc	as the base clo k; base clock r	ck eflects any clo	ck switching of	the device				
bit 3-0	RODIV<3:0>	: Reference Os	cillator Divisor	r Select bits							
	1111 = Base 1101 = Base 1101 = Base 1001 = Base 1010 = Base 1001 = Base 1000 = Base 0111 = Base 0101 = Base 0101 = Base 0011 = Base 0011 = Base 0011 = Base	clock value div clock value div	vided by 32,76 vided by 16,38 vided by 8,192 vided by 4,096 vided by 2,048 vided by 1,024 vided by 512 vided by 512 vided by 128 vided by 4 vided by 8 vided by 8 vided by 4 vided by 2	8 4							

REGISTER 3-4: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

Note 1: For ROSEL (REFOCON<4>), the primary oscillator is available only when configured as the default via the FOSCx settings. This is regardless of whether the device is in Sleep mode.

TABLE 4-4:EXIT DELAY ON WAKE-UP BY RESET FROM SLEEP MODE OR ANY IDLE MODE
(BY CLOCK SOURCES)

Power-Managed Mode	Clock Source ⁽⁵⁾	Exit Delay	Clock Ready Status Bits	
	LP, XT, HS			
PRI IDI E mode	HSPLL		OSTS	
	EC, RC	тоор(1)		
PRI_IDLE mode	HF-INTOSC ⁽²⁾		HFIOFS	
	MF-INTOSC ⁽²⁾		MFIOFS	
	LF-INTOSC		None	
SEC_IDLE mode	SOSC	TCSD ⁽¹⁾	SOSCRUN	
	HF-INTOSC ⁽²⁾		HFIOFS	
SEC_IDLE mode RC_IDLE mode	MF-INTOSC ⁽²⁾	TCSD ⁽¹⁾	MFIOFS	
	LF-INTOSC		None	
	LP, XT, HS	Tost ⁽³⁾		
Sleep mode	HSPLL	Tost + t _{rc} (3)	OSTS	
	EC, RC	TCSD ⁽¹⁾		
	HF-INTOSC ⁽²⁾		HFIOFS	
	MF-INTOSC ⁽²⁾	TIOBST ⁽⁴⁾	MFIOFS	
	LF-INTOSC		None	

Note 1: TCSD (Parameter 38, Table 31-11) is a required delay when waking from Sleep and all Idle modes, and runs concurrently with any other required delays (see **Section 4.4 "Idle Modes"**).

2: Includes postscaler derived frequencies. On Reset, INTOSC defaults to HF-INTOSC at 8 MHz.

3: TOST is the Oscillator Start-up Timer (Parameter 32, Table 31-11). TRC is the PLL Lock-out Timer (Parameter F12, Table 31-7); it is also designated as TPLL.

4: Execution continues during TIOBST (Parameter 39, Table 31-11), the INTOSC stabilization period.

5: The clock source is dependent upon the settings of the SCSx (OSCCON<1:0>), IRCFx (OSCCON<6:4>) and FOSCx (CONFIG1H<3:0>) bits.

FIGURE 7-2: TABLE WRITE OPERATION



7.2 Control Registers

Several control registers are used in conjunction with the ${\tt TBLRD}$ and ${\tt TBLWT}$ instructions. These include the:

- EECON1 register
- EECON2 register
- TABLAT register
- TBLPTR registers

7.2.1 EECON1 AND EECON2 REGISTERS

The EECON1 register (Register 7-1) is the control register for memory accesses. The EECON2 register, not a physical register, is used exclusively in the memory write and erase sequences. Reading EECON2 will read all '0's.

The EEPGD control bit determines if the access is a program or data EEPROM memory access. When clear, any subsequent operations operate on the data EEPROM memory. When set, any subsequent operations operate on the program memory.

The CFGS control bit determines if the access is to the Configuration registers or to program memory/data EEPROM memory. When set, subsequent operations operate on Configuration registers regardless of EEPGD (see **Section 28.0 "Special Features of the CPU**"). When clear, memory selection access is determined by EEPGD. The FREE bit, when set, allows a program memory erase operation. When FREE is set, the erase operation is initiated on the next WR command. When FREE is clear, only writes are enabled.

The WREN bit, when set, allows a write operation. On power-up, the WREN bit is clear. The WRERR bit is set in hardware when the WR bit is set and cleared when the internal programming timer expires and the write operation is complete.

Note:	During normal operation, the WRERR is									
	read as '1'. This can indicate that a write									
	operation was prematurely terminated by									
	a Reset, or a write operation was									
	attempted improperly.									

The WR control bit initiates write operations. The bit cannot be cleared, only set, in software. It is cleared in hardware at the completion of the write operation.

Note: The EEIF interrupt flag bit (PIR4<6>) is set when the write is complete. It must be cleared in software.

REGISTER 10-5: PIR2: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 2

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
OSCFIF	—	—	—	BCLIF	HLVDIF	TMR3IF	TMR3GIF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7	 OSCFIF: Oscillator Fail Interrupt Flag bit 1 = Device oscillator failed, clock input has changed to INTOSC (bit must be cleared in software) 0 = Device clock is operating
bit 6-4	Unimplemented: Read as '0'
bit 3	BCLIF: Bus Collision Interrupt Flag bit
	1 = A bus collision occurred (bit must be cleared in software)0 = No bus collision occurred
bit 2	HLVDIF: High/Low-Voltage Detect Interrupt Flag bit
	 1 = A low-voltage condition occurred (bit must be cleared in software) 0 = The device voltage is above the regulator's low-voltage trip point
bit 1	TMR3IF: TMR3 Overflow Interrupt Flag bit
	1 = TMR3 register overflowed (bit must be cleared in software)0 = TMR3 register did not overflow
bit 0	TMR3GIF: TMR3 Gate Interrupt Flag bit
	 1 = Timer gate interrupt occurred (bit must be cleared in software) 0 = No timer gate interrupt occurred

14.0 TIMER1 MODULE

The Timer1 timer/counter module incorporates these features:

- · Software selectable operation as a 16-bit timer or counter
- Readable and writable 8-bit registers (TMR1H and TMR1L)
- · Selectable clock source (internal or external) with device clock or SOSC oscillator internal options
- Interrupt-on-overflow
- Reset on ECCP Special Event Trigger
- · Timer with gated control

Figure 14-1 displays a simplified block diagram of the Timer1 module.

The module derives its clocking source from either the secondary oscillator or from an external digital source. If using the secondary oscillator, there are the additional options for low-power, high-power and external digital clock source.

Timer1 is controlled through the T1CON Control register (Register 14-1). It also contains the Timer1 Oscillator Enable bit (SOSCEN). Timer1 can be enabled or disabled by setting or clearing control bit, TMR1ON (T1CON<0>).

The Fosc clock source should not be used with the ECCP capture/compare features. If the timer will be used with the capture or compare features, always select one of the other timer clocking options.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	SOSCEN	T1SYNC	RD16	TMR10N
bit 7							bit 0

REGISTER 14-1: T1CON: TIMER1 CONTROL REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6	TMR1CS<1:0>: Timer1 Clock Source Select bits
	10 = Timer1 clock source is either from pin or oscillator, depending on the SOSCEN bit:
	SOSCEN = 0:
	External clock is from the T1CKI pin (on the rising edge).
	<u>SOSCEN = 1:</u> Depending on the SOSCSELx Configuration bit, the clock source is either a crystal oscillator on SOSCI/SOSCO or an internal digital clock from the SCLKI pin. 01 = Timer1 clock source is the system clock (Fosc) ⁽¹⁾ 00 = Timer1 clock source is the instruction clock (Fosc/4)
bit 5-4	T1CKPS<1:0>: Timer1 Input Clock Prescale Select bits
	11 = 1:8 Prescale value 10 = 1:4 Prescale value 01 = 1:2 Prescale value 00 = 1:1 Prescale value
bit 3	SOSCEN: SOSC Oscillator Enable bit
	1 = SOSC is enabled and available for Timer1
	0 = SOSC is disabled for Timer1 The oscillator inverter and feedback resistor are turned off to eliminate power drain.
bit 2	T1SYNC: Timer1 External Clock Input Synchronization Select bit
	<u>TMR1CS<1:0> = 10:</u>
	1 = Do not synchronize external clock input
	0 = Synchronizes external clock input
	$\frac{\text{TMR1CS}(1:0) = 0x}{\text{Tmran}}$
	This bit is ignored. Time T uses the internal clock when TMRTCS<1:0> = 1x.
Note 1	The Fosc clock source should not be selected if the timer will be used with the FCCP canture/compare

ck source should not be selected if the timer will be used with the ECCP capture/compare features.



14.8.2 TIMER1 GATE SOURCE SELECTION

The Timer1 gate source can be selected from one of four sources. Source selection is controlled by the T1GSSx (T1GCON<1:0>) bits (see Table 14-4).

TABLE 14-4: TIN	IER1 GA	TE SO	URCES
-----------------	---------	-------	-------

T1GSS<1:0>	Timer1 Gate Source
00	Timer1 Gate Pin
01	TMR2 to Match PR2 (TMR2 increments to match PR2)
10	Comparator 1 Output (comparator logic high output)
11	Comparator 2 Output (comparator logic high output)

The polarity for each available source is also selectable, controlled by the T1GPOL bit (T1GCON<6>).

14.8.2.1 T1G Pin Gate Operation

The T1G pin is one source for Timer1 gate control. It can be used to supply an external source to the Timer1 gate circuitry.

14.8.2.2 Timer2 Match Gate Operation

The TMR2 register will increment until it matches the value in the PR2 register. On the very next increment cycle, TMR2 will be reset to 00h. When this Reset occurs, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 gate circuitry. The pulse will remain high for one instruction cycle and will return back to a low state until the next match.

Depending on T1GPOL, Timer1 increments differently when TMR2 matches PR2. When T1GPOL = 1, Timer1 increments for a single instruction cycle following a TMR2 match with PR2. When T1GPOL = 0, Timer1 increments continuously except for the cycle following the match when the gate signal goes from low-to-high.

14.8.2.3 Comparator 1 Output Gate Operation

The output of Comparator 1 can be internally supplied to the Timer1 gate circuitry. After setting up Comparator 1 with the CM1CON register, Timer1 will increment depending on the transitions of the CMP1OUT (CMSTAT<6>) bit.

14.8.2.4 Comparator 2 Output Gate Operation

The output of Comparator 2 can be internally supplied to the Timer1 gate circuitry. After setting up Comparator 2 with the CM2CON register, Timer1 will increment depending on the transitions of the CMP2OUT (CMSTAT<7>) bit.

16.5 Timer3 Gates

Timer3 can be configured to count freely or the count can be enabled and disabled using the Timer3 gate circuitry. This is also referred to as the Timer3 gate count enable.

The Timer3 gate can also be driven by multiple selectable sources.

16.5.1 TIMER3 GATE COUNT ENABLE

The Timer3 Gate Enable mode is enabled by setting the TMR3GE bit (TxGCON<7>). The polarity of the Timer3 Gate Enable mode is configured using the T3GPOL bit (T3GCON<6>).

When Timer3 Gate Enable mode is enabled, Timer3 will increment on the rising edge of the Timer3 clock source. When Timer3 Gate Enable mode is disabled, no incrementing will occur and Timer3 will hold the current count. See Figure 16-2 for timing details.

TABLE 16-1: TIMER3 GATE ENABLE SELECTIONS

T3CLK ^(†)	T3GPOL (T3GCON<6>)	T3G Pin	Timer3 Operation	
\uparrow	0	0	Counts	
\uparrow	0	1	Holds Count	
\uparrow	1	0	Holds Count	
\uparrow	1	1	Counts	

† The clock on which TMR3 is running. For more information, see T3CLK in Figure 16-1.



FIGURE 16-2: TIMER3 GATE COUNT ENABLE MODE

18.9 Measuring Temperature with the CTMU Module

The CTMU, along with an internal diode, can be used to measure the temperature. The A/D can be connected to the internal diode and the CTMU module can

source the current to the diode. The A/D reading will reflect the temperature. With the increase, the A/D readings will go low. This can be used for low-cost temperature measurement applications.

EXAMPLE 18-6: ROUTINE FOR TEMPERATURE MEASUREMENT USING INTERNAL DIODE

<pre>// Initialize CTMU CTMUICON = 0x03; CTMUCONHbits.CTMUEN = 1; CTMUCONLbits.EDG1STAT = 1;</pre>	
// Initialize ADC	
$ADCON0 = 0 \times E5;$ $ADCON1 = 0 \times 00;$	// Enable ADC and connect to Internal diode
$ADCON2 = 0 \times BE;$	//Right Justified
ADCON0bits.GO = 1; while(ADCON0bits.G0);	// Start conversion
Temp = ADRES;	// Read ADC results (inversely proportional to temperature)

Note: The temperature diode is not calibrated or standardized; the user must calibrate the diode to their application.

19.1 CCP Module Configuration

Each Capture/Compare/PWM module is associated with a control register (generically, CCPxCON) and a data register (CCPRx). The data register, in turn, is comprised of two 8-bit registers: CCPRxL (low byte) and CCPRxH (high byte). All registers are both readable and writable.

19.1.1 CCP MODULES AND TIMER RESOURCES

The CCP modules utilize Timers, 1 through 4, varying with the selected mode. Various timers are available to the CCP modules in Capture, Compare or PWM modes, as shown in Table 19-1.

TABLE 19-1: CCP MODE – TIMER RESOURCE

CCP Mode	Timer Resource
Capture	Timor1 or Timor2
Compare	
PWM	Timer2 or Timer4

The assignment of a particular timer to a module is determined by the Timer to CCP enable bits in the CCPTMRS register (see Register 19-2). All of the modules may be active at once and may share the same timer resource if they are configured to operate in the same mode (Capture/Compare or PWM) at the same time.

The CCPTMRS register selects the timers for CCP modules, 2, 3, 4 and 5. The possible configurations are shown in Table 19-2.

TABLE 19-2: TIMER ASSIGNMENTS FOR CCP MODULES 2, 3, 4 AND 5

	CCPTMRS Register										
CCP2 CCP3						CCP4			CCP5		
C2TSEL	Capture/ Compare Mode	PWM Mode	C3TSEL	Capture/ Compare Mode	PWM Mode	C4TSEL	C4TSEL Capture/ Compare Mode PWM			Capture/ Compare Mode	PWM Mode
0	TMR1	TMR2	0	TMR1	TMR2	0	TMR1	TMR2	0 0	TMR1	TMR2
1	TMR3	TMR4	1	TMR3	TMR4	1	TMR3	TMR4	0 1	TMR3	TMR4

19.1.2 OPEN-DRAIN OUTPUT OPTION

When operating in Output mode (the Compare or PWM modes), the drivers for the CCPx pins can be optionally configured as open-drain outputs. This feature allows the voltage level on the pin to be pulled to a higher level through an external pull-up resistor and allows the output to communicate with external circuits without the need for additional level shifters.

The open-drain output option is controlled by the CCPxOD bits (ODCON<6:2>). Setting the appropriate bit configures the pin for the corresponding module for open-drain operation.

IGURE 21-5:	SPI N	IODE W	AVEFO	RM (SLA	VE MO	DE WITH	CKE =	0)			
 SS Opilonsi	(.										
80X (0X9°≈ 0	: : : :X		, 	·	·					· ·	: : :
- VAG P 03 - MAG - IIIIIII	· ·	: : :	((() () () () () () () () () () () () () (, , , ,	; ; ; , ,		(((; ; ; ;	2 2 3	, , ,	
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FIGURE 21-6: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)





Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSPIF	TMR1GIF	TMR2IF	TMR1IF
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSPIE	TMR1GIE	TMR2IE	TMR1IE
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSPIP	TMR1GIP	TMR2IP	TMR1IP
PIR3	—	—	RC2IF	TX2IF	CTMUIF	CCP2IF	CCP1IF	_
PIE3	—	—	RC2IE	TX2IE	CTMUIE	CCP2IE	CCP1IE	_
IPR3	—	—	RC2IP	TX2IP	CTMUIP	CCP2IP	CCP1IP	_
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
RCREG1	EUSART1 R	eceive Regist	er					
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
BAUDCON1	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN
SPBRGH1	EUSART1 B	aud Rate Ger	erator Regi	ster High By	⁄te			
SPBRG1	EUSART1 Ba	aud Rate Ger	erator Regi	ster Low By	te			
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
RCREG2	EUSART2 R	eceive Regist	er					
TXSTA2	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
BAUDCON2	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN
SPBRGH2	EUSART2 B	aud Rate Ger	nerator Regi	ster High By	/te			
SPBRG2	EUSART2 B	aud Rate Ger	erator Regi	ster Low By	te			
PMD0	CCP5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD	UART2MD	UART1MD	SSPMD
ODCON	SSPOD	CCP5OD	CCP4OD	CCP3OD	CCP2OD	CCP10D	U2OD	U10D
Legend: -=	unimplement	ed, read as '0	'. Shaded c	ells are not	used for syne	chronous ma	ster receptior	

TABLE 22-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION



25.2 Voltage Reference Accuracy/Error

The full range of voltage reference cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 25-1) keep CVREF from approaching the reference source rails. The voltage reference is derived from the reference source; therefore, the CVREF output changes with fluctuations in that source. The tested absolute accuracy of the voltage reference can be found in **Section 31.0 "Electrical Characteristics"**.

25.3 Operation During Sleep

When the device wakes up from Sleep through an interrupt or a Watchdog Timer time-out, the contents of the CVRCON register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

25.4 Effects of a Reset

A device Reset disables the voltage reference by clearing bit, CVREN (CVRCON<7>). This Reset also disconnects the reference from the RF5 pin by clearing bit, CVROE (CVRCON<6>).

25.5 Connection Considerations

The voltage reference module operates independently of the comparator module. The output of the reference generator may be connected to the RA0 pin if the CVROE bit is set. Enabling the voltage reference output onto RA0 when it is configured as a digital input will increase current consumption. Connecting RA0 as a digital output with CVRSS enabled will also increase current consumption.

The RA0 pin can be used as a simple D/A output with limited drive capability. Due to the limited current drive capability, a buffer must be used on the voltage reference output for external connections to VREF. Figure 25-2 shows an example buffering technique.

REGISTER 27-13: RXB0CON: RECEIVE BUFFER 0 CONTROL REGISTER (CONTINUED)

bit 2	Mode 0: PRODEEN: Descrive Buffer & Deuble Buffer Encode bit
	ABODBEN. Receive Bullet O Double-Bullet Enable bit
	\perp = No Receive Buffer 0 overflow to Receive Buffer 1
	Mode 1 2:
	FIL HIT<4:0 >: Filter Hit bit 2
	This bit combines with other bits to form filter acceptance bits<4:0>.
bit 1	Mode 0:
	JTOFF: Jump Table Offset bit (read-only copy of RXB0DBEN) ⁽²⁾
	1 = Allows jump table offset between 6 and 7
	0 = Allows jump table offset between 1 and 0
	<u>Mode 1, 2:</u>
	FILHIT<4:0>: Filter Hit bit 1
	This bit combines with other bits to form filter acceptance bits<4:0>.
bit 0	Mode 0:
	FILHITO: Filter Hit bit 0
	This bit indicates which acceptance filter enabled the message reception into Receive Buffer 0.
	1 = Acceptance Filter 1 (RXF1)
	0 = Acceptance Filter 0 (RXFU)
	Mode 1, 2:
	FILMI1<4:0>: FILMET MILDIE U This hit in combination with FILMIT<4:1> indicates which accentance filter enabled the message recention.
	into this receive buffer.
	01111 = Acceptance Filter 15 (RXF15)
	01110 = Acceptance Filter 14 (RXF14)
	00000 = Acceptance Filter 0 (RXF0)

- **Note 1:** This bit is set by the CAN module upon receiving a message and must be cleared by software after the buffer is read. As long as RXFUL is set, no new message will be loaded and the buffer will be considered full. After clearing the RXFUL flag, the PIR5 bit, RXB0IF, can be cleared. If RXB0IF is cleared, but RXFUL is not cleared, then RXB0IF is set again.
 - 2: This bit allows the same filter jump table for both RXB0CON and RXB1CON.

REGISTER 27-34: BnDLC: TX/RX BUFFER 'n' DATA LENGTH CODE REGISTERS IN RECEIVE MODE $[0 \le n \le 5, TXnEN (BSEL < n >) = 0]^{(1)}$

U-0	R-x	R-x	R-x	R-x	R-x	R-x	R-x
—	RXRTR	RB1	RB0	DLC3	DLC2	DLC1	DLC0
bit 7						-	bit 0
Legend:							
R = Readable I	bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
bit 7	Unimplemen	ted: Read as '	0'				
bit 6	RXRTR: Rece	eiver Remote T	ransmission	Request bit			
	1 = This is a r 0 = This is no	emote transmi t a remote tran	ssion request smission req	uest			
bit 5	RB1: Reserve	ed bit 1					
	Reserved by	CAN Spec and	read as '0'.				
bit 4	RB0: Reserve	ed bit 0					
	Reserved by	CAN Spec and	read as '0'.				
bit 3-0	DLC<3:0>: D	ata Length Coo	de bits				
	1111 = Rese	rved					
	1110 = Reser	rved					
	1101 = Rese	rved					
	1100 = Rese i	rved					
	1011 = Resei	rved					
	1010 = Resei	rved					
	1001 = Resei	Ved	-				
	1000 = Data	length = 8 byte	S				
	0111 - Data	engli – 7 byle ength – 6 byte	5				
	0110 = Data	length = 5 byte	5 C				
	0101 = Data	length = 4 byte	3 9				
	0011 = Data	length = 3 byte	s				
	0010 = Data	enath = 2 byte	S				
	0001 = Data	length = 1 byte					
	0000 = Data	length = 0 byte	S				

Note 1: These registers are available in Mode 1 and 2 only.

27.2.5 CAN MODULE I/O CONTROL REGISTER

This register controls the operation of the CAN module's I/O pins in relation to the rest of the microcontroller.

REGISTER 27-55: CIOCON: CAN I/O CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
TX2SRC	TX2EN	ENDRHI ⁽¹⁾	CANCAP	—	—	—	CLKSEL
bit 7							bit 0

Legend:									
R = Readable bit -n = Value at POR		W = Writable bit	U = Unimplemented bit,	U = Unimplemented bit, read as '0'					
		'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown					
bit 7	TX2SR0	: CANTX2 Pin Data Source	bit						
	1 = CAN 0 = CAN	1 = CANTX2 pin will output the CAN clock 0 = CANTX2 pin will output CANTX							
bit 6	TX2EN:	TX2EN: CANTX Pin Enable bit							
	1 = CAN 0 = CAN	1 = CANTX2 pin will output \overline{CANTX} or CAN clock as selected by the TX2SRC bit 0 = CANTX2 pin will have digital I/O function							
bit 5	ENDRH	ENDRHI: Enable Drive High bit ⁽¹⁾							
	1 = CAN 0 = CAN	 1 = CANTX pin will drive VDD when recessive 0 = CANTX pin will be tri-state when recessive 							
bit 4	CANCA	CANCAP: CAN Message Receive Capture Enable bit							
	1 = Ena 0 = Disa	 1 = Enable CAN capture; CAN message receive signal replaces input on RC2/CCP1 0 = Disable CAN capture; RC2/CCP1 input to CCP1 module 							
bit 3-1	Unimple	Unimplemented: Read as '0'							
bit 0	CLKSE	CLKSEL: CAN Clock Source Selection bit							
	1 = Use 0 = Use	the oscillator as the source of the PLL as the source of the	of the CAN system clock CAN system clock						
Note 1:	Always set th	is bit when using a differentia	I bus to avoid signal crosstalk	in CANTX from other nearby pir					

27.6.3 TRANSMIT PRIORITY

Transmit priority is a prioritization within the PIC18F66K80 family devices of the pending transmittable messages. This is independent from, and not related to, any prioritization implicit in the message arbitration scheme built into the CAN protocol. Prior to sending the Start-of-Frame (SOF), the priority of all buffers that are queued for transmission is compared. The transmit buffer with the highest priority will be sent first. If two buffers have the same priority setting, the buffer with the highest buffer number will be sent first. There are four levels of transmit priority. If the TXP bits for a particular message buffer are set to '11', that buffer has the highest possible priority. If the TXP bits for a particular message buffer are set to '00', that buffer has the lowest possible priority.





30.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit[™] 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows[®] programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit[™] 2 enables in-circuit debugging on most PIC[®] microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

30.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

30.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM[™] and dsPICDEM[™] demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ[®] security ICs, CAN, IrDA[®], PowerSmart battery management, SEEVAL[®] evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.