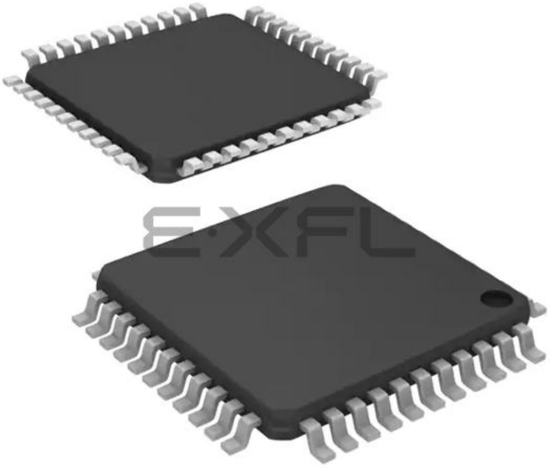
Microchip Technology - PIC18LF46K80T-I/PT Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	ECANbus, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf46k80t-i-pt

6.6.3 MAPPING THE ACCESS BANK IN INDEXED LITERAL OFFSET MODE

The use of Indexed Literal Offset Addressing mode effectively changes how the lower part of Access RAM (00h to 5Fh) is mapped. Rather than containing just the contents of the bottom part of Bank 0, this mode maps the contents from Bank 0 and a user-defined "window" that can be located anywhere in the data memory space.

The value of FSR2 establishes the lower boundary of the addresses mapped into the window, while the upper boundary is defined by FSR2 plus 95 (5Fh). Addresses in the Access RAM above 5Fh are mapped as previously described. (See **Section 6.3.2 "Access Bank"**.) An example of Access Bank remapping in this addressing mode is shown in Figure 6-10.

Remapping the Access Bank applies *only* to operations using the Indexed Literal Offset mode. Operations that use the BSR (Access RAM bit = `1`) will continue to use Direct Addressing as before. Any Indirect or Indexed Addressing operation that explicitly uses any of the indirect file operands (including FSR2) will continue to operate as standard Indirect Addressing. Any instruction that uses the Access Bank, but includes a register address of greater than 05Fh, will use Direct Addressing and the normal Access Bank map.

6.6.4 BSR IN INDEXED LITERAL OFFSET MODE

Although the Access Bank is remapped when the extended instruction set is enabled, the operation of the BSR remains unchanged. Direct Addressing, using the BSR to select the data memory bank, operates in the same manner as previously described.

FIGURE 6-10: REMAPPING THE ACCESS BANK WITH INDEXED LITERAL OFFSET ADDRESSING

Example Situation:

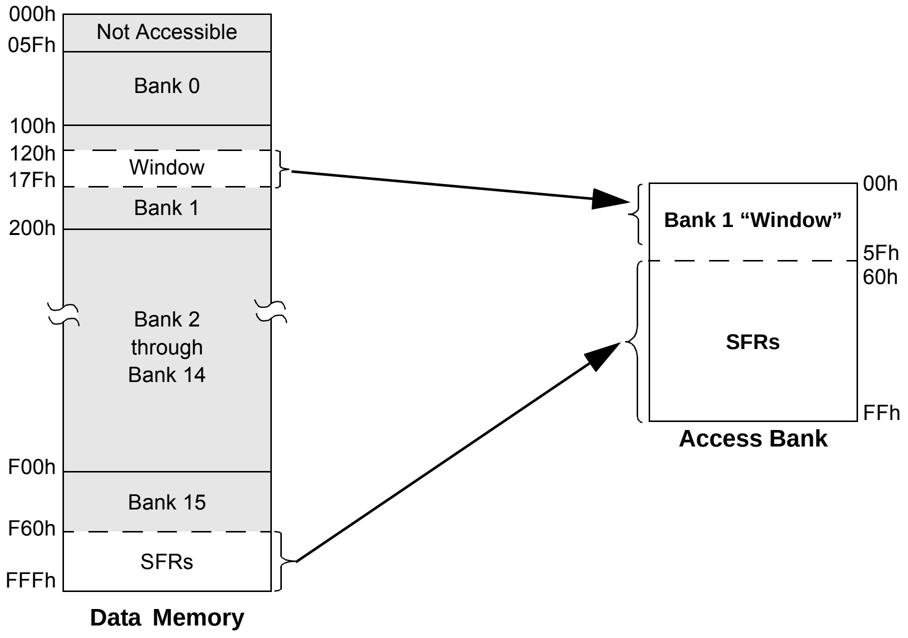
`ADDWF f, d, a`

FSR2H:FSR2L = 120h

Locations in the region from the FSR2 Pointer (120h) to the pointer plus 05Fh (17Fh) are mapped to the bottom of the Access RAM (000h-05Fh).

Special Function Registers at F60h through FFFh are mapped to 60h through FFh, as usual.

Bank 0 addresses below 5Fh are not available in this mode. They can still be addressed by using the BSR.



NOTES:

TABLE 8-1: REGISTERS ASSOCIATED WITH DATA EEPROM MEMORY

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
EEADRH	EEPROM Address Register High Byte							
EEADR	EEPROM Address Register Low Byte							
EEDATA	EEPROM Data Register							
EECON2	EEPROM Control Register 2 (not a physical register)							
EECON1	EEPGD	CFGS	—	FREE	WRERR	WREN	WR	RD
IPR4	TMR4IP	EEIP	CMP2IP	CMP1IP	—	CCP5IP	CCP4IP	CCP3IP
PIR4	TMR4IF	EEIF	CMP2IF	CMP1IF	—	CCP5IF	CCP4IF	CCP3IF
PIE4	TMR4IE	EEIE	CMP2IE	CMP1IE	—	CCP5IE	CCP4IE	CCP3IE

Legend: — = unimplemented, read as ‘0’. Shaded cells are not used during Flash/EEPROM access.

12.0 DATA SIGNAL MODULATOR

Note:	The Data Signal Modulator is only available on 64-pin devices (PIC18F6XK80).

The Data Signal Modulator (DSM) is a peripheral which allows the user to mix a data stream, also known as a modulator signal, with a carrier signal to produce a modulated output.

Both the carrier and the modulator signals are supplied to the DSM module, either internally from the output of a peripheral, or externally through an input pin.

The modulated output signal is generated by performing a logical “AND” operation of both the carrier and modulator signals and then it is provided to the MDOUT pin.

The carrier signal is comprised of two distinct and separate signals: a carrier high (CARH) signal and a carrier low (CARL) signal. During the time in which the modulator (MOD) signal is in a logic high state, the DSM mixes the carrier high signal with the modulator signal. When the modulator signal is in a logic low state, the DSM mixes the carrier low signal with the modulator signal.

Using this method, the DSM can generate the following types of key modulation schemes:

- Frequency-Shift Keying (FSK)
- Phase-Shift Keying (PSK)
- On-Off Keying (OOK)

Additionally, the following features are provided within the DSM module:

- Carrier Synchronization
- Carrier Source Polarity Select
- Carrier Source Pin Disable
- Programmable Modulator Data
- Modulator Source Pin Disable
- Modulated Output Polarity Select
- Slew Rate Control

Figure 12-1 shows a simplified block diagram of the Data Signal Modulator peripheral.

REGISTER 12-3: MDCARH: MODULATION HIGH CARRIER CONTROL REGISTER

R/W-0	R/W-x	R/W-x	U-0	R/W-x	R/W-x	R/W-x	R/W-x
MDCHODIS	MDCHPOL	MDCHSYNC	—	MDCH3[1]	MDCH2[1]	MDCH1[1]	MDCH0[1]
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **MDCHODIS:** Modulator High Carrier Output Disable bit

`1` = Output signal driving the peripheral output pin (selected by MDCH<3:0>) is disabled
`0` = Output signal driving the peripheral output pin (selected by MDCH<3:0>) is enabled

bit 6 **MDCHPOL:** Modulator High Carrier Polarity Select bit

`1` = Selected high carrier signal is inverted
`0` = Selected high carrier signal is not inverted

bit 5 **MDCHSYNC:** Modulator High Carrier Synchronization Enable bit

`1` = Modulator waits for a falling edge on the high time carrier signal before allowing a switch to the low time carrier
`0` = Modulator output is not synchronized to the high time carrier signal[1]

bit 4 **Unimplemented:** Read as ‘`0`’

bit 3-0 **MDCH<3:0>** Modulator Data High Carrier Selection bits[1]

`1111-1001` = Reserved
`1000` = CCP5 output (PWM Output mode only)
`0111` = CCP4 output (PWM Output mode only)
`0110` = CCP3 output (PWM Output mode only)
`0101` = CCP2 output (PWM Output mode only)
`0100` = ECCP1 output (PWM Output mode only)
`0011` = Reference clock module signal
`0010` = MDCIN2 port pin
`0001` = MDCIN1 port pin
`0000` = VSS

Note 1: Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

16.5.4 TIMER3 GATE SINGLE PULSE MODE

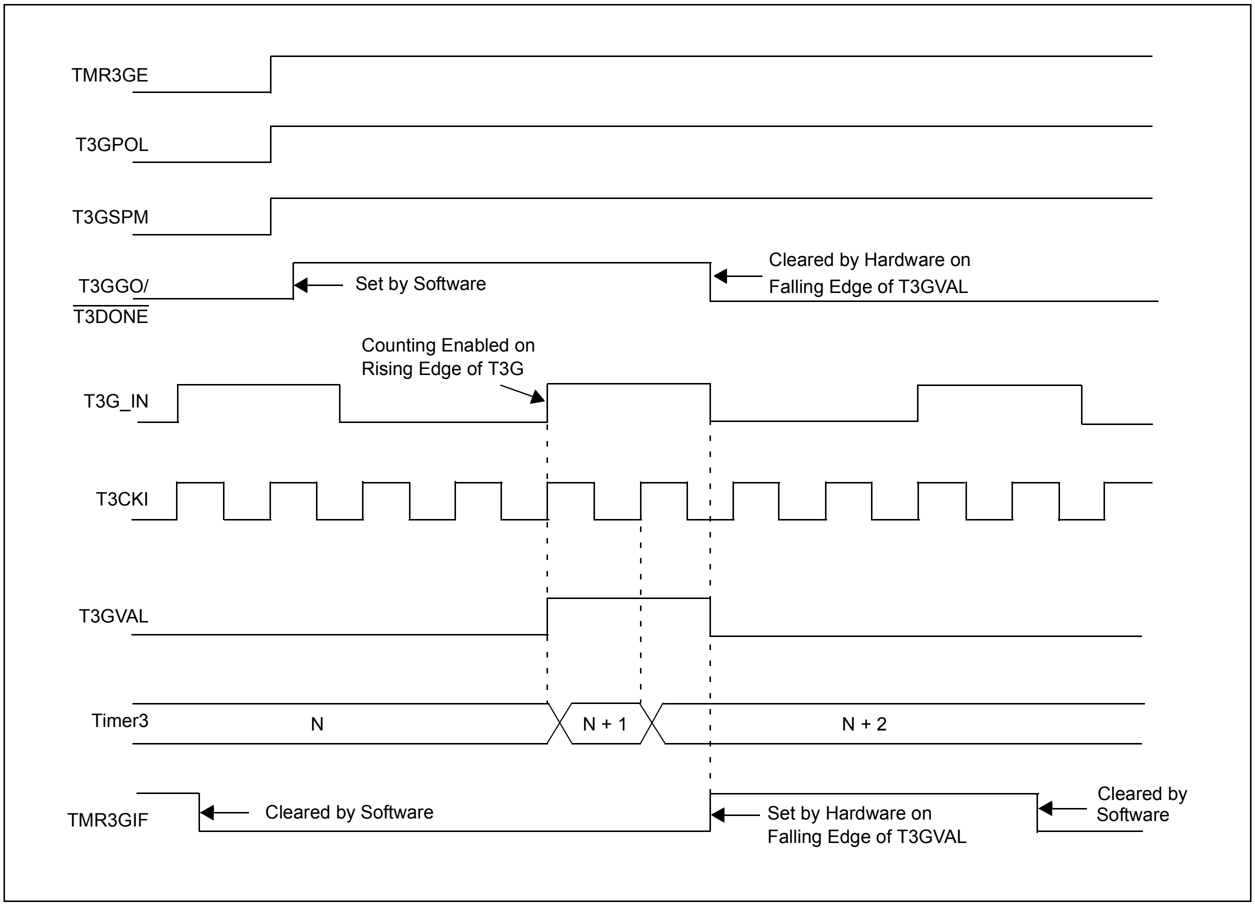
When Timer3 Gate Single Pulse mode is enabled, it is possible to capture a single pulse gate event. Timer3 Gate Single Pulse mode is first enabled by setting the T3GSPM bit (T3GCON<4>). Next, the T3GGO/$\overline{\text{T3DONE}}$ bit (T3GCON<3>) must be set.

The Timer3 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the T3GGO/$\overline{\text{T3DONE}}$ bit will automatically be cleared. No other gate events will be allowed to increment Timer3 until the T3GGO/$\overline{\text{T3DONE}}$ bit is once again set in software.

Clearing the T3GSPM bit will also clear the T3GGO/$\overline{\text{T3DONE}}$ bit. (For timing details, see Figure 16-4.)

Simultaneously enabling the Toggle mode and the Single Pulse mode will permit both sections to work together. This allows the cycle times on the Timer3 gate source to be measured. (For timing details, see Figure 16-5.)

FIGURE 16-4: TIMER3 GATE SINGLE PULSE MODE



20.4.2.1 Direction Change in Full-Bridge Mode

In the Full-Bridge mode, the P1M1 bit in the CCP1CON register allows users to control the forward/reverse direction. When the application firmware changes this direction control bit, the module will change to the new direction on the next PWM cycle.

A direction change is initiated in software by changing the P1M1 bit of the CCP1CON register. The following sequence occurs prior to the end of the current PWM period:

- The modulated outputs (P1B and P1D) are placed in their inactive state.
- The associated unmodulated outputs (P1A and P1C) are switched to drive in the opposite direction.
- PWM modulation resumes at the beginning of the next period.

For an illustration of this sequence, see Figure 20-10.

The Full-Bridge mode does not provide a dead-band delay. As one output is modulated at a time, a dead-band delay is generally not required. There is a situation where a dead-band delay is required. This situation occurs when both of the following conditions are true:

- The direction of the PWM output changes when the duty cycle of the output is at or near 100%.
- The turn-off time of the power switch, including the power device and driver circuit, is greater than the turn-on time.

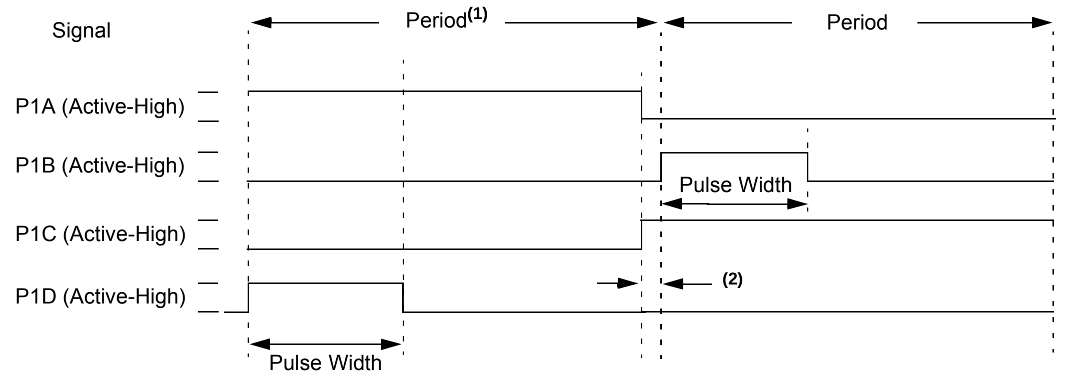
Figure 20-11 shows an example of the PWM direction changing from forward to reverse, at a near 100% duty cycle. In this example, at time, t1, the P1A and P1D outputs become inactive, while the P1C output becomes active. Since the turn-off time of the power devices is longer than the turn-on time, a shoot-through current will flow through power devices, QC and QD (see Figure 20-8), for the duration of ‘t’. The same phenomenon will occur to power devices, QA and QB, for PWM direction change from reverse to forward.

If changing PWM direction at high duty cycle is required for an application, two possible solutions for eliminating the shoot-through current are:

- Reduce PWM duty cycle for one PWM period before changing directions.
- Use switch drivers that can drive the switches off faster than they can drive them on.

Other options to prevent shoot-through current may exist.

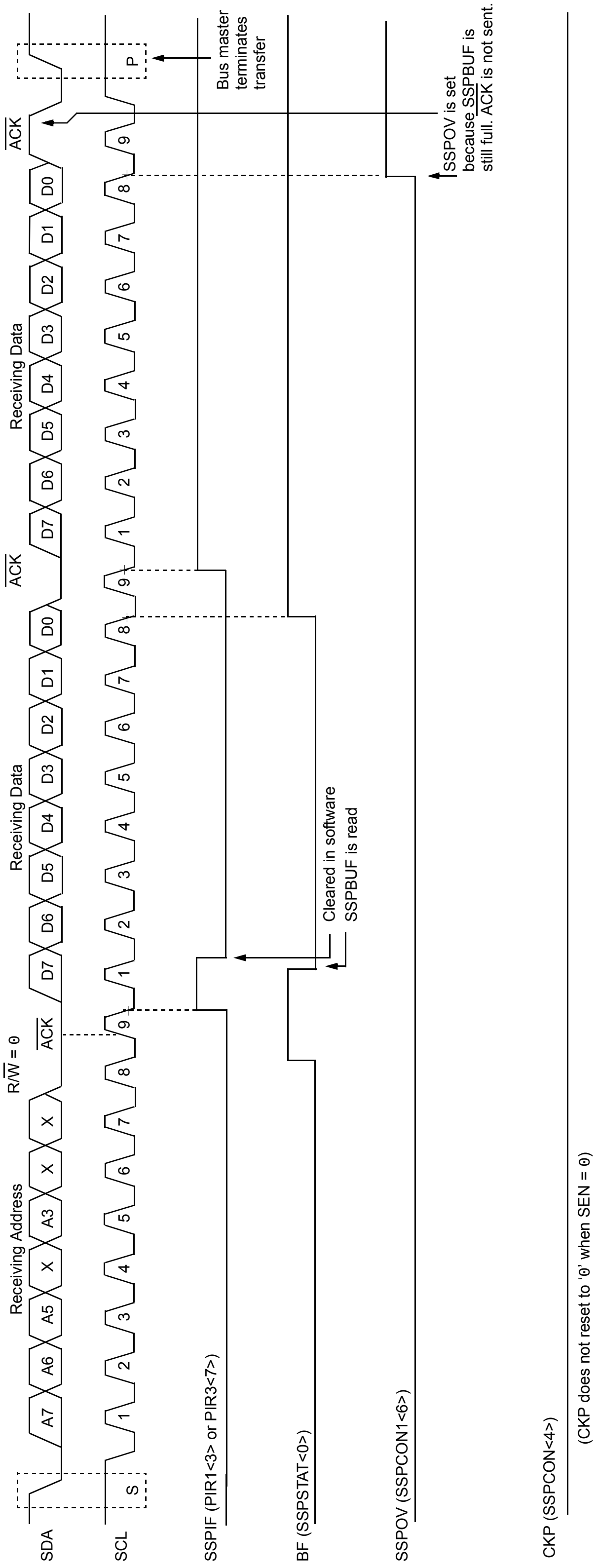
FIGURE 20-10: EXAMPLE OF PWM DIRECTION CHANGE



Note 1: The direction bit, P1M1 of the CCP1CON register, is written any time during the PWM cycle.

2: When changing directions, the P1A and P1C signals switch before the end of the current PWM cycle. The modulated P1B and P1D signals are inactive at this time. The length of this time is: (1/FOSC) • TMR2 Prescale Value.

FIGURE 21-9: I^2C™ SLAVE MODE TIMING WITH SEN = `0` AND ADMSK<5:1> = `01011` (RECEPTION, 7-BIT ADDRESS)



Note 1: x = Don't care (i.e., address bit can either be a '1' or a '0').

2: In this example, an address equal to A7.A6.A5.X.A3.X.X will be Acknowledged and cause an interrupt.

FIGURE 21-16: I^2C™ SLAVE MODE TIMING WITH SEN = 1 (RECEPTION, 10-BIT ADDRESS)

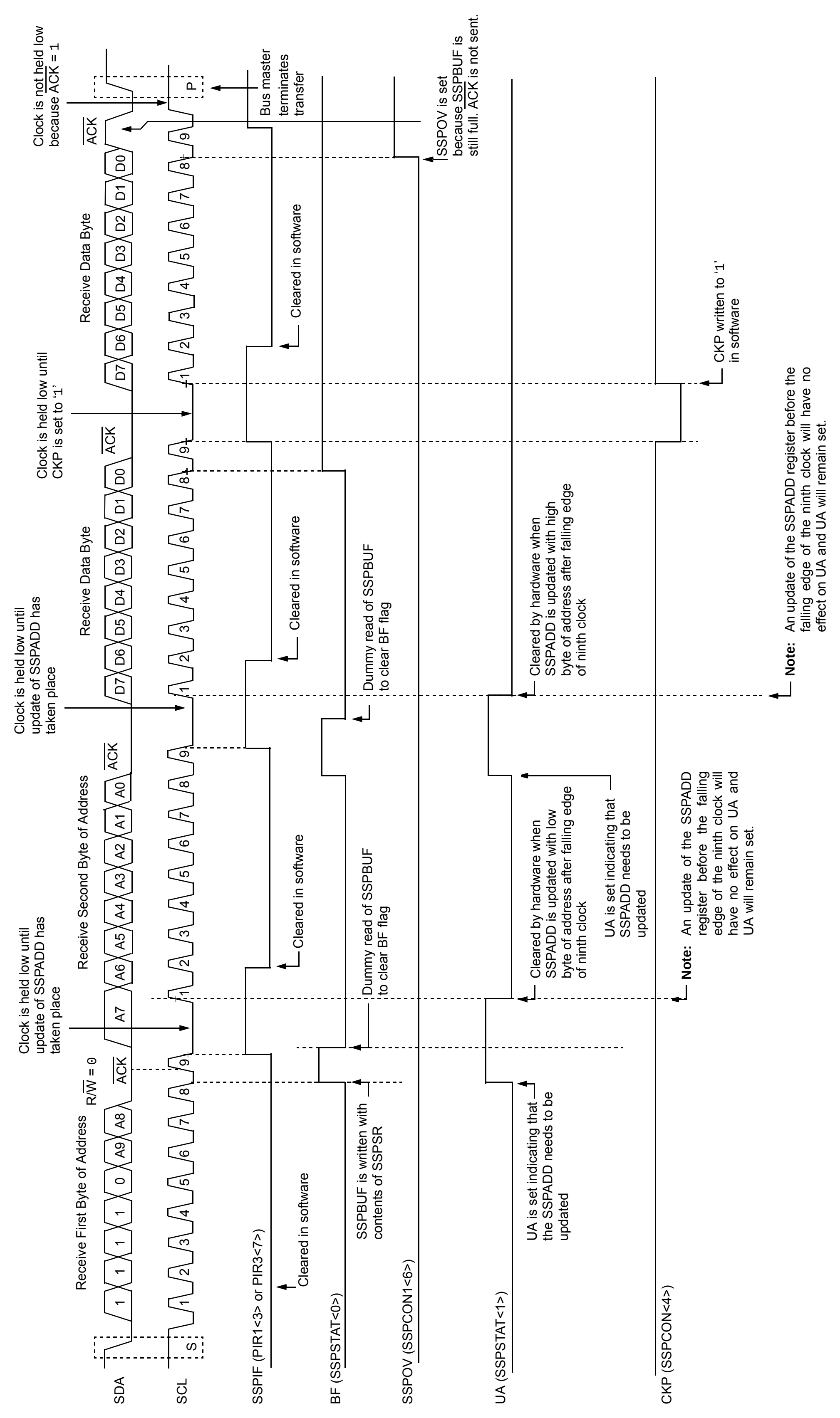
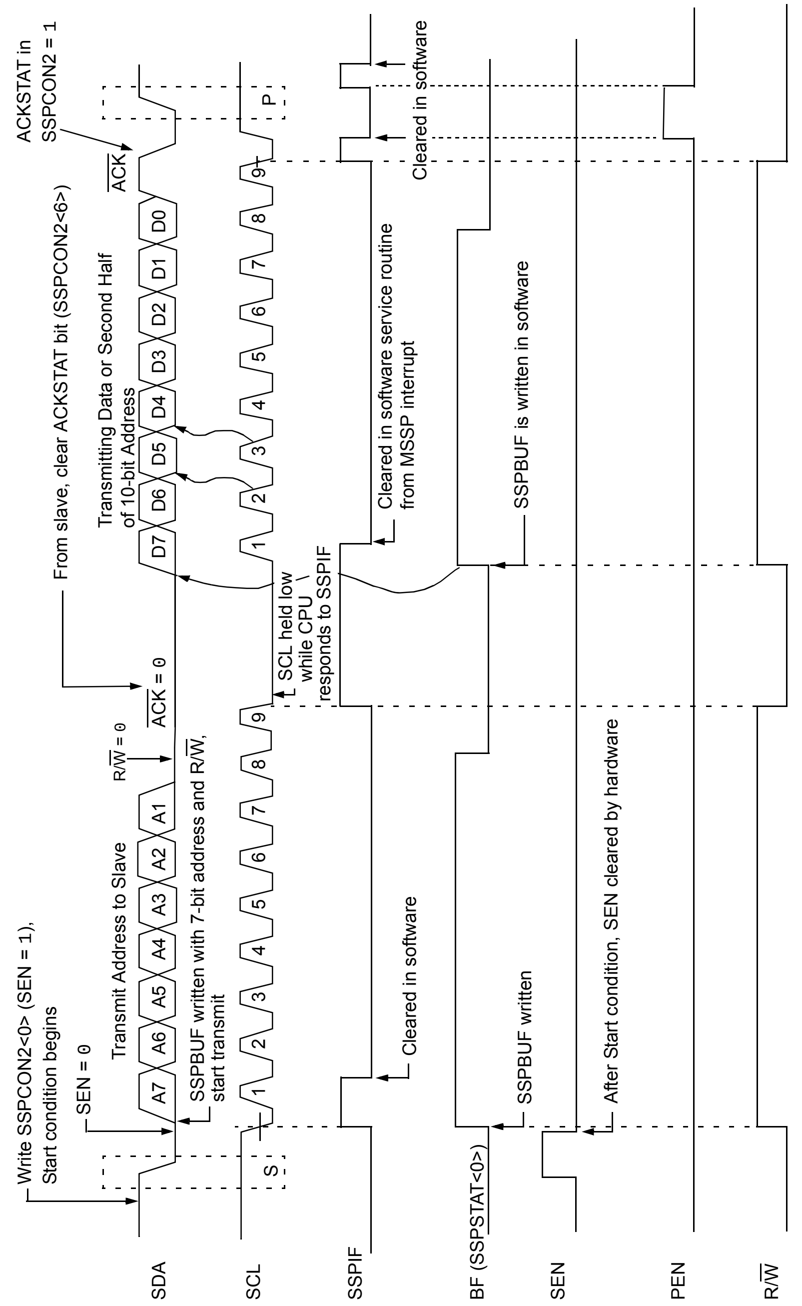


FIGURE 21-23: I²C™ MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESS)



REGISTER 23-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified
0 = Left justified

bit 6 **Unimplemented:** Read as ‘0’

bit 5-3 **ACQT<2:0>:** A/D Acquisition Time Select bits

111 = 20 TAD
110 = 16 TAD
101 = 12 TAD
100 = 8 TAD
011 = 6 TAD
010 = 4 TAD
001 = 2 TAD
000 = 0 TAD(1)

bit 2-0 **ADCS<2:0>:** A/D Conversion Clock Select bits

111 = FRC (clock derived from A/D RC oscillator)(1)
110 = FOSC/64
101 = FOSC/16
100 = FOSC/4
011 = FRC (clock derived from A/D RC oscillator)(1)
010 = FOSC/32
001 = FOSC/8
000 = FOSC/2

Note 1: If the A/D FRC clock source is selected, a delay of one TCY (instruction cycle) is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed before starting a conversion.

26.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

The PIC18F66K80 family of devices has a High/Low-Voltage Detect module (HLVD). This is a programmable circuit that sets both a device voltage trip point and the direction of change from that point. If the device experiences an excursion past the trip point in that direction, an interrupt flag is set. If the interrupt is enabled, the program execution branches to the interrupt vector address and the software responds to the interrupt.

The High/Low-Voltage Detect Control register (Register 26-1) completely controls the operation of the HLVD module. This allows the circuitry to be “turned off” by the user under software control, which minimizes the current consumption for the device.

The module’s block diagram is shown in Figure 26-1.

REGISTER 26-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VDIRMAG	BGVST	IRVST	HLVDEN	HLVDL3[(1)]	HLVDL2[(1)]	HLVDL1[(1)]	HLVDL0[(1)]
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **VDIRMAG:** Voltage Direction Magnitude Select bit

`1` = Event occurs when voltage equals or exceeds trip point (HLVDL<3:0>)
`0` = Event occurs when voltage equals or falls below trip point (HLVDL<3:0>)

bit 6 **BGVST:** Band Gap Reference Voltages Stable Status Flag bit

`1` = Internal band gap voltage references are stable
`0` = Internal band gap voltage references are not stable

bit 5 **IRVST:** Internal Reference Voltage Stable Flag bit

`1` = Indicates that the voltage detect logic will generate the interrupt flag at the specified voltage range
`0` = Indicates that the voltage detect logic will not generate the interrupt flag at the specified voltage range and the HLVD interrupt should not be enabled

bit 4 **HLVDEN:** High/Low-Voltage Detect Power Enable bit

`1` = HLVD enabled
`0` = HLVD disabled

bit 3-0 **HLVDL<3:0>:** Voltage Detection Limit bits[(1)]

`1111` = External analog input is used (input comes from the HLVDIN pin)
`1110` = Maximum setting
.
.
.
`0000` = Minimum setting

Note 1: For the electrical specifications, see Parameter D420 in **Section 31.0 “Electrical Characteristics”**.

REGISTER 27-48: MSEL0: MASK SELECT REGISTER 0[1]

R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
FIL3_1	FIL3_0	FIL2_1	FIL2_0	FIL1_1	FIL1_0	FIL0_1	FIL0_0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **FIL3_<1:0>:** Filter 3 Select bits 1 and 0

`11` = No mask
`10` = Filter 15
`01` = Acceptance Mask 1
`00` = Acceptance Mask 0

bit 5-4 **FIL2_<1:0>:** Filter 2 Select bits 1 and 0

`11` = No mask
`10` = Filter 15
`01` = Acceptance Mask 1
`00` = Acceptance Mask 0

bit 3-2 **FIL1_<1:0>:** Filter 1 Select bits 1 and 0

`11` = No mask
`10` = Filter 15
`01` = Acceptance Mask 1
`00` = Acceptance Mask 0

bit 1-0 **FIL0_<1:0>:** Filter 0 Select bits 1 and 0

`11` = No mask
`10` = Filter 15
`01` = Acceptance Mask 1
`00` = Acceptance Mask 0

Note 1: This register is available in Mode 1 and 2 only.

TABLE 29-2: PIC18F66K80 FAMILY INSTRUCTION SET (CONTINUED)

Mnemonic, Operands		Description	Cycles	16-Bit Instruction Word				Status Affected	Notes
				MSb			LSb		
BIT-ORIENTED OPERATIONS									
BCF	f, b, a	Bit Clear f	1	`1001`	`bbba`	`ffff`	`ffff`	None	1, 2
BSF	f, b, a	Bit Set f	1	`1000`	`bbba`	`ffff`	`ffff`	None	1, 2
BTFSC	f, b, a	Bit Test f, Skip if Clear	1 (2 or 3)	`1011`	`bbba`	`ffff`	`ffff`	None	3, 4
BTFSS	f, b, a	Bit Test f, Skip if Set	1 (2 or 3)	`1010`	`bbba`	`ffff`	`ffff`	None	3, 4
BTG	f, b, a	Bit Toggle f	1	`0111`	`bbba`	`ffff`	`ffff`	None	1, 2
CONTROL OPERATIONS									
BC	n	Branch if Carry	1 (2)	`1110`	`0010`	`nnnn`	`nnnn`	None	
BN	n	Branch if Negative	1 (2)	`1110`	`0110`	`nnnn`	`nnnn`	None	
BNC	n	Branch if Not Carry	1 (2)	`1110`	`0011`	`nnnn`	`nnnn`	None	
BNN	n	Branch if Not Negative	1 (2)	`1110`	`0111`	`nnnn`	`nnnn`	None	
BNOV	n	Branch if Not Overflow	1 (2)	`1110`	`0101`	`nnnn`	`nnnn`	None	
BNZ	n	Branch if Not Zero	1 (2)	`1110`	`0001`	`nnnn`	`nnnn`	None	
BOV	n	Branch if Overflow	1 (2)	`1110`	`0100`	`nnnn`	`nnnn`	None	
BRA	n	Branch Unconditionally	2	`1101`	`0nnn`	`nnnn`	`nnnn`	None	
BZ	n	Branch if Zero	1 (2)	`1110`	`0000`	`nnnn`	`nnnn`	None	
CALL	n, s	Call Subroutine 1st word	2	`1110`	`110s`	`kkkk`	`kkkk`	None	
		2nd word		`1111`	`kkkk`	`kkkk`	`kkkk`		
CLRWDT	—	Clear Watchdog Timer	1	`0000`	`0000`	`0000`	`0100`	$\overline{\text{TO}}$, $\overline{\text{PD}}$	
DAW	—	Decimal Adjust WREG	1	`0000`	`0000`	`0000`	`0111`	C	
GOTO	n	Go to Address 1st word	2	`1110`	`1111`	`kkkk`	`kkkk`	None	
		2nd word		`1111`	`kkkk`	`kkkk`	`kkkk`		
NOP	—	No Operation	1	`0000`	`0000`	`0000`	`0000`	None	
NOP	—	No Operation	1	`1111`	`xxxx`	`xxxx`	`xxxx`	None	4
POP	—	Pop Top of Return Stack (TOS)	1	`0000`	`0000`	`0000`	`0110`	None	
PUSH	—	Push Top of Return Stack (TOS)	1	`0000`	`0000`	`0000`	`0101`	None	
RCALL	n	Relative Call	2	`1101`	`1nnn`	`nnnn`	`nnnn`	None	
RESET		Software Device Reset	1	`0000`	`0000`	`1111`	`1111`	All	
RETFIE	s	Return from Interrupt Enable	2	`0000`	`0000`	`0001`	`000s`	GIE/GIEH, PEIE/GIEL	
RETLW	k	Return with Literal in WREG	2	`0000`	`1100`	`kkkk`	`kkkk`	None	
RETURN	s	Return from Subroutine	2	`0000`	`0000`	`0001`	`001s`	None	
SLEEP	—	Go into Standby mode	1	`0000`	`0000`	`0000`	`0011`	$\overline{\text{TO}}$, $\overline{\text{PD}}$	

Note 1: When a PORT register is modified as a function of itself (e.g., `MOVF PORTB, 1, 0`), the value used will be that value present on the pins themselves. For example, if the data latch is '`1`' for a pin configured as an input and is driven low by an external device, the data will be written back with a '`0`'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = `1`), the prescaler will be cleared if assigned.

3: If the Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

4: Some instructions are two-word instructions. The second word of these instructions will be executed as a `NOP` unless the first word of the instruction retrieves the information embedded in these 16 bits. This ensures that all program memory locations have a valid instruction.

BNC Branch if Not Carry

Syntax:	BNC n
Operands:	-128 ≤ n ≤ 127
Operation:	if Carry bit is ‘`0`’, (PC) + 2 + 2n → PC
Status Affected:	None
Encoding:	`1110` `0011` `nnnn` `nnnn`
Description:	If the Carry bit is ‘`0`’, then the program will branch. The 2’s complement number, ‘2n’, is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction.
Words:	1
Cycles:	1(2)

Q Cycle Activity:
If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal ‘n’	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal ‘n’	Process Data	No operation

Example: `HERE BNC Jump`

Before Instruction
PC = address `(HERE)`
After Instruction
If Carry = `0;`
PC = address `(Jump)`
If Carry = `1;`
PC = address `(HERE + 2)`

BNN Branch if Not Negative

Syntax:	BNN n
Operands:	-128 ≤ n ≤ 127
Operation:	if Negative bit is ‘`0`’, (PC) + 2 + 2n → PC
Status Affected:	None
Encoding:	`1110` `0111` `nnnn` `nnnn`
Description:	If the Negative bit is ‘`0`’, then the program will branch. The 2’s complement number, ‘2n’, is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction.
Words:	1
Cycles:	1(2)

Q Cycle Activity:
If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal ‘n’	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal ‘n’	Process Data	No operation

Example: `HERE BNN Jump`

Before Instruction
PC = address `(HERE)`
After Instruction
If Negative = `0;`
PC = address `(Jump)`
If Negative = `1;`
PC = address `(HERE + 2)`

31.2 DC Characteristics: Power-Down and Supply Current PIC18F66K80 Family (Industrial/Extended) (Continued)

PIC18F66K80 Family (Industrial/Extended)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for industrial -40°C ≤ T_A ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (I_{DD}) Cont.[2,3]						
	PIC18**LF**XXK80	330	480	μA	-40°C	V_{DD} = 1.8V[4] Regulator Disabled	F_{OSC} = 4 MHz (**RC_IDLE** mode, Internal HF-INTOSC)
		330	480	μA	+25°C		
		330	480	μA	+60°C		
		340	500	μA	+85°C		
		350	540	μA	+125°C		
	PIC18**LF**XXK80	522	720	μA	-40°C	V_{DD} = 3.3V[4] Regulator Disabled	
		522	720	μA	+25°C		
		522	720	μA	+60°C		
		540	740	μA	+85°C		
		550	780	μA	+125°C		
	PIC18**F**XXK80	540	760	μA	-40°C	V_{DD} = 3.3V[5] Regulator Enabled	
		540	760	μA	+25°C		
		540	760	μA	+60°C		
		560	780	μA	+85°C		
		580	810	μA	+125°C		
	PIC18**F**XXK80	600	1250	μA	-40°C	V_{DD} = 5V[5] Regulator Enabled	
		600	1250	μA	+25°C		
		600	1250	μA	+60°C		
		610	1300	μA	+85°C		
		620	1340	μA	+125°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to V_{DD} or V_{SS}, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD};
$\overline{\text{MCLR}}$ = V_{DD}; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: For LF devices, $\overline{\text{RETEN}}$ (CONFIG1L<0>) = `1`.

5: For F devices, SRETEN (WDTCON<4>) = `1` and $\overline{\text{RETEN}}$ (CONFIG1L<0>) = `0`.

31.2 DC Characteristics: Power-Down and Supply Current PIC18F66K80 Family (Industrial/Extended) (Continued)

PIC18F66K80 Family (Industrial/Extended)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Module Differential Currents (ΔIWDT, ΔIBOR, ΔIHLVD, ΔIADC)						
D022 (ΔIWDT)	**Watchdog Timer**						
	PIC18**LF**XXK80	0.4	2	μA	-40°C to +125°C	VDD = 1.8V Regulator Disabled	
	PIC18**LF**XXK80	0.6	3	μA	-40°C to +125°C	VDD = 3.3V Regulator Disabled	
	PIC18**F**XXK80	0.6	3	μA	-40°C to +125°C	VDD = 3.3V Regulator Enabled	
	PIC18**F**XXK80	0.8	4	μA	-40°C to +125°C	VDD = 5.5V Regulator Enabled	
D022A (ΔIBOR)	**Brown-out Reset**						
	PIC18**LF**XXK80	4.6	20	μA	-40°C to +125°C	VDD = 1.8V Regulator Disabled	High-Power BOR
	PIC18**F**XXK80	4.6	20	μA	-40°C to +125°C	VDD = 3.3V Regulator Enabled	
	PIC18**F**XXK80	4.6	20	μA	-40°C to +125°C	VDD = 5.5V Regulator Enabled	
D022B **ΔIHLVD**	**High/Low-Voltage Detect**						
	PIC18**LF**XXK80	3.8	10	μA	-40°C to +125°C	VDD = 1.8V Regulator Disabled	
	PIC18L**F**XXK80	4.5	12	μA	-40°C to +125°C	VDD = 3.3V Regulator Disabled	
	PIC18**F**XXK80	3.8	12	μA	-40°C to +125°C	VDD = 3.3V Regulator Enabled	
	PIC18**F**XXK80	4.9	13	μA	-40°C to +125°C	VDD = 5.5V Regulator Enabled	
D026 **ΔIADC**	**A/D Converter**						
	PIC18**LF**XXK80	0.4	1.5		-40°C to +125°C	VDD = 1.8V Regulator Disabled	A/D on, not converting
	PIC18L**F**XXK80	0.5	2	μA	-40°C to +125°C	VDD = 3.3V Regulator Disabled	
	PIC18**F**XXK80	0.5	3	μA	-40°C to +125°C	VDD = 3.3V Regulator Enabled	
	PIC18**F**XXK80	1	3	μA	-40°C to +125°C	VDD = 5.5V Regulator Enabled	

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to VDD or VSS, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

$\overline{\text{OSC1}}$ = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

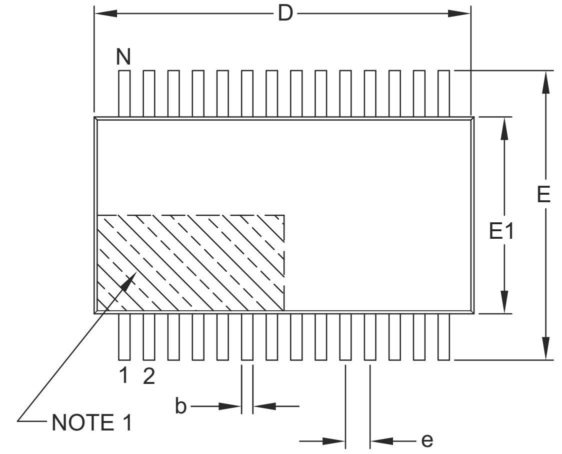
3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

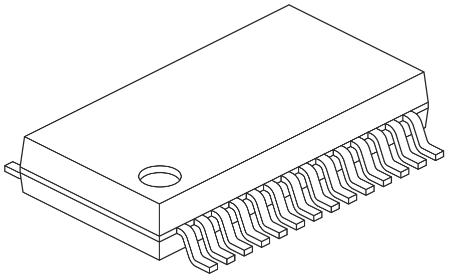
4: For LF devices, $\overline{\text{RETEN}}$ (CONFIG1L<0>) = `1`.

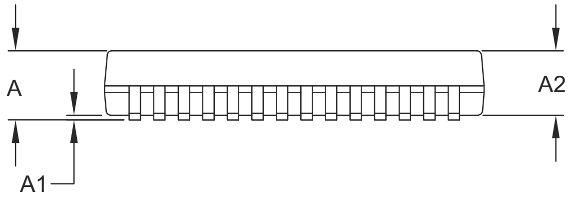
5: For F devices, SRETEN (WDTCON<4>) = `1` and $\overline{\text{RETEN}}$ (CONFIG1L<0>) = `0`.

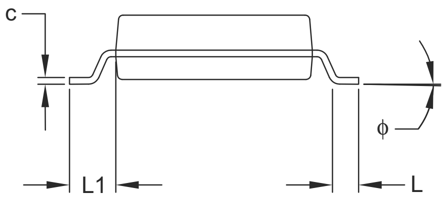
28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

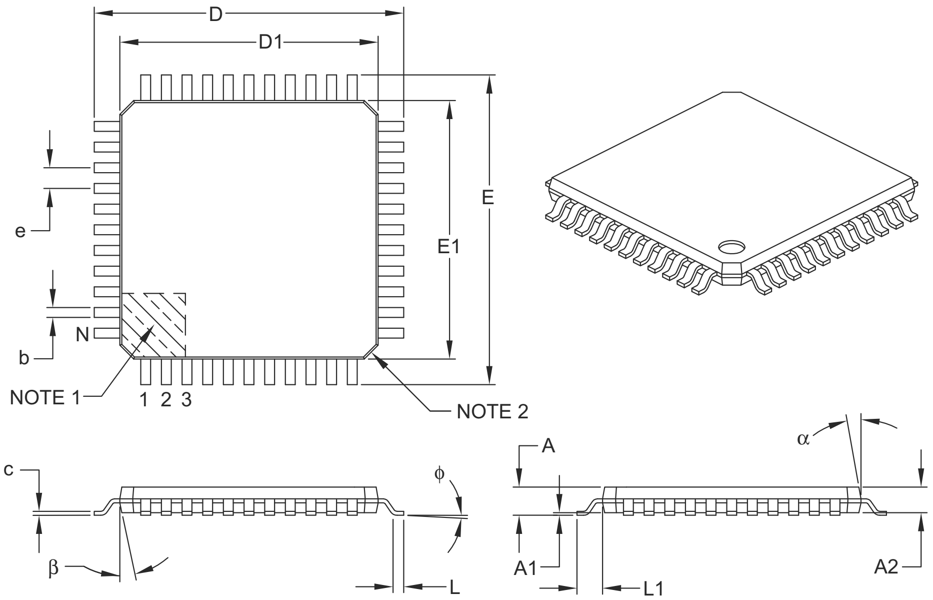
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Leads	N	44		
Lead Pitch	e	0.80 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	12.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B