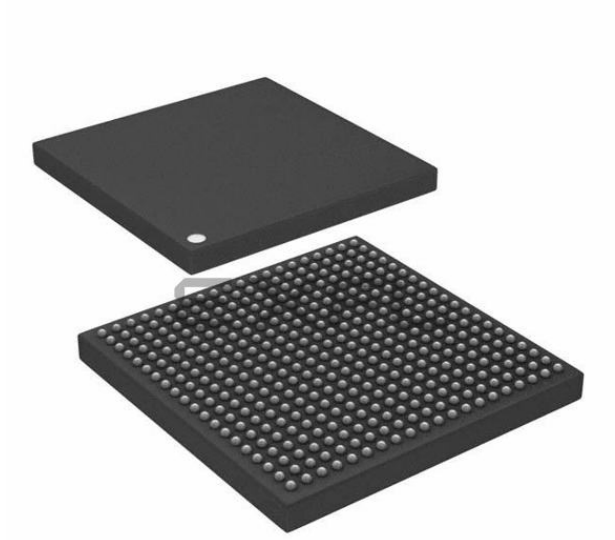
Renesas Electronics America Inc - R9A06G032NGBG#AC0 Datasheet



Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A7, ARM® Cortex®-M3
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	125MHz, 500MHz
Co-Processors/DSP	-
RAM Controllers	DDR2, DDR3
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.5V, 1.8V, 3.3V
Operating Temperature	-40°C ~ 110°C (TJ)
Security Features	-
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r9a06g032ngbg-ac0

Section 1 Overview

The Renesas RZ/N1D group, RZ/N1S group, RZ/N1L group are specifically tailored to meet the demands of Industrial Ethernet based applications.

1.1 Outline of Specifications

Table 1.1 Outline of Specifications (1/9)

Classification	Module/Function	Description
CPU	Arm Cortex-A7	• Arm 32-bit CPU Cortex-A7 (Revision r0p5) • Dual core or single core • Maximum operating frequency: 500 MHz • Clock frequency scaling • L1 cache: 16 KB/16 KB per core • L2 cache: up to 256 KB • FPU, VFPv4-D16 • MMU • Hardware coherent caches • Little endian
	Arm Cortex-M3	• Arm 32-bit CPU Cortex-M3 (Revision r2p1) • Maximum operating frequency: 125 MHz • Memory Protection Unit (MPU) • Little endian
Memory	On-chip 2 MB SRAM	• Capacity: 2 MB (1 MB + 1 MB) • Separated access ports per 512 KB unit • SEC-DED (Single Error Correction, Double Error Detection)
	On-chip 4 MB SRAM	• Capacity: 4 MB • Separated access ports per 1 MB unit • SEC-DED (Single Error Correction, Double Error Detection)
Watchdog		• Free running 12-bit decrementing counters with reload register • Output configurable to operate as a reset or interrupt signal • Stop/hangup watchdog effect while CPU is being stopped by debugger (e.g. by breakpoint execution)
Operating Modes		• Three boot modes (CA7) – NAND Flash – QSPI Flash – USB DFU
Clock	Clock Generation Circuit	• Input 40 MHz clock selectable from an oscillator or crystal • System clock up to 125 MHz • Cortex-A7 clock ×1/×2/×4 with system clock • DDR memory clock 250 MHz/500 MHz
RTC		• Time-of-day clock in 24-hour mode • Calendar • Alarm capability • XTAL 32 kHz • Separate and isolated power supply for RTC backup mode
Reset		• Master Reset input • Internal System Reset (Software, watchdog)

Table 1.1 Outline of Specifications (2/9)

Classification	Module/Function	Description
Data Transfer	Direct Memory Access Controller (DMAC)	• 2 units: – 8 channels, 16 request sources for DMAC1 – 8 channels, 16 request sources for DMAC2 • Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers • Transfer size: – 8, 16, 32, 64 bits • Programmable DMA burst size
	Mailbox	• 3 × programmable mailboxes – 7 × 32-bit data registers per mailbox
Parallel Bus Interface	Medium Speed External Bus Interface (MSEBI)	• Master and slave modes – Data bus width selectable from 8, 16 and 32 bits • Address/data/control-data are multiplexed on data bus • Burst mode • DMA Support – Master mode: Coupling with 4 DMA channels (external request reception capability) – Slave Mode: External request transmission capability • Up to 4 chip selects • Programmable address capability from 2B to 4GB • Programmable setup and hold time • External wait request
I/O Ports	IO Multiplexing	• Locations of IOs for peripherals are selectable • Output drive strength selectable • On-chip Pull-up/Pull-down select
Memory Interfaces	DDR2/3 Controller	• DDR2-500/DDR3-1000 • 16 bits, 8 bits, 8 + ECC bits • Up to 2 chip selects and 2 ODT • Up to 2 GB address capability • ECC SEC/DED software configurable (enable/disable) • Programmable on die termination • Configurable impedance drive and slew rate • DDR2/DDR3 low power control management (by software) • Port Address Protection Check – Up to 16 address protection regions per port
	NAND Flash Controller	• NAND interface with 8-bit bus width • Support for asynchronous mode • 4 chip selects • Write protection • Programmable address cycle (0/1/2/3/4/5) • Integrated DMA • Support for 256 B, 512 B, 2 KB, 1 KB, 4 KB, 8 KB, 16 KB pages • BCH ECC (Error detection and data correction) – ECC data block size: 256 B, 512 B, 1024 B – ECC correction capability: 2, 4, 8, 16, 24, 32 bits errors • Bad Block Management (BBM)

Table 1.1 Outline of Specifications (3/9)

Classification	Module/Function	Description
Memory Interfaces	Quad SPI (QSPI)	• Up to 2 units • Single, dual or quad I/O instructions supported • Execute in Place (XIP) supported • Remap address direct access • Programmable device sizes • Up to 4 chip selects • Support for 1/2/3/4 byte addressing • Support for programmable page size (default 256 bytes) • Support for programmable number of bytes per device block • Programmable write protected regions • Legacy mode allowing software direct access to low level transmit and receive FIFOs • Set of control registers to perform any FLASH command • Support for write burst in direct access
	SD/SDIO/eMMC	• Up to 2 units • SD/SDIO Card interface – Transfers data in 1 bit or 4 bits mode – Transfers data in Default or High Speed mode • eMMC card interface – Transfers data in 1 bit, 4 bits, or 8 bits mode • Speeds – Default mode up to 25 MHz – High Speed mode up to 50 MHz • Support for PIO/SDMA/ADMA transfer
Networking Elements	R-IN Engine	• µITRON-like system calls – 30 system calls for elements such as events, semaphores, and mailboxes • Task Scheduler (Ver. 4.2) – Hardware ISR: 32 routines selectable from 128 QINT routines – Number of context elements: 64 – Number of semaphore identifiers: 128 – Number of event identifiers: 64 – Number of mailbox identifiers: 64 – Number of mailbox elements: 192 – Number of context priority levels: 16 • Hardware function manager • Internal DMA controller • Buffer allocator • Header EnDec • Dedicated Gigabit Ethernet MAC (with built-in MAC DMAC)

Table 1.1 Outline of Specifications (4/9)

Classification	Module/Function	Description
Networking Elements	Advanced 5 Port Switch	• Operation modes: – 10 Mb half- and full-duplex – 100 Mb half- and full-duplex – 1000 Mb full-duplex only • MAC based RMON statistics counters/per port • Port statistics on per port basis (no aggregation) • Look-up table up to 8192 MAC addresses (static and learned) • Packet buffer size: 1 Mbit • 4 queues with individual QoS levels, supporting frame priority classification for the flexible handling of output queues – Optional arbitration management through weighted fair queuing • Support for Ethernet multicast and broadcast frames with flooding control to avoid unnecessary duplication of frames (storm protection) • Programmable multicast destination port mask to restrict frame duplication for individual multicast addresses • IEEE 1588-2008 compatible – Support for 1 step Peer-to-Peer (P2P) (Layer 2 only) – Support for 1 step End-to-End (E2E) (Layer 2 only) • Multicast and broadcast resolution with VLAN domain filtering providing a strict separation of up to 32 VLANs • Support for reception and transmission of VLAN frames • Programmable addition, removal and manipulation of ingress and egress VLAN tags, supporting single and double-tagged VLAN frames on each port • Support for standard frame size (1536 bytes), extended frame sizes up to 1700 bytes and jumbo frames up to 10 Kbytes • Port mirroring programmable per port • RSTP port states (3 for RSTP/ 5 for STP) – RSTP Port states learning, discarding, forwarding configurable per port – BPDU frame supported – MSTP BPDU frame supported (software) • Start in Managed mode • Frame snooping engine • Standalone Energy-Efficient-Ethernet (EEE) management • Filter access per port to assigned addresses only • Programmable egress rate limit per port • Ingress Configurable Broadcast storm protection per port • Ingress Configurable Multicast storm protection per port • 802.1x source address authentication supported • 802.1x guest VLAN supported • PRP functionality (IEC 62439-3 edition 2.0- 2012) • DLR/HUB module • Cut-through • TDMA (Time Division Multiple Access) 4 time slots • Pattern Matchers 8 channels • Remote monitoring via SNMP and the (RMON/MIB) • Powerlink capable Hub

Table 1.1 Outline of Specifications (5/9)

Classification	Module/Function	Description
Networking Elements	HSR Switch	• HSR functionality (IEC 62439-3 edition 2.0- 2012) – DANH – Redundancy Box (Red Box) – Generation of redundant transmit frames – Filtering of duplicated received frames – Redundancy header generation and detection – Table to keep track of received frames • 100 Mbps full-duplex Ethernet • Dynamic frame buffer allocation (page manager) • 128 proxy nodes (VDANs) supported • Support for link-local protocols • Duplicate detection memory • MAC address filtering • 1 × VLAN tag supported • Port statistics on per port basis (no aggregation) • 144 KB frame buffer • IEEE1588 - 2008 • Support for Ethernet multicast frames with flooding control • Extended frame size: up to 2000 bytes (Jumbo frames not supported) • Support for a minimum of 16 nodes in an HSR loop • Configurable duplicate detection residence time
	EtherCAT Slave Controller	• Up to 3 ports • Automatic TX Shift • Enhanced Link Detection • 8 FMMU (Fieldbus Memory Management Unit) • 8 SyncManagers • 64-bit Distributed Clocks • Mapping to global IRQ • Read/Write Offset • Write Protection • AL Status Code Register • Extended Watchdog • AL Event Mask Register • Watchdog Counter • SyncManager Event Times • EPU Error Counter • Lost Link Counter • I^2C interface for external EEPROM
	SercosIII Slave Controller	• 2 ports • Data and clock regeneration • Telegram processing for automatic transmission, and monitoring of synchronization telegrams and data telegrams • Switch over function between Sercos protocol and standard Ethernet protocol via multiplexer • Monitors the received data stream to detect the frame type and starts operation when SercosIII frame type is detected • Handling of the data transfers to and from SRAM based on telegram type (MST/MDT or AT) and operation mode (master or slave)

Table 1.1 Outline of Specifications (6/9)

Classification	Module/Function	Description
Networking Elements	Independent GMAC	• 2 × MAC instances (GMAC1, GMAC2) • Compliance with the following standards: – IEEE 1588-2008 v2 standard for precision networked clock synchronization – IEEE 1588-2008 v2 is compliant with Power IEEE-C37.238 profile – IEEE 802.3-az-2010 for Energy Efficient Ethernet (EEE) • Support for 10/100/1000 Mbps data transfer rates • Support for both half-duplex and full-duplex operation • Programmable frame length to support both standard and “jumbo” Ethernet frames with size up to 16 Kbytes (16KB-1) • 17 MAC address registers for the address filter block • Variety of flexible addresses filtering modes are supported • Native DMA with simple-independent channels for transmit and receive engines • Advanced IEEE1588-2002 & 2008 Ethernet frame time-stamping supported • Provides the flexibility to control the Pulse-Per-Second (PPS) output signal (one MAC only) • Programmable CRC generation and checking • Support for RMON statistics (setting for reduction in IP layer only) • Station Management Block, MDIO interface
Subsystem Elements	USB2.0 HOST	• 1 dedicated port + 1 configurable port (Host or Function) • Supports: – High speed (HS): 480 Mbps (USB 2.0) – Full speed (FS): 12 Mbps (USB 1.1) – Low speed (LS): 1.5 Mbps (USB 1.1) • USB Plug Detect (UPD) • Output port power switch management • Overcurrent indication from application • Integrated DMA • Transmit and receive FIFOs
	USB2.0 Function	• 1 configurable port (Host or Function) • Supports: – High speed (HS): 480 Mbps (USB 2.0) – Full speed (FS): 12 Mbps (USB 1.1) • USB Plug Detect (UPD) which detects the connection of a host via VBUS • 16 physical endpoints • Integrated DMA • Endpoint buffer
	UART 1, 2, 3	• Compliant with 16550 UART • Separate 16×8 (16 location depth × 8-bit width) transmit and 16×8 receive FIFOs • RS485 & MODBUS® enhanced features • Baud rate generation up to 5.2 Mbaud • Generation and detection of line breaks • Programmable hardware flow control • Auto Flow Control mode as specified in the 16750 standard • Supports TXD, RXD, CTS_N, RTS_N, DTR_N, DSR_N, DCD_N, RI_N
	UART 4, 5, 6, 7, 8	• In addition to UART 1, 2, 3, the following function is available: – DMA coupling with burst-mode management

Table 1.1 Outline of Specifications (7/9)

Classification	Module/Function	Description
Subsystem Elements	SPI 1, 2, 3, 4 (Master)	• Transmit and receive FIFOs (16 × 16) • Programmable RXD sampling logic • Programmable data-size for frames (from 4 to 16 bits) • 4 chip selects • DMA controller interface
	SPI 5, 6 (Slave)	• Transmit and receive FIFOs (16 × 16) • Programmable data-size for frames (from 4 to 16 bits) • DMA controller interface
	I^2C 1, 2	• Two speeds: – Standard mode (0 to 100 Kbps) – Fast mode (≤ 400 Kbps) • Separated 8×8 transmit and 8×8 receive FIFOs • Master or slave I^2C operation • 7- or 10-bit addressing • 7- or 10-bit combined format transfers • Bulk transmit mode • Programmable SDA hold time ($t_{HD; DAT}$)
	CAN 1, 2	• Supports both 11-bit and 29-bit identifiers • Supports bit rates from 125 Kbps to 1 Mbps • Acceptance filtering • Software-driven bit-rate detection (offering hot plug-in support) • Single-shot transmission option, listen-only mode, reception of ‘own’ messages • Arbitration lost interrupt with record of bit position • Read/write error counters • Last error register • Programmable error limit warning • Transmit periodic “Sync frame” • Programmable time base
	General Purpose Timers	• 2 units, each supporting: – 6 programmable 16-bit timers – 2 programmable 32-bit timers • Prescaler selectable between 2 time bases • Auto-reload mode or single-shot mode • DMA coupling (only for the 32-bit timers)

Table 1.1 Outline of Specifications (8/9)

Classification	Module/Function	Description
ADC	ADC	• Up to 2 units • Resolution 12 bits • Sampling rate from 0.0625 MSPS to 1 MSPS • Analog inputs – 8 channels: (5 ch + 3 ch S/H) • Individual trigger per channel • DNL, ± 1.0 LSB (Max.) [at VAIN = 0.0 V to AVDD, f_{CLK} = 20 MHz] • INL, ± 4.0 LSB (Max.) [at VAIN = 0.0 V to AVDD, f_{CLK} = 20 MHz] • Power-down mode • Two level of priority • Round-robin management of simultaneous conversion requests with the same level of priority. • DMA coupling • Virtual channel capability
Multimedia	LCD Controller	• Programmable LCD Panel resolutions • Interface for 1 Port TFT LCD Panel: – 18-bit digital (6 bits/color) – 24-bit digital (8 bits/color) • Programmable frame buffer bits-per-pixel (bpp) – 1, 2, 4, 8 bpp mapped through Color Palette to 18-bit LCD pixel – 16, 18, bpp directly drive 18-bit LCD pixel – 24 bpp directly drive 24-bit LCD pixel • Hardware blink supported • Pulse Width Modulation module for LCD panel LED backlight brightness control • Power up and down sequencing supported • Integrated DMA
Safety Elements (option)*1	Clock Monitoring	• Monitors abnormal output clock frequency from the PLL circuit or on-chip oscillator
	Watchdog Safe	• Allow to generate a system reset in event of SW failure
	Safety Reset	• Allow to generate an external reset output
	Safety Filtering	• Allow to prevent unauthorized memory access
Debugging Interface		• ETM coupled with JTAG debugger • Single Embedded Trace Buffer (32 KB) shared by Cortex-A7 and Cortex-M3 cores • Arm JTAG • Arm SWD
Power Supply Voltage		• Core Voltage: 1.15 V ± 0.05 V • IO voltage: 3.3 V • DDR IO voltage: 1.8 V; 1.5 V
Operating Temperature		Junction temperature: −40°C to +110°C

Note 1. Details of these optional functions will only be disclosed after completion of a binding NDA. For details, please contact local Renesas sales.

1.2 SoC Block Diagram

Please refer to **Section 1.3, Function Comparison per Device Family and Package** about available functions according to the package.

1.2.1 RZ/N1D

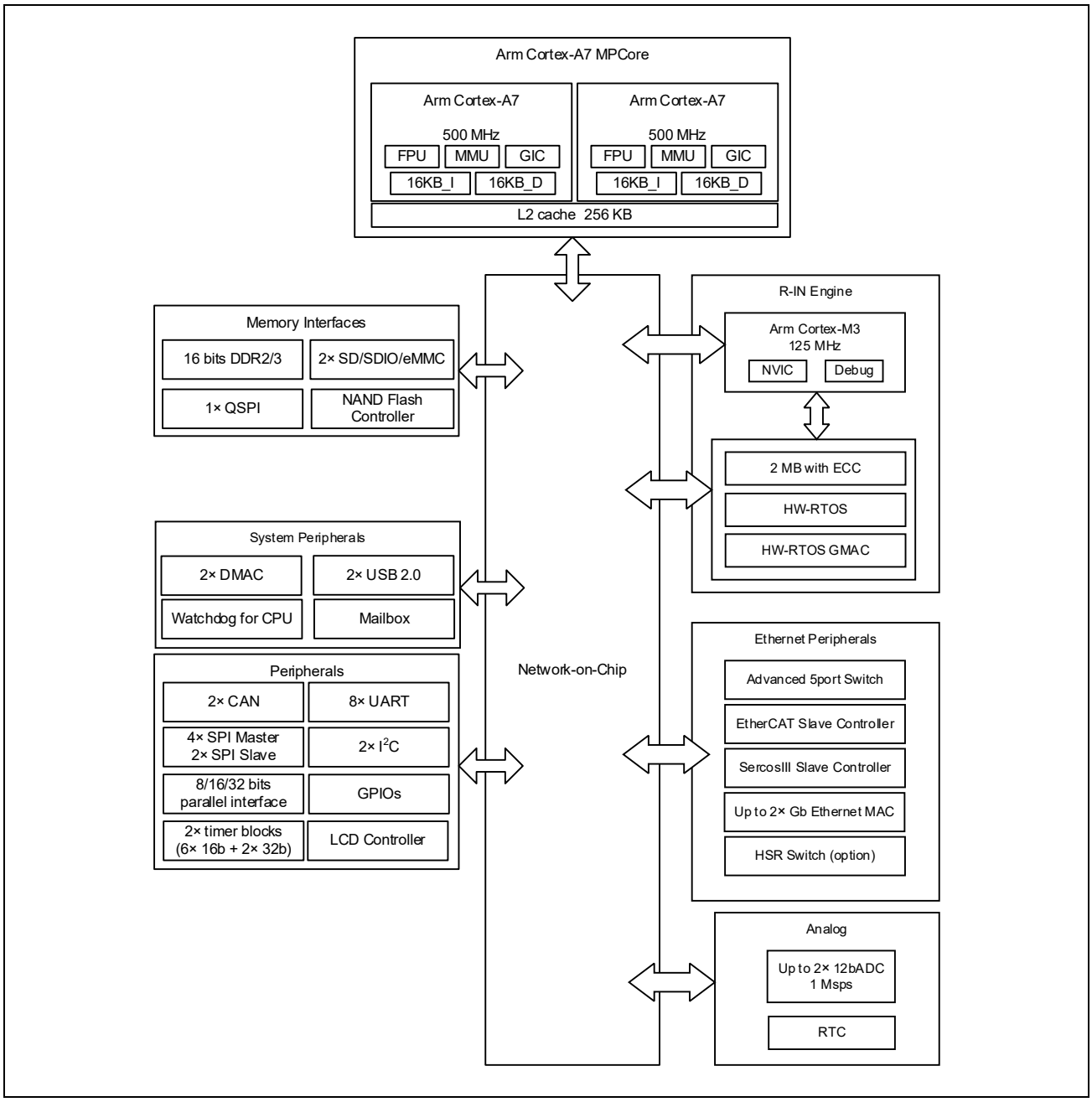


Figure 1.1 Block Diagram of RZ/N1D

1.2.3 RZ/N1L

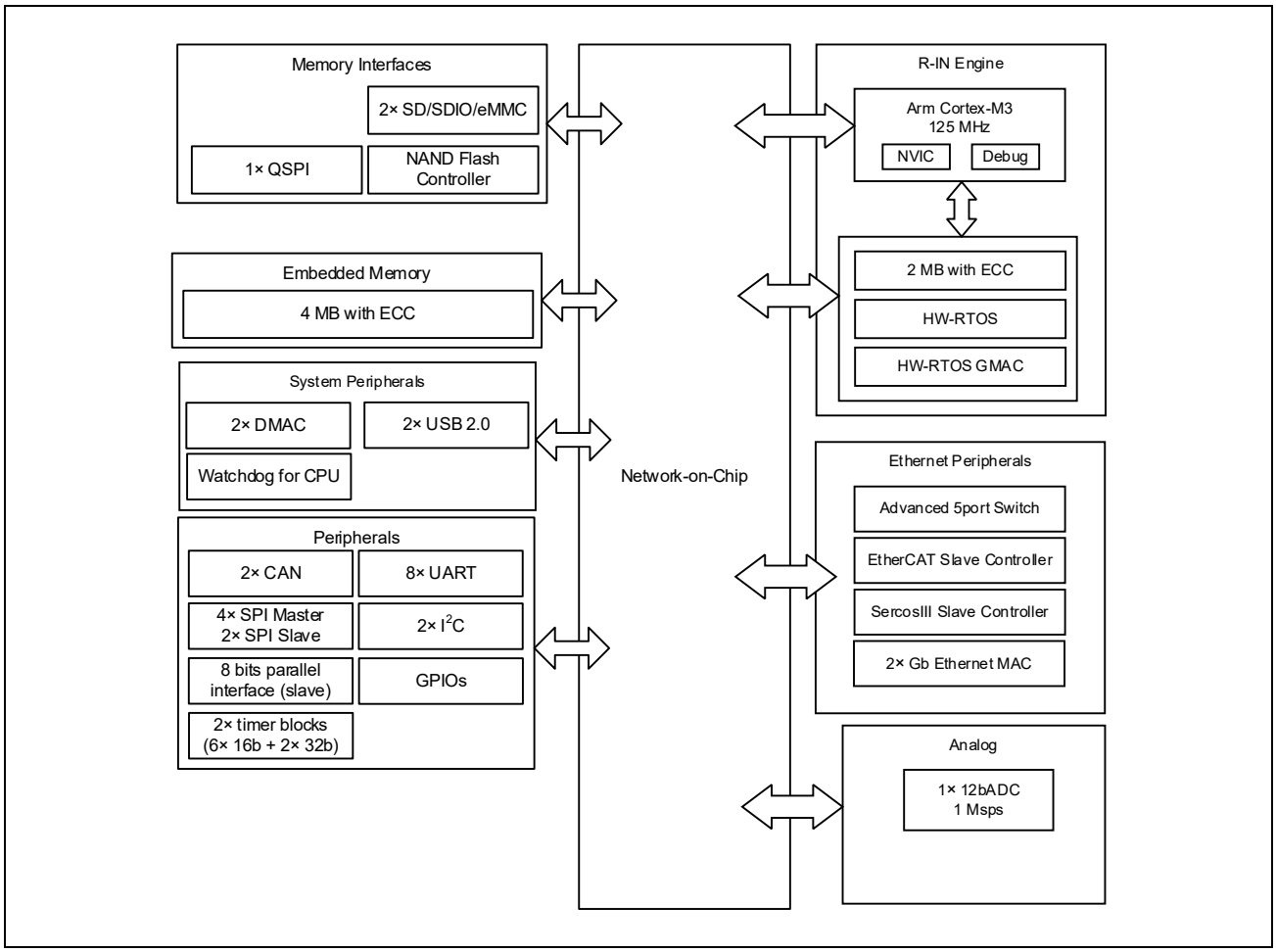


Figure 1.3 Block Diagram of RZ/N1L

Note 9. Shared with peripheral signals.

1.4 List of Products

Table 1.3 List of Products

Name	P/N	Package(s)	Main CPU	PRP/HSR
RZ/N1D	*1	400BGA	Dual Cortex-A7	—
	R9A06G032VGBA	324BGA		
	R9A06G032NGBG	400BGA	Dual Cortex-A7	PRP/HSR
RZ/N1S	R9A06G033VGBA	196BGA	Single Cortex-A7	—
	R9A06G033NGBG	324BGA	Single Cortex-A7	PRP
RZ/N1L	R9A06G034VGBA	196BGA	Cortex-M3	—

Note 1. Please contact local Renesas sales.

1.5 Pin Assignments

1.5.1 RZ/N1D BGA-400 Package

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
20	GND	GPIO75	GPIO77	GPIO36	GPIO37	GPIO42	GPIO48	GPIO53	GPIO54	GPIO59	GPIO12	GPIO18	GPIO20	GPIO62	GPIO63	GPIO90	GPIO88	GPIO86	GPIO84	GND	20
19	GPIO78	GPIO76	GPIO74	GPIO68	GPIO38	GPIO41	GPIO45	GPIO51	GPIO56	GPIO58	GPIO13	GPIO17	GPIO64	GPIO106	GPIO91	GPIO89	GPIO87	GPIO85	GPIO93	GPIO82	19
18	GPIO30	GPIO79	GPIO73	GPIO71	GPIO66	GPIO39	GPIO44	GPIO47	GPIO52	GPIO55	GPIO19	GPIO15	GPIO22	GPIO102	GPIO107	GPIO96	GPIO95	GPIO100	GPIO80	GPIO81	18
17	GPIO27	GPIO32	GPIO34	GPIO69	GPIO70	GPIO67	GPIO40	GPIO46	GPIO49	GPIO57	GPIO16	GPIO21	GPIO104	GPIO99	GPIO98	GPIO97	GPIO105	GPIO103	GPIO92	GPIO83	17
16	GPIO24	GPIO28	GPIO29	GPIO129	GPIO128	GPIO72	GPIO65	GPIO43	GPIO50	GND	GPIO14	GPIO23	GPIO108	GPIO101	VDD11_CA7	GPIO120	GPIO109	GPIO118	GPIO94	GPIO117	16
15	GPIO6	GPIO8	GPIO31	GPIO33	GPIO35	GND	GND	GND	RGMII5_VDDQ	RGMII5_VDDQ	GND	GND	VDD33	GND	VDD11_CA7	GPIO125	GPIO126	GPIO121	GPIO116	GPIO119	15
14	GPIO5	GPIO9	GPIO10	GPIO26	RGMII3_VDDQ	RGMII3_VDDQ	VDD33	RGMII4_VDDQ	RGMII4_VDDQ	GND	RGMII2_VDDQ	RGMII2_VDDQ	VDD33	GND	GPIO124	GPIO123	GPIO122	GPIO111	GPIO115	GPIO113	14
13	GPIO2	GPIO4	GPIO3	GPIO11	GPIO25	GND	VDD11	GND	VDD11	VDD11	GND	VDD11	GND	VDD33	GPIO127	JTAG_TDO	JTAG_TCK	GPIO114	GPIO112	GPIO110	13
12	GPIO0	GPIO131	GPIO1	GPIO7	RGMII1_VDDQ	GND	VDD11	GND	GND	GND	GND	GND	VDD11	VDD33	GND	JTAG_TRST_N	JTAG_TDI	JTAG_TMS	GPIO61	GPIO60	12
11	GPIO137	GPIO135	GPIO133	GPIO132	GPIO130	RGMII1_VDDQ	GND	GND	GND	GND	GND	GND	GND	USB_AVSS	USB_RREF	USB_AVDD	USB_VBUS	MRESET_N	MRESET_OUT	USB_GND	11
10	GPIO139	GPIO136	GPIO138	GPIO140	GPIO134	GND	VDD33	GND	GND	GND	GND	GND	VDD11	USB_AVSS	USB_GND	USB_GND	USB_GND	USB_GND	USB_DM1	USB_DP1	10
9	GPIO141	GPIO143	GPIO147	GPIO144	CTRSTBYB	VDD33	VDD33	VDD11	GND	GND	GND	GND	VDD11	GND	USB_VD33	USB_VD33	USB_GND	USB_GND	USB_DM2	USB_DP2	9
8	GPIO145	GPIO149	GPIO142	GPIO148	ANF_VDD_PRG	RTC_VDD33	GND	VDD11	VDD11	DVSS	DVDD	VDD11	GND	VDD33	ADC2_AGND	ADC2_AVDD	ADC2_IN6	ADC2_IN7	ADC2_IN8	USB_GND	8
7	RTC_XI	GPIO146	RTC_PWRGOOD	GPIO152	GPIO150	GND	VDD33	DVDDQ	GND	DVSS	DVDD	DVDDQ	VDD33	TMC2	THMODE	ADC2_VREFN	ADC2_VREFP	ADC2_IN3	ADC2_IN2	ADC2_IN4	7
6	RTC_XO	GPIO151	GPIO153	GPIO154	GPIO158	GND	VDD33	GND	DVDDQ	DVDDQ	DVDDQ	DVDDQ	GND	CONFIG1	CONFIG0	ADC1_AVDD	ADC1_VREFP	ADC1_IN8	ADC2_IN1	ADC2_IN0	6
5	GPIO155	GPIO157	GPIO159	GPIO163	GPIO162	DDR_DQ6	GND	GND	GND	DDR_VREF	GND	DDR_ADDR0	GND	DDR_ADDR5	CONFIG2	ADC1_AGND	ADC1_VREFN	ADC1_IN4	ADC1_IN6	ADC1_IN7	5
4	GPIO160	GPIO156	GPIO167	GPIO165	GND	DDR_DQ0	DDR_DQS_N0	DDR_DQ7	DDR_DQ5	DDR_MZQ	DDR_CS1	DDR_ADDR12	DDR_ADDR15	DDR_BA0	DDR_ADDR7	DDR_ADDR1	TMC1	ADC1_IN3	ADC1_IN0	ADC1_IN2	4
3	GPIO161	GPIO169	GPIO166	GND	DDR_DQ4	DDR_DQS0	DDR_DM0	DDR_DQ1	DDR_DQ3	GND	DDR_ADDR10	DDR_RAS	DDR_CAS	DDR_ADDR3	DDR_ADDR4	DDR_ADDR9	DDR_ADDR14	DDR_RESET_N	GND	ADC1_IN1	3
2	GPIO164	GPIO168	DDR_DQ14	DDR_DQ8	DDR_DQ2	DDR_DM1	DDR_DQS_N1	DDR_DQ9	DDR_DQ15	DDR_CLKP	DDR_CLKEN	DDR_WE	DDR_ODT0	DDR_BA2	DDR_ADDR2	DDR_ADDR11	DDR_ADDR13	GND	MCLK_XO	GND	2
1	GND	GND	DDR_DQ12	DDR_DQ10	GND	DDR_DQS1	GND	DDR_DQ11	DDR_DQ13	DDR_CLKN	GND	DDR_CS0	DDR_ODT1	DDR_BA1	GND	DDR_ADDR6	DDR_ADDR8	GND	MCLK_XI	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	

Figure 1.4 RZ/N1D Pinout BGA-400 (Top View)

1.5.2 RZ/N1D BGA-324 Package

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	
18	GND	GPIO75	GPIO77	GPIO36	GPIO41	GPIO42	GPIO46	GPIO48	GPIO51	GPIO54	GPIO64	GPIO101	GPIO107	GPIO90	GPIO88	GPIO86	GPIO84	GND	18
17	GPIO78	GPIO76	GPIO74	GPIO66	GPIO39	GPIO44	GPIO47	GPIO52	GPIO53	GPIO56	GPIO108	GPIO99	GPIO91	GPIO89	GPIO87	GPIO85	GPIO93	GPIO82	17
16	GPIO79	GPIO69	GPIO72	GPIO68	GPIO37	GPIO40	GPIO45	GPIO50	GPIO57	GPIO58	GPIO106	GPIO96	GPIO97	GPIO95	GPIO120	GPIO100	GPIO80	GPIO81	16
15	GPIO30	GPIO33	GPIO73	GPIO70	GPIO67	GPIO38	GPIO43	GPIO49	GPIO55	GPIO102	GPIO104	GPIO98	GPIO105	VDD11_CA7	GPIO125	GPIO103	GPIO92	GPIO83	15
14	GPIO35	GPIO28	GPIO31	GPIO128	GPIO71	GPIO65	RGMII4_VDDQ	GND	GPIO59	GPIO62	GPIO63	GPIO109	GND	VDD11_CA7	GPIO124	GPIO126	GPIO94	GPIO115	14
13	GPIO29	GPIO32	GPIO34	GPIO129	VDD33	GND	RGMII4_VDDQ	RGMII5_VDDQ	RGMII5_VDDQ	VDD33	VDD33	GND	GND	GPIO123	GPIO122	GPIO118	GPIO116	GPIO113	13
12	GPIO24	GPIO27	GPIO25	GPIO26	RGMII3_VDDQ	GND	VDD11	GND	GND	VDD11	GND	VDD11	VDD33	GPIO127	GPIO121	GPIO117	GPIO119	GPIO114	12
11	GPIO133	GPIO131	GPIO132	GPIO130	RGMII3_VDDQ	VDD33	GND	GND	GND	GND	GND	VDD11	VDD33	JTAG_TDO	JTAG_TDI	GPIO111	GPIO112	GPIO110	11
10	GPIO135	GPIO137	GPIO136	GPIO134	GND	VDD11	GND	GND	GND	GND	GND	USB_AVSS	GND	JTAG_TRST_N	JTAG_TMS	JTAG_TCK	GPIO61	GPIO60	10
9	GPIO139	GPIO138	GPIO147	GPIO142	VDD33	VDD33	GND	GND	GND	GND	GND	USB_AVSS	USB_RREF	USB_AVDD	USB_VBUS	MRESET_N	MRESET_OUT	USB_GND	9
8	GPIO141	GPIO143	GPIO140	GPIO146	ANF_VDD_PRG	VDD33	GND	GND	DVSS	DVDD	VDD11	USB_VD33	USB_VD33	USB_GND	USB_GND	USB_GND	USB_DM1	USB_DP1	8
7	GPIO145	GPIO149	GPIO144	CTRSTBYB	RTC_VDD33	VDD11	GND	DVDDQ	DVSS	DVDD	VDD11	GND	VDD33	CONFIG0	USB_GND	USB_GND	USB_DM2	USB_DP2	7
6	RTC_XI	GPIO148	GPIO150	RTC_PWRGOOD	GND	VDD33	VDD11	DVDDQ	DVDDQ	DVDDQ	DVDDQ	VDD33	TMC2	ADC1_AVDD	ADC1_VREFP	ADC1_IN6	ADC1_IN8	USB_GND	6
5	RTC_XO	GPIO151	GPIO154	GND	DDR_DQ6	GND	GND	GND	DDR_VREF	DDR_ADDR0	GND	THMODE	TMC1	CONFIG2	ADC1_AGND	ADC1_VREFN	ADC1_IN4	ADC1_IN7	5
4	GPIO152	GPIO153	GND	DDR_DQ0	DDR_DQS0	DDR_DQ1	DDR_DQ7	DDR_MZQ	GND	DDR_ADDR12	DDR_BA0	DDR_ADDR5	DDR_ADDR7	DDR_ADDR1	CONFIG1	ADC1_IN1	ADC1_IN2	ADC1_IN0	4
3	GPIO155	DDR_DQ14	DDR_DQ4	DDR_DQS_N0	DDR_DM0	DDR_DQ3	DDR_DQ5	GND	DDR_ADDR10	DDR_RAS	DDR_ADDR15	DDR_ADDR3	DDR_ADDR4	DDR_ADDR9	DDR_ADDR14	DDR_RESET_N	GND	ADC1_IN3	3
2	DDR_DQ12	DDR_DQ10	DDR_DQ2	DDR_DM1	DDR_DQS_N1	DDR_DQ9	DDR_DQ15	DDR_CLKP	DDR_CLKEN	DDR_WE	DDR_CAS	DDR_BA2	DDR_ADDR2	DDR_ADDR11	DDR_ADDR13	GND	MCLK_XO	GND	2
1	GND	DDR_DQ8	GND	DDR_DQS1	GND	DDR_DQ11	DDR_DQ13	DDR_CLKN	GND	DDR_CS0	DDR_ODT0	DDR_BA1	GND	DDR_ADDR6	DDR_ADDR8	GND	MCLK_XI	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	

Figure 1.5 RZ/N1D Pinout BGA-324 (Top View)

1.5.3 RZ/N1S BGA-324 Package

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	
18	GND	GPIO69	GND	GPIO48	GPIO55	GPIO59	GPIO12	GPIO17	GPIO20	GND	GPIO0	GPIO2	GPIO6	GND	GPIO88	GPIO86	GPIO84	GND	18
17	GPIO67	GPIO68	GPIO70	GPIO50	GPIO51	GPIO57	GND	GPIO14	GPIO19	GPIO21	GPIO1	GPIO3	GPIO8	GPIO90	GPIO89	GPIO87	GPIO85	GPIO93	17
16	GPIO66	GPIO65	GPIO64	GPIO71	GPIO53	GPIO49	GPIO56	GPIO13	GPIO18	GPIO23	GPIO5	GPIO7	GPIO9	GPIO153	GPIO91	GPIO81	GPIO82	GPIO80	16
15	GND	GPIO62	GPIO63	GPIO72	GPIO52	GPIO54	GPIO58	GPIO15	GPIO16	GPIO22	GPIO4	GPIO11	GPIO10	GPIO154	GPIO152	GPIO151	GPIO92	GND	15
14	GPIO43	GPIO45	GPIO46	GPIO73	VDD33	VDD33	RGMII5 _VDDQ	RGMII5 _VDDQ	RGMII2 _VDDQ	RGMII2 _VDDQ	RGMII1 _VDDQ	RGMII1 _VDDQ	VDD33	GPIO155	GPIO157	GPIO150	GPIO83	GPIO94	14
13	GPIO38	GPIO39	GPIO44	GPIO47	GND	GND	GND	GND	GND	GND	GND	GND	VDD33	GPIO156	GPIO158	GPIO159	MRESET _OUT	GND	13
12	GPIO36	GPIO37	GPIO41	GPIO42	RGMII4 _VDDQ	GND	VDD11	VDD11	VDD11	VDD11	VDD11	VDD11	GND	GND	GND	MRESET _N	MCLK _XO	MCLK _XI	12
11	GND	GPIO34	GPIO33	GPIO40	RGMII4 _VDDQ	GND	VDD11	GND	GND	GND	GND	VDD11	PLL _AVDD	GND	GND	USB _VBUS	USB _GND	USB _GND	11
10	GPIO32	GPIO35	GPIO31	GPIO30	RGMII3 _VDDQ	GND	VDD11	GND	GND	GND	GND	VDD11	PLL _AGND	USB _AVDD	USB _RREF	USB _GND	USB _DM1	USB _DP1	10
9	GPIO28	GPIO27	GPIO29	GPIO25	RGMII3 _VDDQ	GND	VDD11	GND	GND	GND	GND	VDD11	VDD33	USB _VD33	USB _VD33	USB _GND	USB _DM2	USB _DP2	9
8	GPIO24	GPIO26	GPIO77	GND	GND	VDD33	VDD11	GND	GND	GND	GND	VDD11	GND	ADC1 _AVDD	ADC1 _VREFN	ADC1 _IN7	USB _GND	USB _GND	8
7	GND	GPIO79	GPIO76	GPIO74	GND	VDD33	VDD11	VDD11	VDD11	VDD11	VDD11	VDD11	GND	ADC1 _AGND	ADC1 _VREFP	ADC1 _IN2	ADC1 _IN8	ADC1 _IN6	7
6	GPIO61	GPIO78	GPIO75	GPIO133	GND	VDD33	GND	GND	GND	GND	GND	GND	GND	VDD33	TMC2	ADC1 _IN0	ADC1 _IN1	ADC1 _IN3	6
5	GPIO60	VDD33	GPIO149	RTC _VDD33	GND	GND	VDD33	VDD33	VDD33	GND	GND	GND	VDD33	VDD33	JTAG _TRST_N	JTAG _TDI	JTAG _TMS	ADC1 _IN4	5
4	GND	ANF_VDD _PRG	RTC_PWR GOOD	GPIO123	GPIO125	GPIO127	GPIO129	GPIO130	GPIO131	GPIO132	GPIO134	GPIO136	CTRSTBY B	CONFIG1	TMC1	JTAG _TCK	GPIO148	GND	4
3	RTC_XO	GPIO120	GPIO121	GPIO122	GPIO124	GPIO126	GPIO128	GPIO106	GPIO109	GPIO112	GPIO114	GPIO135	THMODE	CONFIG0	JTAG_TD O	GPIO145	GPIO146	GPIO147	3
2	RTC_XI	GPIO119	GPIO97	GPIO98	GPIO100	GPIO102	GPIO104	GPIO105	GPIO108	GPIO111	GPIO113	GPIO116	GPIO137	GPIO138	GPIO139	GPIO142	GPIO143	GPIO144	2
1	GND	GPIO95	GPIO96	GND	GPIO99	GPIO101	GPIO103	GND	GPIO107	GPIO110	GND	GPIO115	GPIO117	GPIO118	GND	GPIO140	GPIO141	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	

Figure 1.6 RZ/N1S Pinout BGA-324 (Top View)

1.5.4 RZ/N1S BGA-196 Package

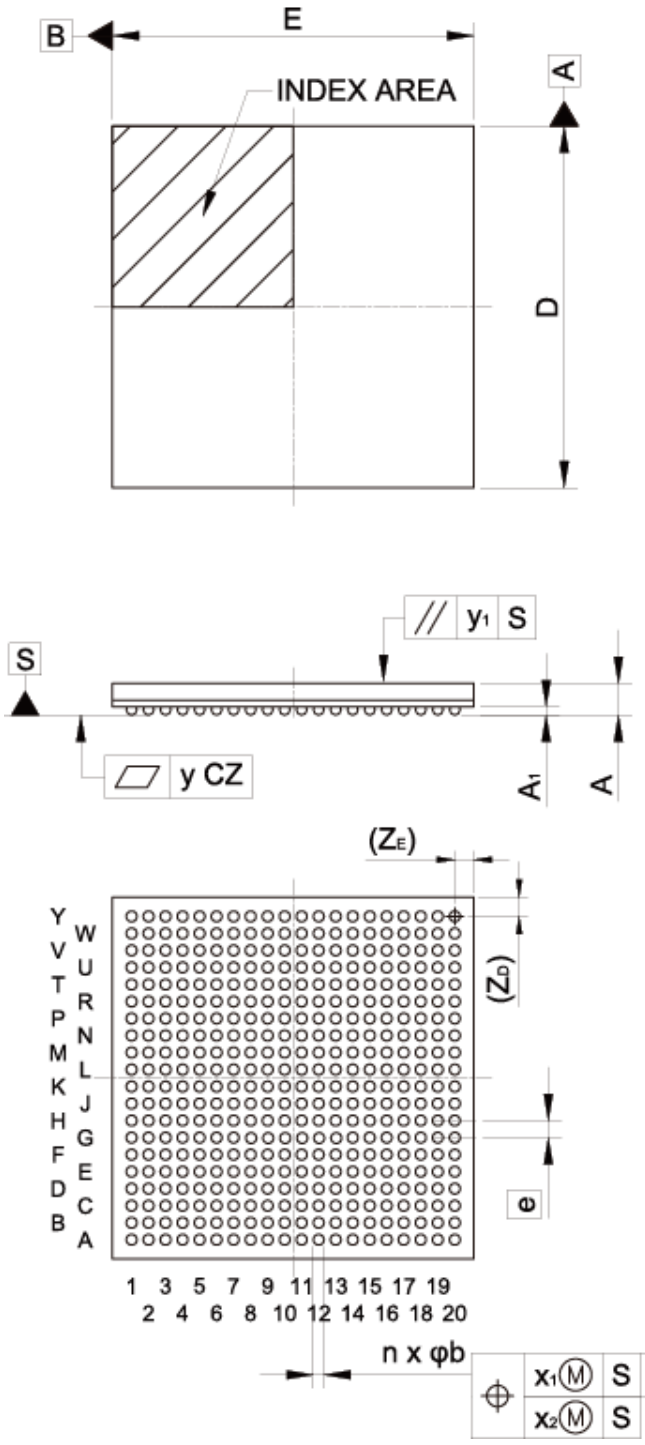
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14	GND	GPIO70	GND	GPIO48	GPIO51	GPIO57	GND	GPIO3	GPIO7	GPIO8	GND	GPIO89	GPIO87	GND	14
13	GPIO64	GPIO68	GPIO71	GPIO50	GPIO49	GPIO56	GPIO0	GPIO2	GPIO6	GPIO90	GPIO86	GPIO84	GPIO81	GPIO93	13
12	GPIO63	GPIO67	GPIO72	GPIO52	GPIO54	GPIO58	GPIO1	GPIO5	GPIO9	GPIO88	GPIO91	GPIO82	GPIO80	GPIO83	12
11	GPIO66	GPIO65	GPIO69	GPIO53	GPIO55	GPIO59	GPIO4	GPIO11	GPIO10	VDD33	GPIO85	GPIO92	GPIO94	GND	11
10	GND	GPIO45	GPIO62	GPIO73	VDD33	RGMII5_VDDQ	RGMII5_VDDQ	RGMII1_VDDQ	RGMII1_VDDQ	GND	VDD11	MRESET_OUT	MCLK_XO	MCLK_XI	10
9	GPIO47	GPIO43	GPIO42	GPIO44	VDD11	GND	VDD11	GND	VDD11	PLL_AVDD	PLL_AGND	MRESET_N	USB_VBUS	USB_GND	9
8	GPIO46	GPIO39	GPIO38	GPIO41	RGMII4_VDDQ	GND	GND	GND	GND	USB_AVDD	USB_RREF	USB_GND	USB_DM1	USB_DP1	8
7	GND	GPIO36	GPIO37	GPIO40	RGMII4_VDDQ	VDD11	GND	GND	VDD11	USB_VD33	USB_VD33	USB_GND	USB_DM2	USB_DP2	7
6	GPIO61	GPIO77	GPIO79	GPIO76	VDD33	GND	GND	GND	GND	GND	ADC1_AVDD	ADC1_VREFN	USB_GND	USB_GND	6
5	GPIO60	GPIO75	GPIO78	GPIO74	VDD11	GND	VDD11	VDD11	GND	VDD11	ADC1_AGND	ADC1_VREFP	ADC1_IN8	ADC1_IN7	5
4	GND	RTC_VDD33	VDD33	ANF_VDD_PRG	VDD33	GPIO105	GPIO107	GPIO112	VDD33	VDD33	TMC2	ADC1_IN2	ADC1_IN0	ADC1_IN6	4
3	RTC_XO	RTC_PWRGOOD	GPIO97	GPIO95	GPIO100	GPIO103	GPIO111	GPIO115	GPIO117	CTRSTBYB	CONFIG1	TMC1	ADC1_IN4	ADC1_IN3	3
2	RTC_XI	GPIO98	GPIO96	GPIO102	GPIO104	GPIO108	GPIO110	GPIO114	GPIO116	THMODE	CONFIG0	JTAG_TCK	JTAG_TMS	ADC1_IN1	2
1	GND	GPIO99	GPIO101	GND	GPIO106	GPIO109	GND	GPIO113	GPIO118	GND	JTAG_TDO	JTAG_TRST_N	JTAG_TDI	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

Figure 1.7 RZ/N1S Pinout BGA-196 (Top View)

1.6 Package Dimensions

1.6.1 BGA-400 Package

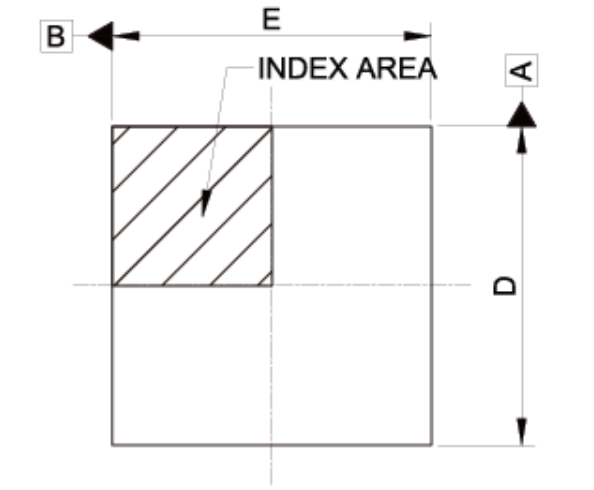
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA400-17x17-0.80	PLBG0400GB-A	0.88

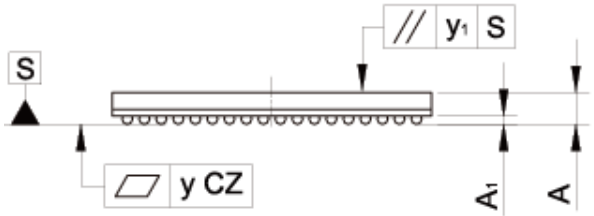


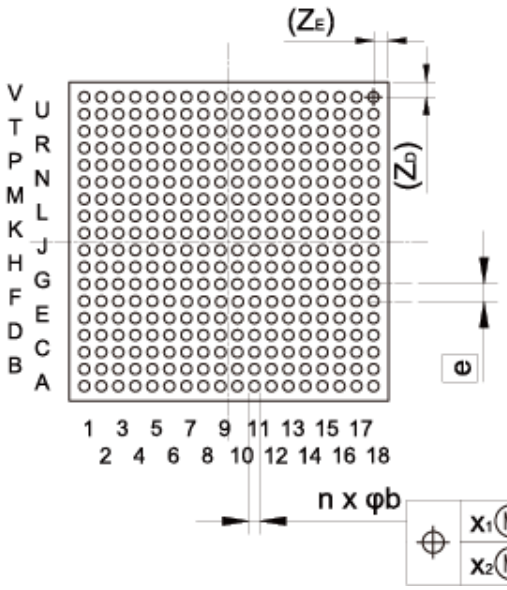
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	16.90	17.00	17.10
E	16.90	17.00	17.10
A	—	—	1.70
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x_1	—	—	0.15
x_2	—	—	0.08
y	—	—	0.10
y_1	—	—	0.20
n	—	400	—
Z_D	—	0.90	—
Z_E	—	0.90	—

1.6.2 BGA-324 Package

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA324-15x15-0.80	PLBG0324GA-A	0.70







Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	14.90	15.00	15.10
E	14.90	15.00	15.10
A	—	—	1.70
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x_1	—	—	0.15
x_2	—	—	0.08
y	—	—	0.10
y_1	—	—	0.20
n	—	324	—
Z_D	—	0.70	—
Z_E	—	0.70	—

REVISION HISTORY	RZ/N1D Group, RZ/N1S Group, RZ/N1L Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.50	Mar 13, 2017	—	First Edition issued
0.80	Oct 31, 2017	1	Features, revised
		2	1.1, Table 1.1 (1/9), modified
		3	1.1, Table 1.1 (2/9): General Purpose I/O Ports → IO Multiplexing, modified. IO Multiplexing: Locations of IOs for Peripherals are selectable, added. DDR2/3 Controller: Description, modified.
		4	1,1, Table 1.1 (3/9): SD/SDIO/eMMC: Normal mode → Default mode, revised
		8	1.1, Table 1.1 (7/9): SPI Master: ssi_clk → SPI_SCLK, corrected. SPI Slave: DMA Transmit and Receive transfer enabling by external event (rising or falling edge), deleted. CAN: 2× triggers, deleted.
		9	1.1, Table 1.1 (8/9), modified
		11 to 13	1.2, Figure 1.1, 1.2, and 1.3, corrected
		14	1.3, corrected and modified
		15	1.4, modified
		16	1.5.1, VDD11 (R15 and R16) → VDD11_CA7
		17	1.5.2, VDD11 (P14 and P15) → VDD11_CA7
		16 and 17	1.5.1 and 1.5.2, TDO → JTAG_TDO, TCK → JTAG_TCK, TRST_N → JTAG_TRST_N, TDI → JTAG_TDI, TMS → JTAG_TMS, USB_AGND → USB_AVSS, USB_VDD33 → USB_VD33, DGND → DVSS, XTAL → MCLK_XO, EXTAL → MCLK_XI
		20	1.5.5, RTC_VDD33 → VDD33, RTC_PWRGOOD → VDD33, RTC_XO → N.C., RTC_XI → GND, ANF_VDD_33V → VDD33, ANF_VDD_PRG → GND
0.90	Dec 28, 2017	1, 7	Features and 1.1 add trademarks
		1, 2, 9, 11 to 14	Features, 1.1, 1.2, and 1.3, ARM → Arm, changed
		1	Features, Low Power Features: revised. Advanced real-time Ethernet features: Advanced 5 (4 + 1) Port Switch (A5PSW): Optional bypass switch, deleted
		2	1.1, Table 1.1 (1/9): Cortex-A7: Dynamic frequency → Clock frequency scaling, changed. Cortex-A7 and Cortex-M3: Unaligned memory access supported, deleted
		3	1.1, Table 1.1 (2/9): DMAC: Undirectional transfer supported, deleted
		3	1.1, Table 1.1 (2/9): MSEBI: Address/data/control-data are multiplexed on data bus, added
		3	1.1, Table 1.1 (2/9): DDR2/3 Controller: Programmable output slope in DDR2/3 and configurable on die termination → Programmable on die termination, modified.
		4	1.1, Table 1.1 (3/9): QSPI: revised
		4	1.1, Table 1.1 (3/9): SD/SDIO/eMMC: Designed to work with I/O cards, read-only cards, and read/write cards, Variable-length data transfers, Password protection of cards, deleted
		7	1.1, Table 1.1 (6/9): USB2.0 HOST: 1 dedicated port → 1 dedicated port + 1 configurable port (Host or Function), revised
		7	1.1, Table 1.1 (6/9): UART 4, 5, 6, 7, 8: Same as UART 1, 2, 3 with following features → In addition to UART 1, 2, 3, the following function is available, modified
		8	1.1, Table 1.1 (7/9): SPI 1, 2, 3, 4: Programmable RXD sampling logic with RXD sampling delays of up to 64 SPI_SCLK cycles → Programmable RXD sampling logic, modified
		8	1.1, Table 1.1 (7/9): I^2C 1, 2: Handles bit and byte waiting at all bus speeds, deleted
		9	1.1, Table 1.1 (8/9): LCD Controller: description about resolutions, revised
		9	1.1, Table 1.1 (8/9): Clock Monitoring: from the PLL circuit or low speed on-chip oscillator → from the PLL circuit or on-chip oscillator, modified
		11	1.2, description, added
		11 to 13	1.2, Figure 1.1 to 1.3, modified
		16 to 19	1.5.1 to 1.5.4, ANF_VDD_33V → VDD33, modified

All trademarks and registered trademarks are the property of their respective owners.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other disputes involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawing, chart, program, algorithm, application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics products.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (space and undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. When using the Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat radiation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions or failure or accident arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please ensure to implement safety measures to guard them against the possibility of bodily injury, injury or damage caused by fire, and social damage in the event of failure or malfunction of Renesas Electronics products, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures by your own responsibility as warranty for your products/system. Because the evaluation of microcomputer software alone is very difficult and not practical, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please investigate applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive carefully and sufficiently and use Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall not use Renesas Electronics products or technologies for (1) any purpose relating to the development, design, manufacture, use, stockpiling, etc., of weapons of mass destruction, such as nuclear weapons, chemical weapons, or biological weapons, or missiles (including unmanned aerial vehicles (UAVs)) for delivering such weapons, (2) any purpose relating to the development, design, manufacture, or use of conventional weapons, or (3) any other purpose of disturbing international peace and security, and you shall not sell, export, lease, transfer, or release Renesas Electronics products or technologies to any third party whether directly or indirectly with knowledge or reason to know that the third party or any other party will engage in the activities described above. When exporting, selling, transferring, etc., Renesas Electronics products or technologies, you shall comply with any applicable export control laws and regulations promulgated and administered by the governments of the countries asserting jurisdiction over the parties or transactions.
10. Please acknowledge and agree that you shall bear all the losses and damages which are incurred from the misuse or violation of the terms and conditions described in this document, including this notice, and hold Renesas Electronics harmless, if such misuse or violation results from your resale or making Renesas Electronics products available any third party.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.3.0-1 November 2016)

RENESAS

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

© 2017 Renesas Electronics Corporation. All rights reserved.

Colophon 6.0