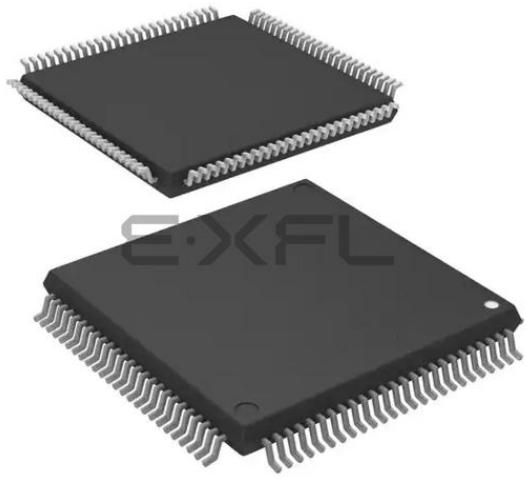
Renesas Electronics America Inc - R5F72433D100FP#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH2A
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	SCI
Peripherals	DMA, PWM, WDT
Number of I/O	63
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f72433d100fp-u0

Classification	Symbol	I/O	Name	Function
Interrupts	NMI	Input	Non-maskable interrupt	Non-maskable interrupt request pin. Fix it high when not in use.
	IRQ7 to IRQ0	Input	Interrupt requests 7 to 0	Maskable interrupt request pins. Level-input or edge-input detection can be selected. When the edge-input detection is selected, the rising edge, falling edge, or both edges can also be selected.
	$\overline{\text{IRQOUT}}$	Output	Interrupt request output	Indicates that an interrupt has occurred, enabling external devices to be informed of an interrupt occurrence even while the bus mastership is released.
Address bus	A25 to A0	Output	Address bus	Outputs addresses. (A25 to A21 are available only in the SH7286.)
Data bus	D31 to D0	I/O	Data bus	Bidirectional data bus. (D31 to D16 are available only in the SH7286.)
Bus control	$\overline{\text{CS7}}$ to $\overline{\text{CS0}}$	Output	Chip select 7 to 0	Chip-select signals for external memory or devices.
	$\overline{\text{RD}}$	Output	Read	Indicates that data is read from an external device.
	RD/$\overline{\text{WR}}$	Output	Read/write	Read/write signal.
	$\overline{\text{BS}}$	Output	Bus start	Bus-cycle start signal.
	$\overline{\text{AH}}$	Output	Address hold	Address hold timing signal for the device that uses the address/data-multiplexed bus.
	$\overline{\text{FRAME}}$	Output	Frame signal	In burst MPX-I/O interface mode, negated before the last bus cycle to indicate that the next bus cycle is the last access (only in SH7286)
	$\overline{\text{WAIT}}$	Input	Wait	Input signal for inserting a wait cycle into the bus cycles during access to the external space.
	$\overline{\text{WRHH}}$	Output	Write to HH byte	Indicates a write access to bits 31 to 24 of data of external memory or device (only in SH7286).
	$\overline{\text{WRHL}}$	Output	Write to HL byte	Indicates a write access to bits 23 to 16 of data of external memory or device (only in SH7286).

7.3.9 Break Bus Cycle Register_2 (BBR_2)

BBR_2 is a 16-bit readable/writable register, which specifies (1) disabling or enabling of user break interrupts, (2) including or excluding of the data bus value, (3) bus master of the I bus, (4) C bus cycle or I bus cycle, (5) instruction fetch or data access, (6) read or write, and (7) operand size as the break conditions of channel 2. BBR_2 is initialized to H'0000 by a power-on reset, but retains its previous value by a manual reset or in software standby mode or sleep mode.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	UBID2	-	-	CP2[2:0]			CD2[1:0]		ID2[1:0]		RW2[1:0]		SZ2[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	UBID2	0	R/W	User Break Interrupt Disable 2 Disables or enables user break interrupt requests when a channel-2 break condition is satisfied. 0: User break interrupt requests enabled 1: User break interrupt requests disabled
12, 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 8	CP2[2:0]	000	R/W	I-Bus Bus Master Select 2 Select the bus master when the bus cycle of the channel-2 break condition is the I bus cycle. However, when the C bus cycle is selected, this bit is invalidated (only the CPU cycle). xx1: CPU cycle is included in break conditions x1x: DMAC cycle is included in break conditions 1xx: DTC cycle is included in break conditions

Section 9 Bus State Controller (BSC)

The bus state controller (BSC) outputs control signals for various types of memory that is connected to the external address space and external devices. BSC functions enable this LSI to connect directly with SRAM, SDRAM, and other memory storage devices, and external devices.

9.1 Features

The BSC has the following features.

1. External address space
   - A maximum of 64 Mbytes for each of areas CS0 to CS7.
   - Can specify the normal space interface, SRAM interface with byte selection, burst ROM (clock synchronous or asynchronous), MPX-I/O, and SDRAM for each address space.
   - Can select the data bus width (8, 16, or 32 bits) for each address space.
   - Controls insertion of wait cycles for each address space.
   - Controls insertion of wait cycles for each read access and write access.
   - Can set independent idle cycles during the continuous access for five cases: read-write (in same space/different spaces), read-read (in same space/different spaces), the first cycle is a write access.
2. Normal space interface
   - Supports the interface that can directly connect to the SRAM.
3. Burst ROM interface (clock asynchronous)
   - High-speed access to the ROM that has the page mode function.
4. MPX-I/O interface
   - Can directly connect to a peripheral LSI that needs an address/data multiplexing.
5. SDRAM interface
   - Can set the SDRAM in up to two areas.
   - Multiplex output for row address/column address.
   - Efficient access by single read/single write.
   - High-speed access in bank-active mode.
   - Supports an auto-refresh and self-refresh.
   - Supports low-frequency and power-down modes.
   - Issues MRS and EMRS commands.

Table 9.2 Address Map in On-Chip ROM-Enabled Mode

Address	Space	Memory to be Connected	Size
H'0000 0000 to H'000F FFFF	On-chip ROM	On-chip ROM	256 Kbytes (SH7243) 768 Kbytes (SH7285) 1 Mbytes (SH7286)
H'0070 0000 to H'01FF FFFF	Other	Reserved area	—
H'0200 0000 to H'03FF FFFF	CS0	Normal space, SRAM with byte selection, burst ROM (asynchronous or synchronous)	32 Mbytes
H'0400 0000 to H'07FF FFFF	CS1	Normal space, SRAM with byte selection	64 Mbytes
H'0800 0000 to H'0BFF FFFF	CS2	Normal space, SRAM with byte selection, SDRAM	64 Mbytes
H'0C00 0000 to H'0FFF FFFF	CS3	Normal space, SRAM with byte selection, SDRAM	64 Mbytes
H'1000 0000 to H'13FF FFFF	CS4	Normal space, SRAM with byte selection, burst ROM (asynchronous)	64 Mbytes
H'1400 0000 to H'17FF FFFF	CS5	Normal space, SRAM with byte selection, MPX-I/O	64 Mbytes
H'1800 0000 to H'1BFF FFFF	CS6	Normal space, SRAM with byte selection	64 Mbytes
H'1C00 0000 to H'1FFF FFFF	CS7	Normal space, SRAM with byte selection	64 Mbytes
H'2000 0000 to H'FFF7 FFFF	Other	Reserved area	—
H'FFF8 0000 to H'FFFB FFFF	Other	On-chip RAM, reserved area*	—
H'FFFC 0000 to H'FFFF FFFF	Other	On-chip peripheral modules, reserved area*	—

Note: * For the on-chip RAM space, access the addresses shown in section 27, On-Chip RAM. For the on-chip peripheral module space, access the addresses shown in section 30, List of Registers. Do not access addresses which are not described in these sections. Otherwise, the correct operation cannot be guaranteed.

9.4.1 Common Control Register (CMNCR)

CMNCR is a 32-bit register that controls the common items for each area. This register is initialized to H'00001010 by a power-on reset and retains the value by a manual reset and in software standby mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	BLOCK	DPRTY[1:0]		DMAIW[2:0]			DMA IWA	-	-	HIZ CKIO	HIZ MEM	HIZ CNT
Initial value:	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
11	BLOCK	0	R/W	Bus Lock Specifies whether or not the $\overline{\text{BREQ}}$ signal is received. 0: Receives $\overline{\text{BREQ}}$. 1: Does not receive $\overline{\text{BREQ}}$.
10, 9	DPRTY[1:0]	00	R/W	DMA Burst Transfer Priority Specify the priority for a refresh request/bus mastership request during DMA burst transfer. 00: Accepts a refresh request and bus mastership request during DMA burst transfer. 01: Accepts a refresh request but does not accept a bus mastership request during DMA burst transfer. 10: Accepts neither a refresh request nor a bus mastership request during DMA burst transfer. 11: Reserved (setting prohibited)

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	TTSE	0	R/W	Timing Select E Specifies the timing for transferring data from TGRF_0 to TGRE_0 when they are used together for buffer operation. In channels 3 and 4, bit 2 is reserved. It is always read as 0 and the write value should always be 0. When channel 0 is used in a mode other than PWM mode, do not set this bit to 1. 0: When compare match E occurs in channel 0 1: When TCNT_0 is cleared
1	TTSB	0	R/W	Timing Select B Specifies the timing for transferring data from TGRD to TGRB in each channel when they are used together for buffer operation. When the channel is used in a mode other than PWM mode, do not set this bit to 1. 0: When compare match B occurs in each channel 1: When TCNT is cleared in each channel
0	TTSA	0	R/W	Timing Select A Specifies the timing for transferring data from TGRC to TGRA in each channel when they are used together for buffer operation. When the channel is used in a mode other than PWM mode, do not set this bit to 1. 0: When compare match A occurs in each channel 1: When TCNT is cleared in each channel

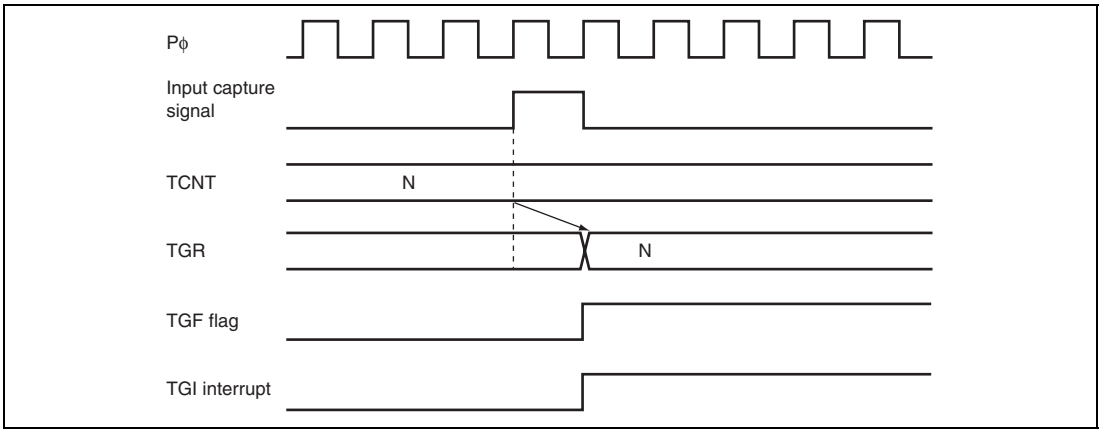


Figure 11.112 TGI Interrupt Timing (Input Capture) (Channel 5)

(3) TCFV Flag/TCFU Flag Setting Timing

Figure 11.113 shows the timing for setting of the TCFV flag in TSR on overflow, and TCIV interrupt request signal timing.

Figure 11.114 shows the timing for setting of the TCFU flag in TSR on underflow, and TCIU interrupt request signal timing.

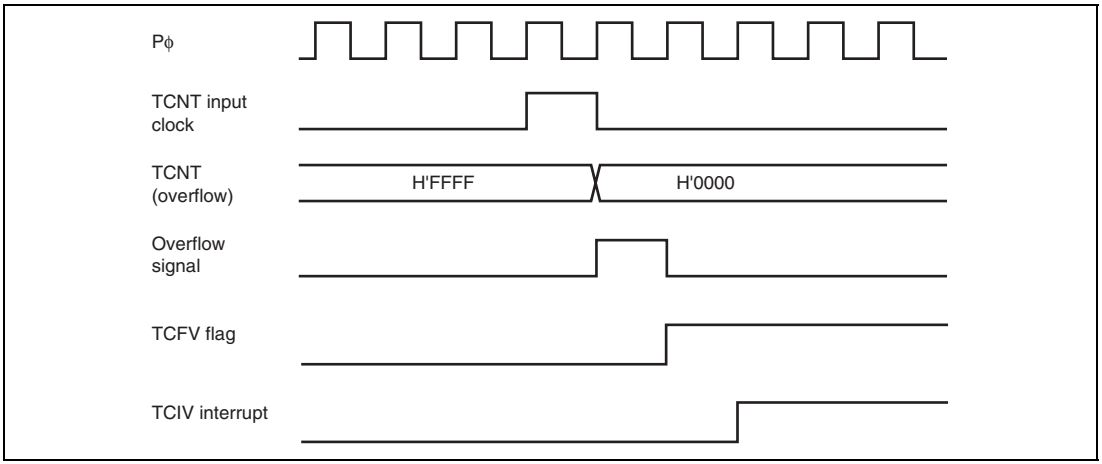


Figure 11.113 TCIV Interrupt Setting Timing

11.7.10 Contention between TGR Write and Input Capture

If an input capture signal is generated in the T2 state of a TGR write cycle, the input capture operation takes precedence and the write to TGR is not performed for channels 0 to 4. For channel 5, write to TGR is performed and the input capture signal is generated.

Figures 11.128 and 129 show the timing in this case.

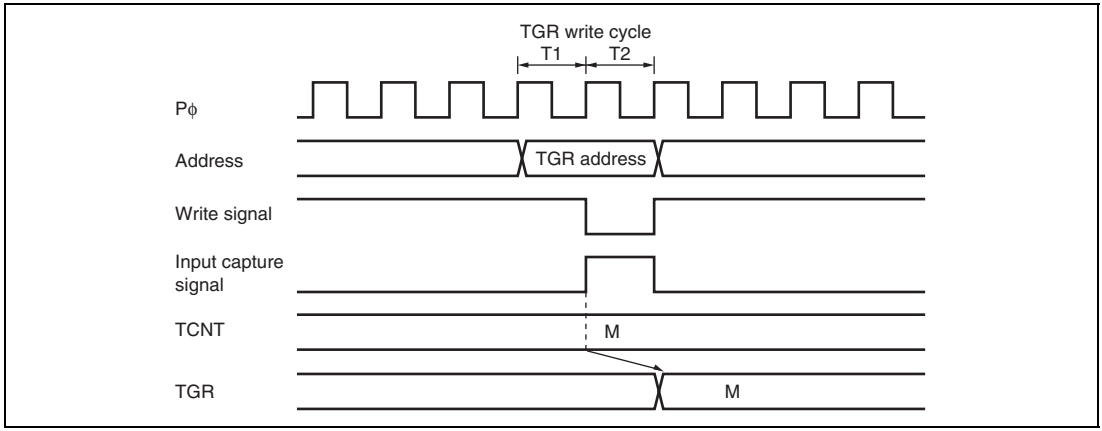


Figure 11.128 Contention between TGR Write and Input Capture (Channels 0 to 4)

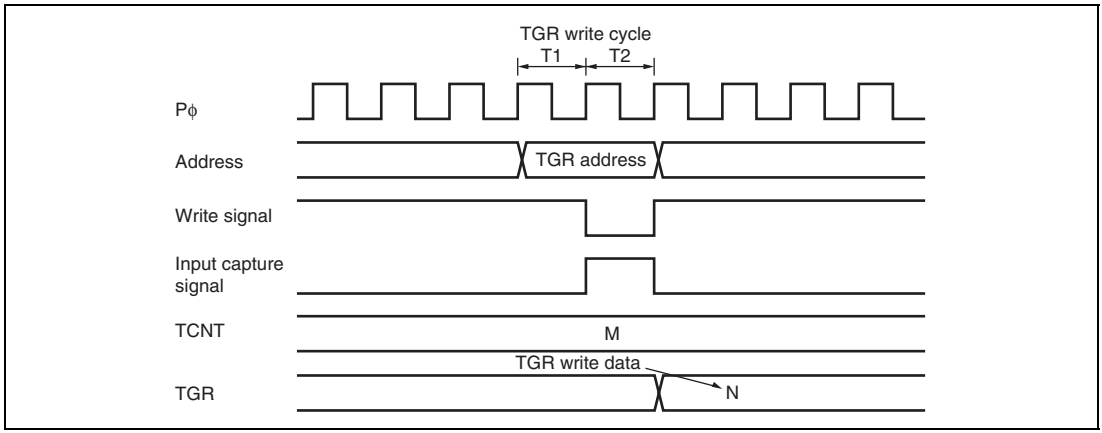


Figure 11.129 Contention between TGR Write and Input Capture (Channel 5)

(12) Operation when Error Occurs during PWM Mode 1 Operation, and Operation is Restarted in Reset-Synchronized PWM Mode

Figure 11.150 shows an explanatory diagram of the case where an error occurs in PWM mode 1 and operation is restarted in reset-synchronized PWM mode after re-setting.

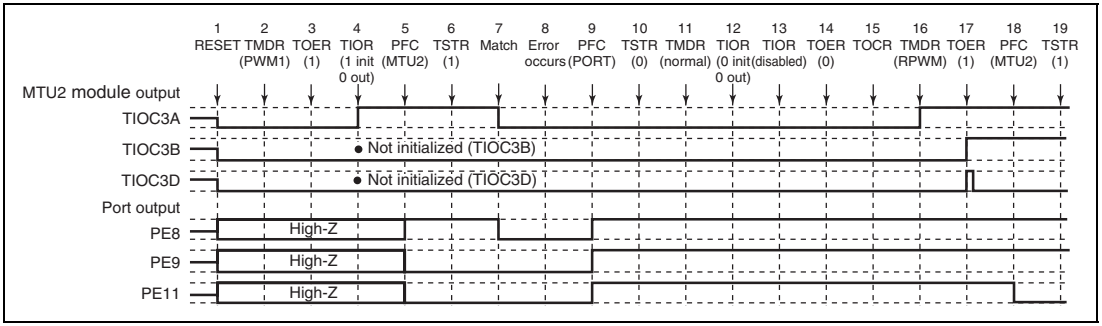


Figure 11.150 Error Occurrence in PWM Mode 1, Recovery in Reset-Synchronized PWM Mode

1 to 14 are the same as in figure 11.149.

15. Select the reset-synchronized PWM output level and cyclic output enabling/disabling with TOCR.
16. Set reset-synchronized PWM.
17. Enable channel 3 and 4 output with TOER.
18. Set MTU2 output with the PFC.
19. Operation is restarted by TSTR.

Item	Channel 3	Channel 4	Channel 5
A/D converter start request delaying function	—	• A/D converter start request at a match between TADCORA_4S and TCNT_4S • A/D converter start request at a match between TADCORB_4S and TCNT_4S	—
Interrupt skipping function	• Skips TGRA_3S compare match interrupts	• Skips TCIV_4S interrupts	—

[Legend]
√: Possible
—: Not possible

16.6 Serial Port Register (SCSPTR) and SCI Pins

The relationship between SCSPTR and the SCI pins is shown in figures 16.19 and 16.20.

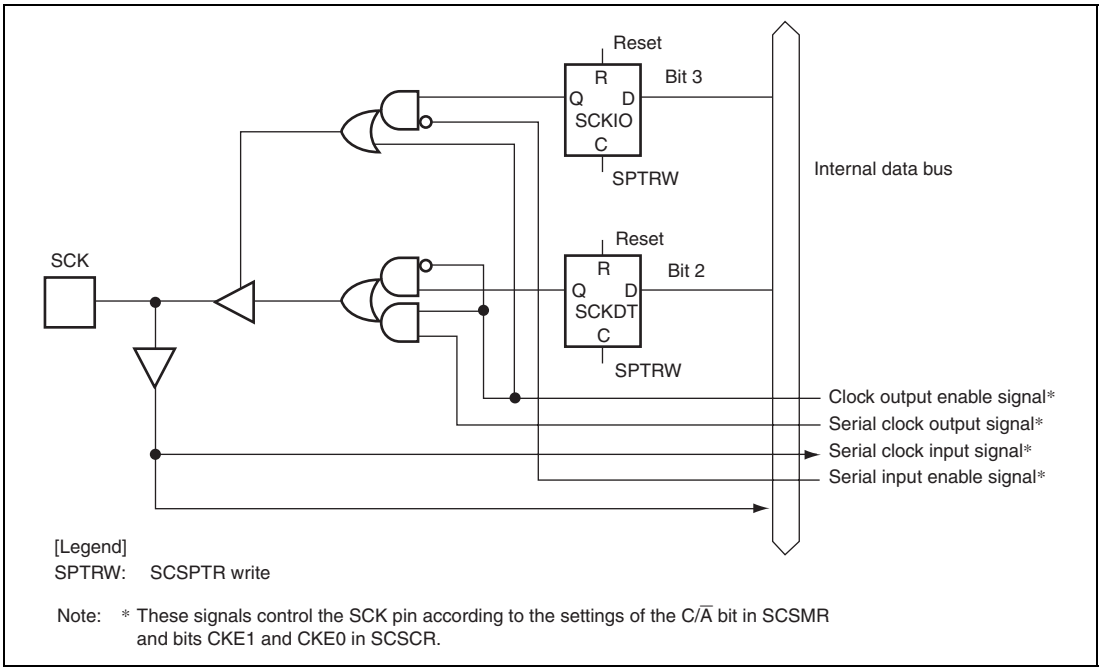


Figure 16.19 SCKIO Bit, SCKDT Bit, and SCK Pin

18.4.7 Clock Synchronous Communication Mode

In clock synchronous communication mode, data communications are performed via three lines: clock line (SSCK), data input line (SSI), and data output line (SSO).

(1) Initial Settings in Clock Synchronous Communication Mode

Figure 18.12 shows an example of the initial settings in clock synchronous communication mode. Before data transfer, clear both the TE and RE bits in SSER to 0 to set the initial values.

Note: Before changing operating modes and communications formats, clear both the TE and RE bits to 0. Although clearing the TE bit to 0 sets the TDRE bit to 1, clearing the RE bit to 0 does not change the values of the RDRF and ORER bits and SSRDR. Those bits retain the previous values.

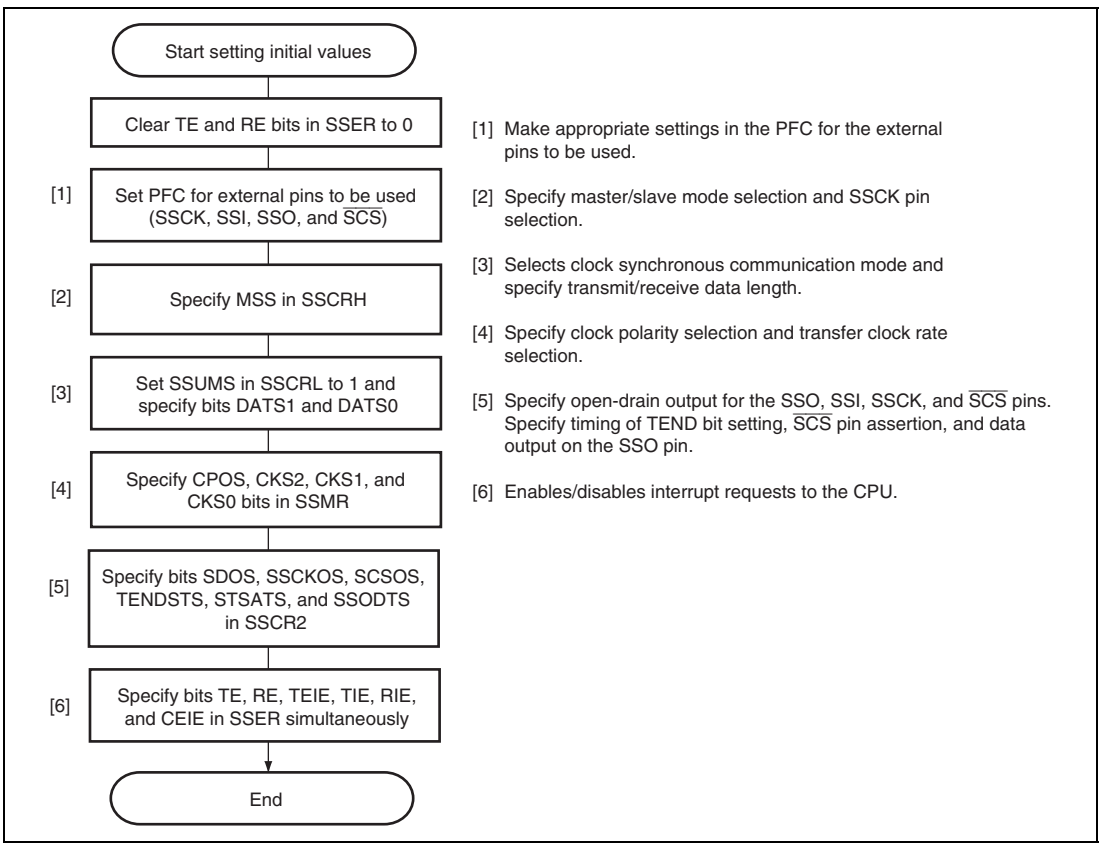


Figure 18.12 Example of Initial Settings in Clock Synchronous Communication Mode

- BCR0 (Address = H'006)

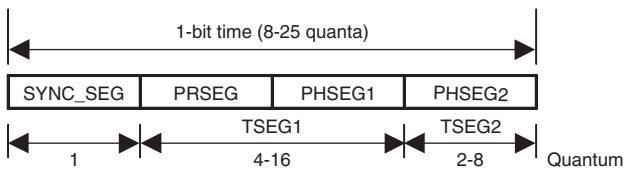
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	BRP[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 8 to 15 : Reserved. The written value should always be '0' and the returned value is '0'.

Bits 7 to 0—Baud Rate Pre-scale (BRP[7:0] = BCR0 [7:0]): These bits are used to define the peripheral bus clock periods contained in a Time Quantum.

Bit 7: BRP[7]	Bit 6: BRP[6]	Bit 5: BRP[5]	Bit 4: BRP[4]	Bit 3: BRP[3]	Bit 2: BRP[2]	Bit 1: BRP[1]	Bit 0: BRP[0]	Description
0	0	0	0	0	0	0	0	2 × peripheral bus clock (Initial value)
0	0	0	0	0	0	0	1	4 × peripheral bus clock
0	0	0	0	0	0	1	0	6 × peripheral bus clock
: :	: :	: :	: :	: :	: :	: :	: :	2 × (register value+1) × peripheral bus clock
0	1	1	1	1	1	1	1	512 × peripheral bus clock

- Requirements of Bit Configuration Register



SYNC_SEG: Segment for establishing synchronisation of nodes on the CAN bus. (Normal bit edge transitions occur in this segment.)

PRSEG: Segment for compensating for physical delay between networks.

PHSEG1: Buffer segment for correcting phase drift (positive). (This segment is extended when synchronisation (resynchronisation) is established.)

PHSEG2: Buffer segment for correcting phase drift (negative). (This segment is shortened when synchronisation (resynchronisation) is established)

TSEG1: TSG1 + 1

Table 23.14 Multiplexed Pins (SH7286 Port E)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)	Function 6 (Related Module)	Function 7 (Related Module)	Function 8 (Related Module)	Function 9 (Related Module)
E	PE15 I/O (Port)	—	DACK1 output (DMAC)	$\overline{\text{IRQOUT}}$ output (INTC)	—	—	TIOC4D I/O (MTU2)	—	—
	PE14 I/O (Port)	$\overline{\text{AH}}$ output (BSC)	DACK0 output (DMAC)	—	—	—	TIOC4C I/O (MTU2)	—	—
	PE13 I/O (Port)	—	—	$\overline{\text{MRES}}$ input (system control)	—	—	TIOC4B I/O (MTU2)	—	—
	PE12 I/O (Port)	—	—	—	—	—	TIOC4A I/O (MTU2)	—	—
	PE11 I/O (Port)	—	—	—	—	—	TIOC3D I/O (MTU2)	—	—
	PE10 I/O (Port)	—	—	—	—	TXD2 output (SCI)	TIOC3C I/O (MTU2)	—	—
	PE9 I/O (Port)	—	—	—	—	—	TIOC3B I/O (MTU2)	—	—
	PE8 I/O (Port)	—	—	—	—	SCK2 I/O (SCI)	TIOC3A I/O (MTU2)	—	—
	PE7 I/O (Port)	$\overline{\text{BS}}$ output (BSC)	—	$\overline{\text{UBCTRG}}$ output (UBC)	—	RXD2 input (SCI)	TIOC2B I/O (MTU2)	—	—
	PE6 I/O (Port)	—	—	—	TIOC3DS I/O (MTU2S)	SCK3 I/O (SCIF)	TIOC2A I/O (MTU2)	—	—
	PE5 I/O (Port)	—	—	—	TIOC3BS I/O (MTU2S)	TXD3 output (SCIF)	TIOC1B I/O (MTU2)	—	—
	PE4 I/O (Port)	—	—	—	—	RXD3 input (SCIF)	TIOC1A I/O (MTU2)	—	—
	PE3 I/O (Port)	—	TEND1 output (DMAC)	—	TIOC4DS I/O (MTU2S)	—	TIOC0D I/O (MTU2)	—	—

Bit	Bit Name	Initial Value	R/W	Description
6 to 4	PB1MD[2:0]	000*	R/W	PB1 Mode Select the function of the PB1/A17/REFOUT/IRQ4/$\overline{\text{ADTRG}}$ pin. 000: PB1 I/O (port) 001: A17 output (BSC) 010: REFOUT output (BSC) 011: IRQ4 input (INTC) 100: Setting prohibited 101: Setting prohibited 110: Setting prohibited 111: $\overline{\text{ADTRG}}$ input (ADC)
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	PB0MD[2:0]	000*	R/W	PB0 Mode Select the function of the PB0/A16/IRQ3 pin. 000: PB0 I/O (port) 001: A16 output (BSC) 010: Setting prohibited 011: IRQ3 input (INTC) 100: Setting prohibited 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited

Note: * The initial value is 1 during the on-chip ROM disabled external extension mode.

Table 24.4 Port B Data Registers H and L (PBDRH and PBDRL) Read/Write Operations

- PBDRH bits 3 to 0 and PBDRL bits 15 to 6 and 3 to 0

PBDRH, PBDRL	Pin Function	Read	Write
0	General input	Pin state	Can write to PBDRH or PBDRL, but it has no effect on pin state.
	Other than general input	Pin state	Can write to PBDRH or PBDRL, but it has no effect on pin state.
1	General output	PBDRH/PBDRL value	The value written is output from the pin.
	Other than general output	PBDRH/PBDRL value	Can write to PBDRH or PBDRL, but it has no effect on pin state.

25.3.6 USB Interrupt Enable Register 1 (USBIER1)

USBIER1 enables the interrupt requests indicated in USB interrupt flag register 1 (USBIFR1). When an interrupt flag is set while the corresponding bit in USBIER1 is set to 1, an interrupt request is sent to the CPU. The interrupt vector number is decided by the contents of USB interrupt select register 1 (USBISR1).

USBEPDR0I is initialized to H'00 by a power-on reset.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	EP3TR	EP3TS	VBUSF
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved The write value should always be 0.
2	EP3TR	0	R/W	EP3 transfer request
1	EP3TS	0	R/W	EP3 transmit completion
0	VBUSF	0	R/W	USB bus connection

(2) Flash Program Code Select Register (FPCS)

FPCS selects the on-chip programming program to be downloaded.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	PPVS
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PPVS	0	R/W	Program Pulse Single Selects the programming program. 0: On-chip programming program is not selected [Clearing condition] When transfer is completed 1: On-chip programming program is selected

(3) Flash Erase Code Select Register (FECS)

FECS selects download of the on-chip erasing program.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	EPVB
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

1. Select Erasure

In response to the erasure selection command, the boot program transfers the program that performs erasure, i.e. erases data in the user MAT.

Command	H'48

- Command H'48 (1 byte): Selects erasure.

Response	H'06

- Response H'06 (1 byte): Response to selection of erasure
  This ACK code is returned after transfer of the program that performs erasure.

Error response	H'C8	ERROR

- Error response H'C8 (1 byte): Error response to selection of erasure
- ERROR (1 byte): Error code
  H'54: Error in selection processing (processing was not completed because of a transfer error.)

2. Block Erasure

In response to the block erasure command, the boot program erases the data in a specified block of the user MAT.

Command	H'58	Size	Block number	SUM

- Command H'58 (1 byte): Erasure of a block
- Size (1 byte): The number of characters in the block number field (fixed at 1)
- Block number (1 byte): Block number of the block to be erased
- SUM (1 byte): Checksum

Response	H'06

- Response H'06 (1 byte): Response to the block erasure command
  This ACK code is returned when the block has been erased.