Renesas Electronics America Inc - R5F72865D100FP#U2 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH2A
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, SCI, SSU, USB
Peripherals	DMA, PWM, WDT
Number of I/O	101
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x12b, 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f72865d100fp-u2

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Classification	Symbol	I/O	Name	Function
Multi-function timer pulse unit 2 (MTU2)	TCLKA, TCLKB, TCLKC, TCLKD	Input	MTU2 timer clock input	External clock input pins for the timer.
	TIOC0A, TIOC0B, TIOC0C, TIOC0D	I/O	MTU2 input capture/output compare (channel 0)	The TGRA_0 to TGRD_0 input capture input/output compare output/PWM output pins.
	TIOC1A, TIOC1B	I/O	MTU2 input capture/output compare (channel 1)	The TGRA_1 and TGRB_1 input capture input/output compare output/PWM output pins.
	TIOC2A, TIOC2B	I/O	MTU2 input capture/output compare (channel 2)	The TGRA_2 and TGRB_2 input capture input/output compare output/PWM output pins.
	TIOC3A, TIOC3B, TIOC3C, TIOC3D	I/O	MTU2 input capture/output compare (channel 3)	The TGRA_3 to TGRD_3 input capture input/output compare output/PWM output pins.
	TIOC4A, TIOC4B, TIOC4C, TIOC4D	I/O	MTU2 input capture/output compare (channel 4)	The TGRA_4 to TGRD_4 input capture input/output compare output/PWM output pins.
	TIC5U, TIC5V, TIC5W	Input	MTU2 input capture (channel 5)	The TGRU_5, TGRV_5, and TGRW_5 input capture input/dead time compensation input pins.
Port output enable (POE)	$\overline{\text{POE8}}$ to $\overline{\text{POE0}}$	Input	Port output control	Request signal input to place the MTU2 and MTU2S waveform output pin in the high impedance state (SH7243 has only $\overline{\text{POE8}}$, $\overline{\text{POE4}}$, $\overline{\text{POE3}}$, and $\overline{\text{POE0}}$).

(3) Break Condition Specified for I Bus Data Access Cycle

(Example 3-1)

- Register specifications
  BBR_0 = H'0094, BAR_0 = H'00314156, BAMR_0 = H'00000000,
  BBR_1 = H'12A9, BAR_1 = H'00055555, BAMR_1 = H'00000000, BRCR = H'00000000
  <Channel 0>
  Address: H'00314156, Address mask: H'00000000
  Bus cycle: I bus/instruction fetch/read (operand size is not included in the condition)
  <Channel 1>
  Address: H'00055555, Address mask: H'00000000
  Bus cycle: I bus/data access/write/byte
  On channel 0, the setting of I bus/instruction fetch is ignored.
  On channel 1, a user break occurs when the DMAC writes byte data in address H'00055555 on the I bus (write by the CPU does not generate a user break).

7.5 Interrupt Source

The UBC has the user break interrupt as an interrupt source.

Table 7.4 gives details on this interrupt source.

A user break interrupt is generated when one of the compare match flags (SCMFD3 to SCMFD0 and SCMFC3 to SCMFC0) in the break control register (BRCR) is set to 1. Clearing the interrupt flag bit to 0 cancels the interrupt request.

Table 7.4 Interrupt Source

Abbreviation	Interrupt Source	Interrupt Enable Bit	Interrupt Flag	Interrupt Level
User break	User break interrupt	—	SCMFD3, SCMFD2, SCMFD1, SCMFD0, SCMFC3, SCMFC2, SCMFC1, SCMFC0	Fixed to 15

Table 9.20 Relationship between Bus Width, Access Size, and Number of Bursts

Bus Width	Access Size	CSnWCR. BST[1:0] Bits	Number of Bursts	Access Count
8 bits	8 bits	Not affected	1	1
	16 bits	Not affected	2	1
	32 bits	Not affected	4	1
	16 bytes*2	x0	16	1
		10	4	4
16 bits	8 bits	Not affected	1	1
	16 bits	Not affected	1	1
	32 bits	Not affected	2	1
	16 bytes*2	00	8	1
		01	2	4
		10*1	4	2
			2, 4, 2	3

Notes: 1. When the bus width is 16 bits, the access size is 16 bits, and the BST[1:0] bits in CSnWCR are 10, the number of bursts and access count depend on the access start address. At address H'xxx0 or H'xxx8, 4-4 burst access is performed. At address H'xxx4 or H'xxxC, 2-4-2 burst access is performed.

2. Only the DMAC is capable of transfer with 16 bytes as the unit of access. The maximum unit of access for the DTC and CPU is 32 bits.

10.3.1 DMA Source Address Registers (SAR)

The DMA source address registers (SAR) are 32-bit readable/writable registers that specify the source address of a DMA transfer. During a DMA transfer, these registers indicate the next source address. When the data of an external device with DACK is transferred in single address mode, SAR is ignored.

To transfer data of 16-bit or 32-bit width, specify the address with 16-bit or 32-bit address boundary respectively. To transfer data in units of 16 bytes, set a value at a 16-byte boundary.

SAR is initialized to H'00000000 by a reset and retains the value in software standby mode and module standby mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

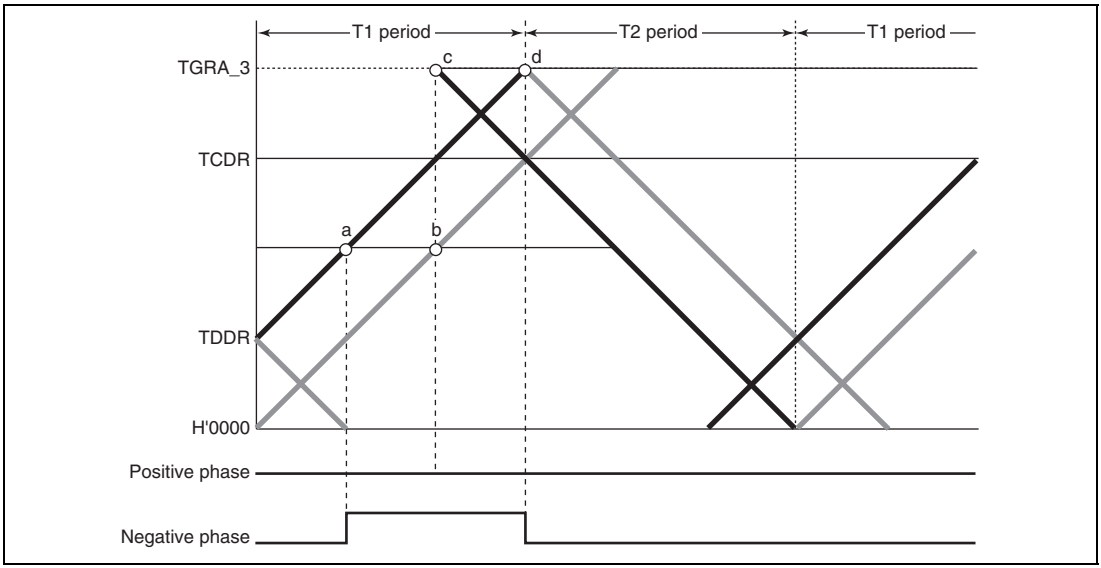


Figure 11.51 Example of Complementary PWM Mode 0% and 100% Waveform Output (3)

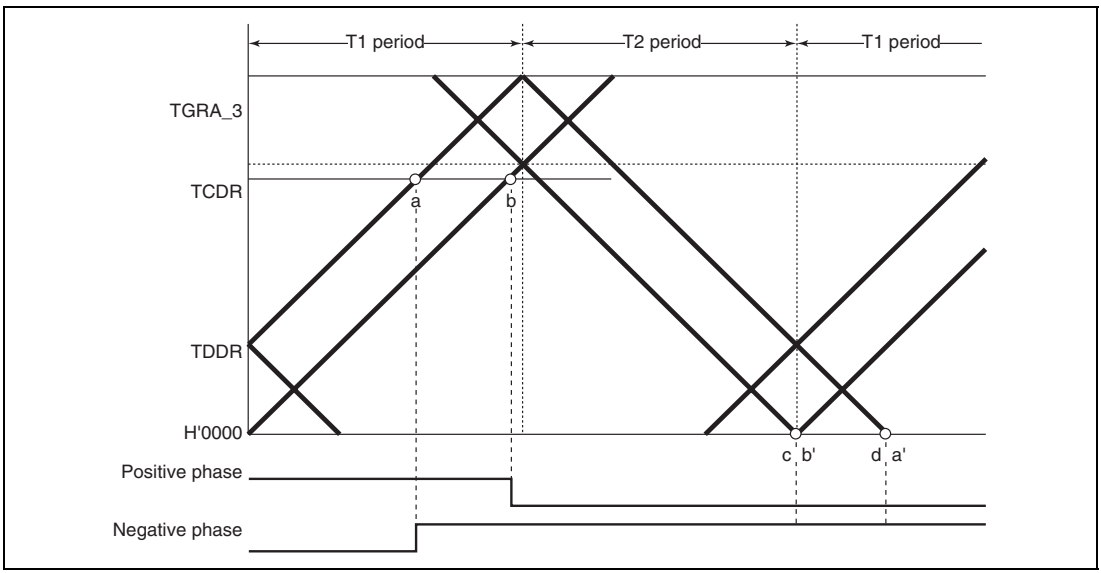
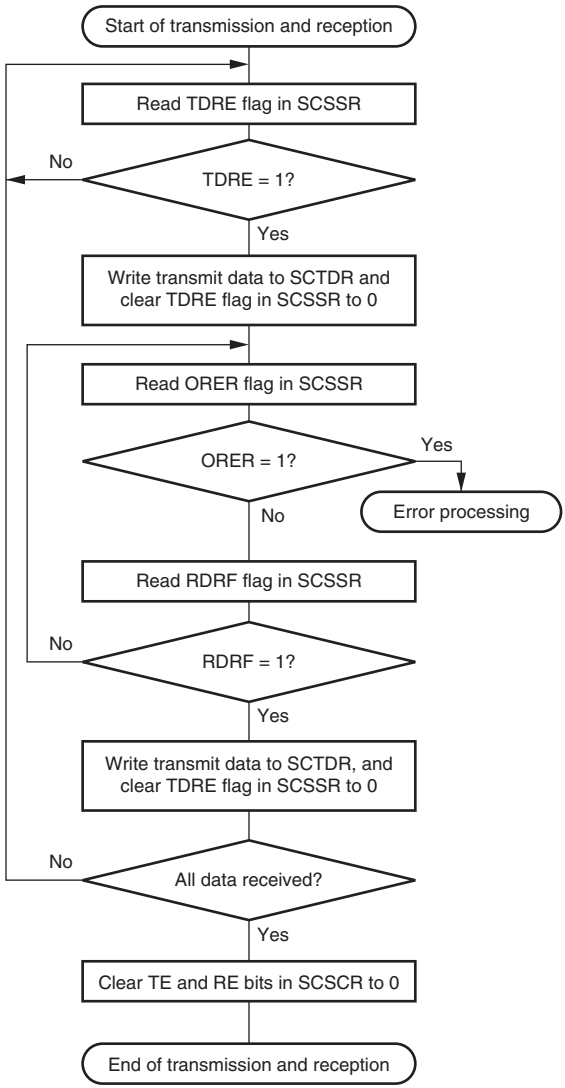


Figure 11.52 Example of Complementary PWM Mode 0% and 100% Waveform Output (4)



[1] SCI status check and transmit data write:
Read SCSSR and check that the TDRE flag is set to 1, then write transmit data to SCTDR and clear the TDRE flag to 0.
Transition of the TDRE flag from 0 to 1 can also be identified by a TXI interrupt.

[2] Receive error processing:
If a receive error occurs, read the ORER flag in SCSSR, and after performing the appropriate error processing, clear the ORER flag to 0. Reception cannot be resumed if the ORER flag is set to 1.

[3] SCI status check and receive data read:
Read SCSSR and check that the RDRF flag is set to 1, then read the receive data in SCRDR and clear the RDRF flag to 0. Transition of the RDRF flag from 0 to 1 can also be identified by an RXI interrupt.

[4] Serial transmission/reception continuation procedure:
To continue serial transmission/reception, before the MSB (bit 7) of the current frame is received, finish reading the RDRF flag, reading SCRDR, and clearing the RDRF flag to 0. Also, before the MSB (bit 7) of the current frame is transmitted, read 1 from the TDRE flag to confirm that writing is possible. Then write data to SCTDR and clear the TDRE flag to 0.
Checking and clearing of the TDRE flag is automatic when the DTC is activated by a transmit data empty interrupt (TXI) request and data is written to SCTDR. Also, the RDRF flag is cleared automatically when the DTC is activated by a receive data full interrupt (RXI) request and the SCRDR value is read.

[5] Serial transmission/reception end procedure:
To finish serial transmission/reception, clear the TE and RE bits in SCSCR to 0 simultaneously.

Note: When switching from transmit or receive operation to simultaneous transmit and receive operations, first clear the TE bit and RE bit to 0, then set both these bits to 1 simultaneously.

Figure 16.14 Sample Flowchart for Transmitting/Receiving Serial Data

Bit	Bit Name	Initial Value	R/W	Description
2	AL/OVE	0	R/W	Arbitration Lost Flag/Overrun Error Flag Indicates that arbitration was lost in master mode with the I²C bus format and that the final bit has been received while RDRF = 1 with the clocked synchronous format. When two or more master devices attempt to seize the bus at nearly the same time, if the I²C bus interface 3 detects data differing from the data it sent, it sets AL to 1 to indicate that the bus has been occupied by another master. [Clearing condition] • When 0 is written in AL/OVE after reading AL/OVE = 1 [Setting conditions] • If the internal SDA and SDA pin disagree at the rise of SCL in master transmit mode • When the SDA pin outputs high in master mode while a start condition is detected • When the final bit is received with the clocked synchronous format while RDRF = 1
1	AAS	0	R/W	Slave Address Recognition Flag In slave receive mode, this flag is set to 1 if the first frame following a start condition matches bits SVA[6:0] in SAR. [Clearing condition] • When 0 is written in AAS after reading AAS = 1 [Setting conditions] • When the slave address is detected in slave receive mode • When the general call address is detected in slave receive mode.
0	ADZ	0	R/W	General Call Address Recognition Flag This bit is valid in slave receive mode with the I²C bus format. [Clearing condition] • When 0 is written in ADZ after reading ADZ = 1 [Setting condition] • When the general call address is detected in slave receive mode

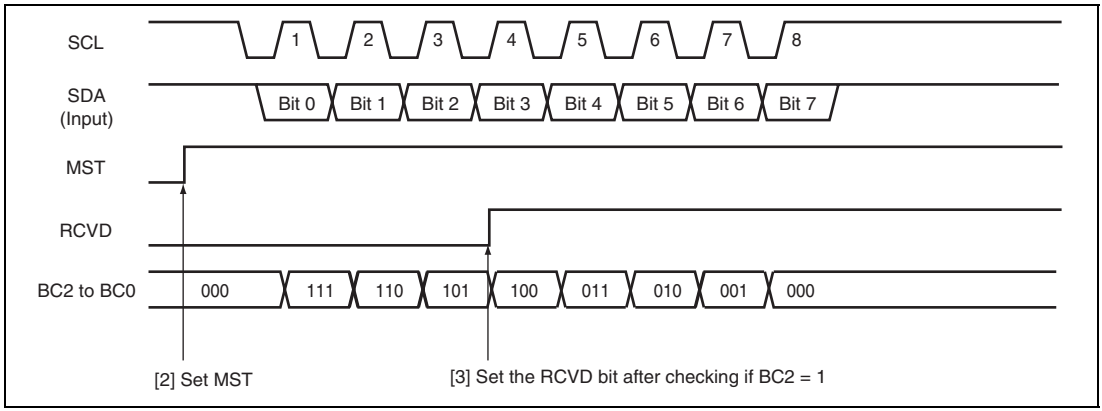


Figure 19.16 Operation Timing For Receiving One Byte (MST = 1)

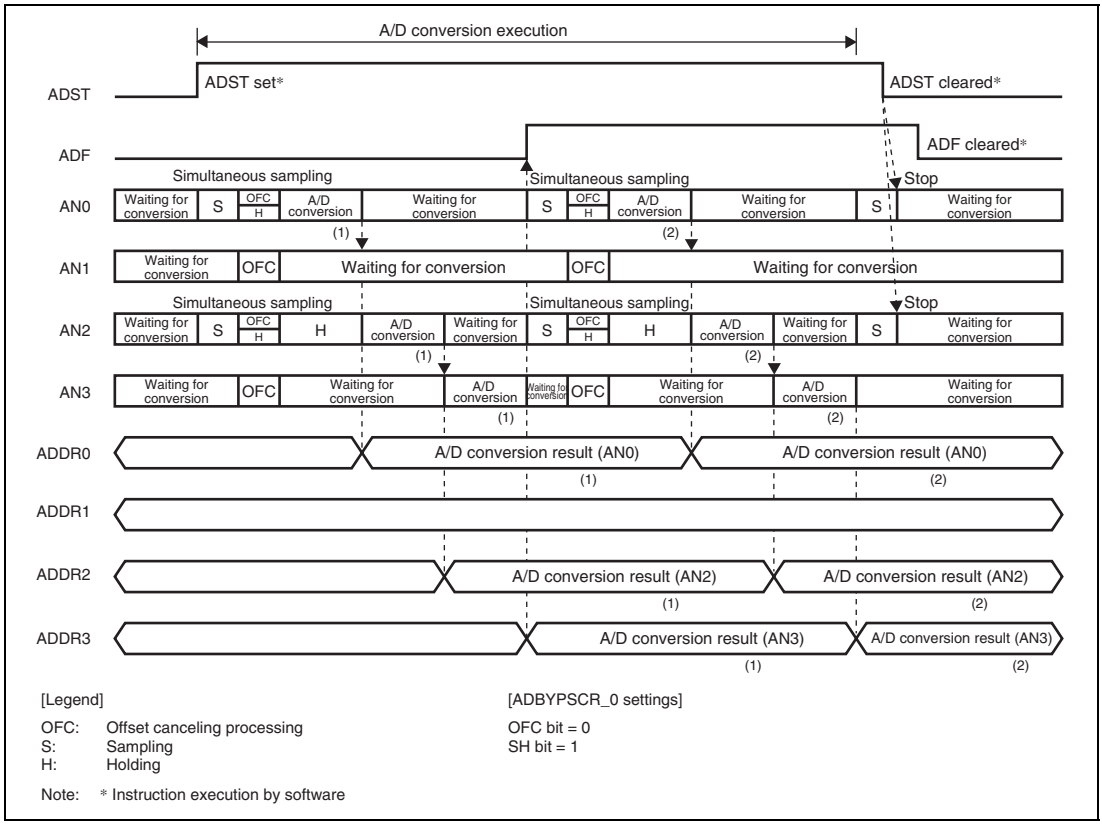


Figure 20.6 Example 1 of A/D Converter Operation (Continuous Scan Mode, Sample-and-Hold Circuit Enabled, and Offset Canceling Circuit Enabled)

(1) Message Control Field

STDID[10:0]: These bits set the identifier (standard identifier) of data frames and remote frames.

EXTID[17:0]: These bits set the identifier (extended identifier) of data frames and remote frames.

RTR (Remote Transmission Request bit) : Used to distinguish between data frames and remote frames. This bit is overwritten by received CAN Frames depending on Data Frames or Remote Frames.

Important: Please note that, when ATX bit is set with the setting MBC=001(bin), the RTR bit will never be set. When a Remote Frame is received, the CPU can be notified by the corresponding RFPR set or IRR[2] (Remote Frame Request Interrupt), however, as RCAN-ET needs to transmit the current message as a Data Frame, the RTR bit remains unchanged.

Important: In order to support automatic answer to remote frame when MBC=001(bin) is used and ATX=1 the RTR flag must be programmed to zero to allow data frame to be transmitted.

Note: when a Mailbox is configured to send a remote frame request the DLC used for transmission is the one stored into the Mailbox.

RTR	Description
0	Data frame
1	Remote frame

IDE (Identifier Extension bit) : Used to distinguish between the standard format and extended format of CAN data frames and remote frames.

IDE	Description
0	Standard format
1	Extended format

Bit	Bit Name	Initial Value	R/W	Description
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	PD10MD[2:0]	000*	R/W	PD10 Mode Select the function of the PD10/D10/TIOC3BS pin. 000: PD10 I/O (port) 001: D10 I/O (BSC) 010: Setting prohibited 011: Setting prohibited 100: TIOC3BS I/O (MTU2S) 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	PD9MD[2:0]	000*	R/W	PD9 Mode Select the function of the PD9/D9/TIOC3CS pin. 000: PD9 I/O (port) 001: D9 I/O (BSC) 010: Setting prohibited 011: Setting prohibited 100: TIOC3CS I/O (MTU2S) 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

- Port D Control Register L3 (PDCRL3)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	PD11MD[2:0]			-	PD10MD[2:0]			-	PD9MD[2:0]			-	PD8MD[2:0]		
Initial value:	0	0	0	0*	0	0	0	0*	0	0	0	0*	0	0	0	0*
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Note: * The initial value is 1 during the on-chip ROM disabled external extension mode.

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	PD11MD[2:0]	000*	R/W	PD11 Mode Select the function of the PD11/D11/TIOC3DS pin. 000: PD11 I/O (port) 001: D11 I/O (BSC) 010: Setting prohibited 011: Setting prohibited 100: TIOC3DS I/O (MTU2S) 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	PD10MD[2:0]	000*	R/W	PD10 Mode Select the function of the PD10/D10/TIOC3BS pin. 000: PD10 I/O (port) 001: D10 I/O (BSC) 010: Setting prohibited 011: Setting prohibited 100: TIOC3BS I/O (MTU2S) 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
6 to 4	PE13MD[2:0]	000	R/W	PE13 Mode Select the function of the PE13/$\overline{\text{MRES}}$/TIOC4B pin. 000: PE13 I/O (port) 001: Setting prohibited 010: Setting prohibited 011: $\overline{\text{MRES}}$ (system control) 100: Setting prohibited 101: Setting prohibited 110: TIOC4B I/O (MTU2) 111: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	PE12MD[2:0]	000	R/W	PE12 Mode Select the function of the PE12/TIOC4A pin. 000: PE12 I/O (port) 001: Setting prohibited 010: Setting prohibited 011: Setting prohibited 100: Setting prohibited 101: Setting prohibited 110: TIOC4A I/O (MTU2) 111: Setting prohibited

Note: * $\overline{\text{IRQOUT}}$ (INTC) or $\overline{\text{REFOUT}}$ (BSC) is selected by the IRQOUT function control register (IFCR).

29.4.4 H-UDI Reset

An H-UDI reset is executed by setting an H-UDI reset assert command in SDIR. An H-UDI reset is of the same kind as a power-on reset. An H-UDI reset is released by setting an H-UDI reset negate command. The required time between the H-UDI reset assert command and H-UDI reset negate command is the same as time for keeping the $\overline{\text{RES}}$ pin low to apply a power-on reset.

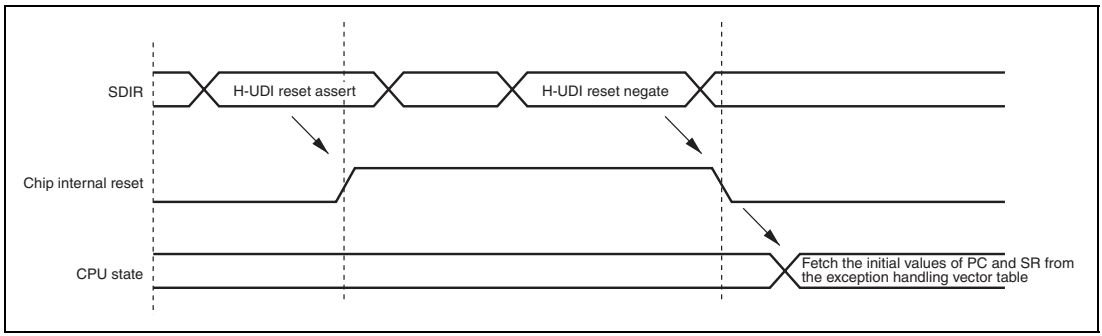


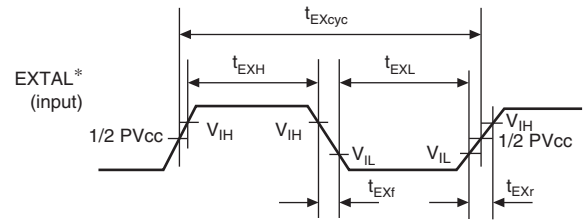
Figure 29.4 H-UDI Reset

29.4.5 H-UDI Interrupt

The H-UDI interrupt function generates an interrupt by setting a command from the H-UDI in SDIR. An H-UDI interrupt is a general exception/interrupt operation, resulting in fetching the exception service routine start address from the exception handling vector table, jumping to that address, and starting program execution from that address. This interrupt request has a fixed priority level of 15.

H-UDI interrupts are accepted in sleep mode, but not in software standby mode.

Module Name	Register Name	Abbreviation	Number of Bits	Address	Access Size
MTU2S	Timer A/D converter start request cycle set buffer register B_4S	TADCOBRB_4S	16	H'FFFE4A4A	16
	Timer control register U_5S	TCRU_5S	8	H'FFFE4884	8
	Timer control register V_5S	TCRV_5S	8	H'FFFE4894	8
	Timer control register W_5S	TCRW_5S	8	H'FFFE48A4	8
	Timer I/O control register U_5S	TIORU_5S	8	H'FFFE4886	8
	Timer I/O control register V_5S	TIORV_5S	8	H'FFFE4896	8
	Timer I/O control register W_5S	TIORW_5S	8	H'FFFE48A6	8
	Timer interrupt enable register_5S	TIER_5S	8	H'FFFE48B2	8
	Timer status register_5S	TSR_5S	8	H'FFFE48B0	8
	Timer start register_5S	TSTR_5S	8	H'FFFE48B4	8
	Timer counter U_5S	TCNTU_5S	16	H'FFFE4880	16, 32
	Timer counter V_5S	TCNTV_5S	16	H'FFFE4890	16, 32
	Timer counter W_5S	TCNTW_5S	16	H'FFFE48A0	16, 32
	Timer general register U_5S	TGRU_5S	16	H'FFFE4882	16
	Timer general register V_5S	TGRV_5S	16	H'FFFE4892	16
	Timer general register W_5S	TGRW_5S	16	H'FFFE48A2	16
	Timer compare match clear register S	TCNTCMPCLRS	8	H'FFFE48B6	8
	Timer start register S	TSTRS	8	H'FFFE4A80	8, 16
	Timer synchronous register S	TSYRS	8	H'FFFE4A81	8
	Timer read/write enable register S	TRWERS	8	H'FFFE4A84	8
	Timer output master enable register S	TOERS	8	H'FFFE4A0A	8
	Timer output control register 1S	TOCR1S	8	H'FFFE4A0E	8, 16
	Timer output control register 2S	TOCR2S	8	H'FFFE4A0F	8
	Timer gate control register S	TGCRS	8	H'FFFE4A0D	8
	Timer cycle control register S	TCDRS	16	H'FFFE4A14	16, 32
	Timer dead time data register S	TDDRS	16	H'FFFE4A16	16
	Timer subcounter S	TCNTSS	16	H'FFFE4A20	16, 32
	Timer cycle buffer register S	TCBRS	16	H'FFFE4A22	16
	Timer interrupt skipping set register S	TITCRS	8	H'FFFE4A30	8, 16
	Timer interrupt skipping counter S	TITCNTS	8	H'FFFE4A31	8
	Timer buffer transfer set register S	TBTERS	8	H'FFFE4A32	8
	Timer dead time enable register S	TDERS	8	H'FFFE4A34	8
	Timer synchronous clear register S	TSYCRS	8	H'FFFE4A50	8



Note: * When the clock is input on the EXTAL pin.

Figure 31.1 EXTAL Clock Input Timing

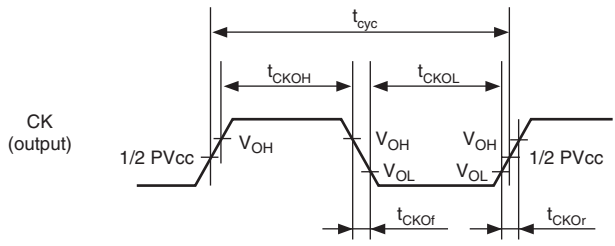
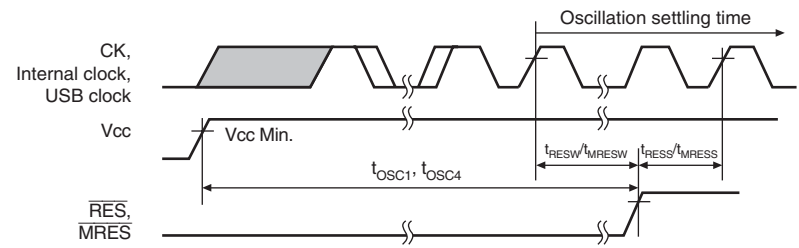


Figure 31.2 CK Clock Output Timing



Note: Oscillation settling time when the internal oscillator is used.

Figure 31.3 Power-On Oscillation Settling Time

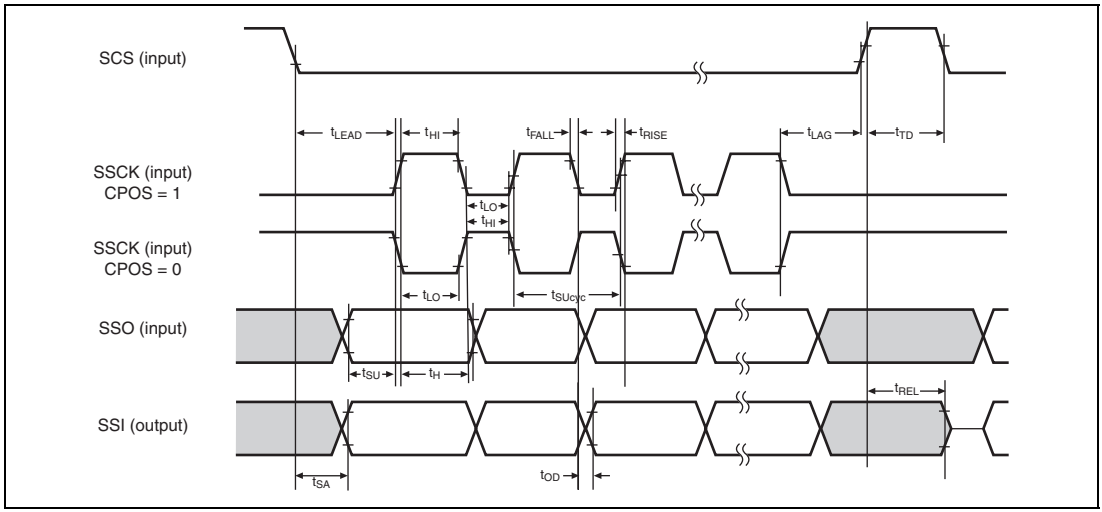


Figure 31.51 SSU Timing (Slave, CPHS = 1)

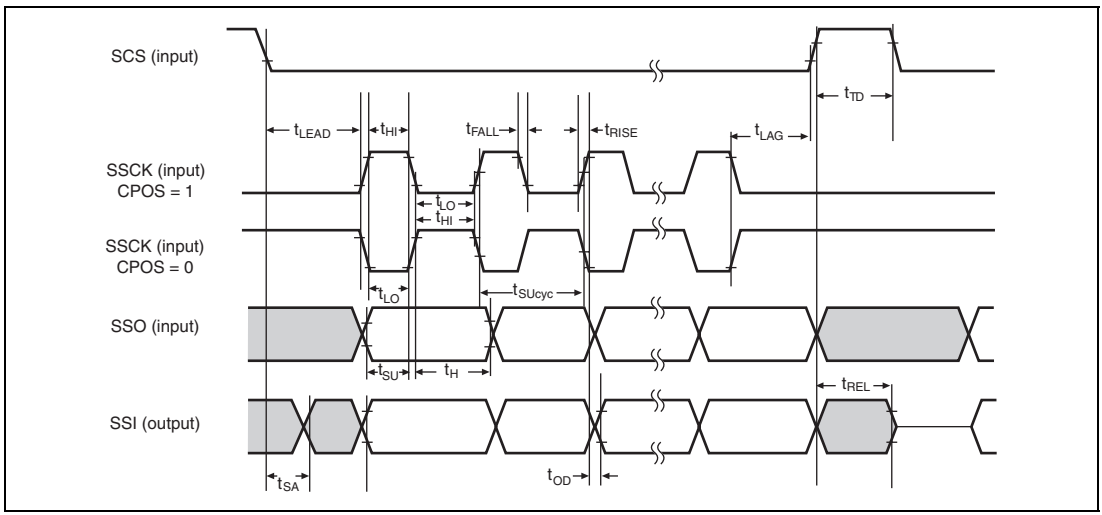


Figure 31.52 SSU Timing (Slave, CPHS = 0)

Pin Function		Pin State									
		Reset State				Power-Down State					
		Power-On									
		Expansion without ROM		Expansion with ROM	Single-chip				Bus Master-ship Release	Oscillation Stop Detected	POE Function Used
Type	Pin Name	8 bits	16 bits			Manual	Software Standby	Sleep			
SCIF	SCK3	Z				I/O	K*1	I/O	I/O	I/O	I/O
	SCK3 (PE6)	Z				I/O	Z (MZIZEL in HCPCR = 0) K*1 (MZIZEL in HCPCR = 1)	I/O	I/O*8	I/O	I/O
	RXD3	Z				I	Z	I	I	I	I
	TXD3	Z				O	O*1	O	O	O	O
	TXD3 (PE5)	Z				O	Z (MZIZEL in HCPCR = 0) O*1 (MZIZEL in HCPCR = 1)	O	O	O*8	O
UBC	$\overline{\text{UBCTRG}}$	Z				O	O*1	O	O	O	O
A/D Converter	AN0 to AN7	Z				I	Z	I	I	I	I
	$\overline{\text{ADTRG}}$	Z				I	Z	I	I	I	I
I/O Port	PA6 to PA9, PA10 to PA15	Z				I/O	K*1	I/O	I/O	I/O	I/O
	PB0, PB1, PB6 to PB8, PB11, PB12	Z				I/O	K*1	I/O	I/O	I/O	I/O
	PC0 to PC15	Z				I/O	K*1	I/O	I/O	I/O	I/O
	PD0 to PD8, PD10	Z				I/O	K*1	I/O	I/O	I/O	I/O
	PD9, PD11 to PD15	Z				I/O	Z (MZIZDL in HCPCR = 0) K*1 (MZIZDL in HCPCR = 1)	I/O	I/O	I/O*6	Z
	PE4, PE7, PE8, PE10	Z				I/O	K*1	I/O	I/O	I/O	I/O
	PE0 to PE3, PE5, PE6	Z				I/O	Z (MZIZEL in HCPCR = 0) K*1 (MZIZEL in HCPCR = 1)	I/O	I/O	I/O*8	Z

Pin Function		Pin State									
		Reset State					Power-Down State				
		Power-On									
Type	Pin Name	Expansion without ROM 8 bits	Expansion without ROM 16 bits	Expansion with ROM	Single-chip	Manual	Software Standby	Sleep	Bus Mastership Release	Oscillation Stop Detected	POE Function Used
MTU2S	TIOC3BS (PD29), TIOC3DS (PD28)	Z				I/O	Z (MZIZDH in HCPCR = 0) K*1 (MZIZDH in HCPCR = 1)	I/O	I/O	I/O*5	Z
	TIOC3BS (PE5), TIOC3DS (PE6)	Z				I/O	Z (MZIZEL in HCPCR = 0) K*1 (MZIZEL in HCPCR = 1)	I/O	I/O	I/O*8	Z
	TIOC4AS (PD12), TIOC4BS (PD13), TIOC4CS (PD14), TIOC4DS (PD15)	Z				I/O	Z (MZIZDL in HCPCR = 0) K*1 (MZIZDL in HCPCR = 1)	I/O	I/O	I/O*6	Z
	TIOC4AS (PD27), TIOC4BS (PD26), TIOC4CS (PD25), TIOC4DS (PD24)	Z				I/O	Z (MZIZDH in HCPCR = 0) K*1 (MZIZDH in HCPCR = 1)	I/O	I/O	I/O*5	Z
	TIOC4AS (PE0), TIOC4BS (PE1), TIOC4CS (PE2), TIOC4DS (PE3)	Z				I/O	Z (MZIZEL in HCPCR = 0) K*1 (MZIZEL in HCPCR = 1)	I/O	I/O	I/O*8	Z
	TIC5US, TIC5VS, TIC5WS	Z				I	Z	I	I	I	I
POE	$\overline{\text{POE0}}$ to $\overline{\text{POE8}}$	Z				I	Z	I	I	I	I