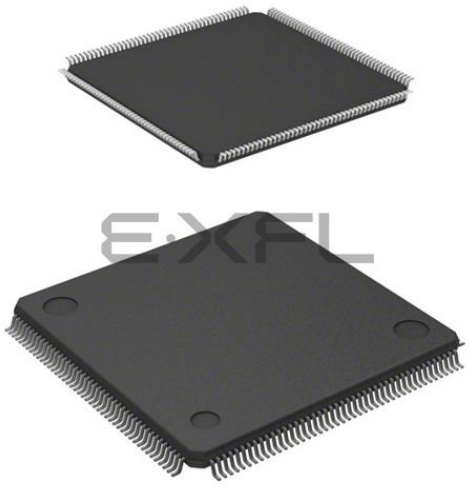

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Details	
Product Status	Not For New Designs
Core Processor	SH2A
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, SCI, SSU, USB
Peripherals	DMA, PWM, WDT
Number of I/O	101
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x12b, 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f72865n100fa-u2

The table below shows the format of instruction codes, operation, and execution states. They are described by using this format according to their classification.

Instruction	Instruction Code	Operation	Execution States	T Bit
Indicated by mnemonic.	Indicated in MSB ↔ LSB order.	Indicates summary of operation.	Value when no wait states are inserted.*1	Value of T bit after instruction is executed.
[Legend]	[Legend]	[Legend]		Explanation of Symbols
Rm: Source register	mmmm: Source register	→, ←: Transfer direction		—: No change
Rn: Destination register	nnnn: Destination register 0000: R0 0001: R1 ····· 1111: R15	(xx): Memory operand		
imm: Immediate data		M/Q/T: Flag bits in SR		
disp: Displacement*2		&: Logical AND of each bit		
	iiii: Immediate data	|: Logical OR of each bit		
	dddd: Displacement	^: Exclusive logical OR of each bit		
		~: Logical NOT of each bit		
		<<n: n-bit left shift		
		>>n: n-bit right shift		

Notes: 1. Instruction execution cycles: The execution cycles shown in the table are minimums. In practice, the number of instruction execution states will be increased in cases such as the following:
   a. When there is a conflict between an instruction fetch and a data access
   b. When the destination register of a load instruction (memory → register) is the same as the register used by the next instruction.
2. Depending on the operand size, displacement is scaled by ×1, ×2, or ×4. For details, refer to the SH-2A, SH2A-FPU Software Manual.

2.4.5 Shift Instructions

Table 2.14 Shift Instructions

Instruction		Instruction Code	Operation	Execution Cycles	T Bit	Compatibility SH2, SH2E	SH4	SH-2A
ROTL	Rn	0100nnnn00000100	T ← Rn ← MSB	1	MSB	Yes	Yes	Yes
ROTR	Rn	0100nnnn00000101	LSB → Rn → T	1	LSB	Yes	Yes	Yes
ROTCL	Rn	0100nnnn00100100	T ← Rn ← T	1	MSB	Yes	Yes	Yes
ROTCR	Rn	0100nnnn00100101	T → Rn → T	1	LSB	Yes	Yes	Yes
SHAD	Rm,Rn	0100nnnnmmmm1100	When Rm ≥ 0, Rn << Rm → Rn When Rm < 0, Rn >> |Rm| → [MSB → Rn]	1	—		Yes	Yes
SHAL	Rn	0100nnnn00100000	T ← Rn ← 0	1	MSB	Yes	Yes	Yes
SHAR	Rn	0100nnnn00100001	MSB → Rn → T	1	LSB	Yes	Yes	Yes
SHLD	Rm,Rn	0100nnnnmmmm1101	When Rm ≥ 0, Rn << Rm → Rn When Rm < 0, Rn >> |Rm| → [0 → Rn]	1	—		Yes	Yes
SHLL	Rn	0100nnnn00000000	T ← Rn ← 0	1	MSB	Yes	Yes	Yes
SHLR	Rn	0100nnnn00000001	0 → Rn → T	1	LSB	Yes	Yes	Yes
SHLL2	Rn	0100nnnn00001000	Rn << 2 → Rn	1	—	Yes	Yes	Yes
SHLR2	Rn	0100nnnn00001001	Rn >> 2 → Rn	1	—	Yes	Yes	Yes
SHLL8	Rn	0100nnnn00011000	Rn << 8 → Rn	1	—	Yes	Yes	Yes
SHLR8	Rn	0100nnnn00011001	Rn >> 8 → Rn	1	—	Yes	Yes	Yes
SHLL16	Rn	0100nnnn00101000	Rn << 16 → Rn	1	—	Yes	Yes	Yes
SHLR16	Rn	0100nnnn00101001	Rn >> 16 → Rn	1	—	Yes	Yes	Yes

Table 9.20 Relationship between Bus Width, Access Size, and Number of Bursts

Bus Width	Access Size	CSnWCR. BST[1:0] Bits	Number of Bursts	Access Count
8 bits	8 bits	Not affected	1	1
	16 bits	Not affected	2	1
	32 bits	Not affected	4	1
	16 bytes*2	x0	16	1
		10	4	4
16 bits	8 bits	Not affected	1	1
	16 bits	Not affected	1	1
	32 bits	Not affected	2	1
	16 bytes*2	00	8	1
		01	2	4
		10*1	4	2
			2, 4, 2	3

Notes: 1. When the bus width is 16 bits, the access size is 16 bits, and the BST[1:0] bits in CSnWCR are 10, the number of bursts and access count depend on the access start address. At address H'xxx0 or H'xxx8, 4-4 burst access is performed. At address H'xxx4 or H'xxxC, 2-4-2 burst access is performed.

2. Only the DMAC is capable of transfer with 16 bytes as the unit of access. The maximum unit of access for the DTC and CPU is 32 bits.

9.5.8 SRAM Interface with Byte Selection

The SRAM interface with byte selection is for access to an SRAM which has a byte-selection pin ($\overline{\text{WRxx}}$). This interface has 16-bit data pins and accesses SRAMs having upper and lower byte selection pins, such as UB and LB.

When the BAS bit in CSnWCR is cleared to 0 (initial value), the write access timing of the SRAM interface with byte selection is the same as that for the normal space interface. While in read access of a byte-selection SRAM interface, the byte-selection signal is output from the $\overline{\text{WRxx}}$ pin, which is different from that for the normal space interface. The basic access timing is shown in figure 9.36. In write access, data is written to the memory according to the timing of the byte-selection pin ($\overline{\text{WRxx}}$). For details, please refer to the Data Sheet for the corresponding memory.

If the BAS bit in CSnWCR is set to 1, the $\overline{\text{WRxx}}$ pin and RD/$\overline{\text{WR}}$ pin timings change. Figure 9.37 shows the basic access timing. In write access, data is written to the memory according to the timing of the write enable pin (RD/$\overline{\text{WR}}$). The data hold timing from RD/$\overline{\text{WR}}$ negation to data write must be acquired by setting the HW1 and HW0 bits in CSnWCR. Figure 9.38 shows the access timing when a software wait is specified.

Table 11.19 TIORL_4 (Channel 4)

				Description	
Bit 7 IOD3	**Bit 6 IOD2**	**Bit 5 IOD1**	**Bit 4 IOD0**	**TGRD_4 Function**	**TIOC4D Pin Function**
0	0	0	0	Output compare register*2	Output retained*1
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	X	0	0	Input capture register*2	Input capture at rising edge
			1		Input capture at falling edge
		1	X		Input capture at both edges

[Legend]

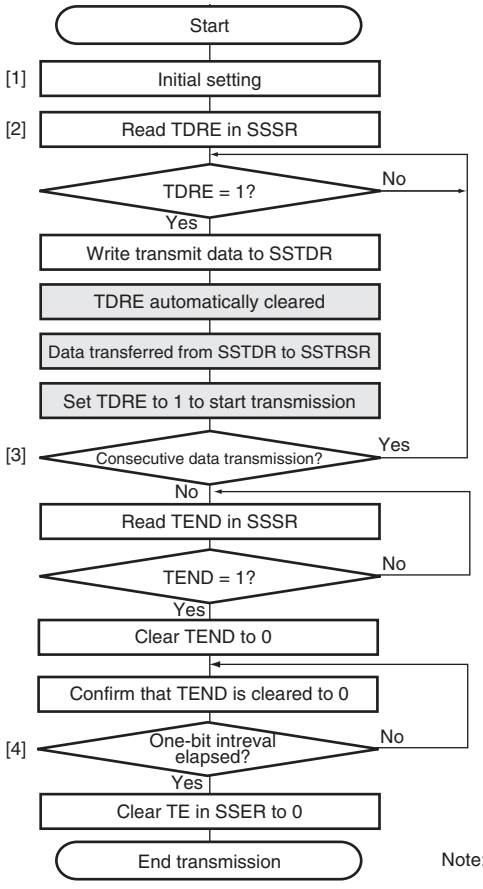
X: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. When the BFB bit in TMDR_4 is set to 1 and TGRD_4 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 16.8 Bit Rates and SCBRR Settings in Clock Synchronous Mode (2)

Bit Rate (bits/s)	Pϕ (MHz)											
	22		24		26		28		30		32	
	n	N	n	N	n	N	n	N	n	N	n	N
250												
500	3	171	3	187	3	202	3	218	3	233	3	249
1000	3	85	3	93	3	101	3	108	3	116	3	124
2500	2	137	2	149	2	162	2	174	2	187	2	199
5000	2	68	2	74	2	80	2	87	2	93	2	99
10000	1	137	1	149	1	162	1	174	1	187	1	199
25000	0	219	0	239	1	64	1	69	1	74	1	79
50000	0	109	0	119	0	129	0	139	0	149	0	159
100000	0	54	0	59	0	64	0	69	0	74	0	79
250000	0	21	0	23	0	25	0	27	0	29	0	31
500000	0	10	0	11	0	12	0	13	0	14	0	15
1000000	—	—	0	5	—	—	0	6	—	—	0	7
2500000	—	—	—	—	—	—	—	—	0	2	—	—
5000000	—	—	—	—	—	—	—	—	—	—	—	—



[1] Initial setting:
Specify the transmit data format.

[2] Check that the SSU state and write transmit data:
Write transmit data to SSTDR after reading and confirming that the TDRE bit is 1. The TDRE bit is automatically cleared to 0 and transmission is started by writing data to SSTDR.

[3] Procedure for consecutive data transmission:
To continue data transmission, confirm that the TDRE bit is 1 meaning that SSTDR is ready to be written to. After that, data can be written to SSTDR. The TDRE bit is automatically cleared to 0 by writing data to SSTDR.

[4] Procedure for data transmission end:
To end data transmission, confirm that the TEND bit is cleared to 0. After completion of transmitting the last bit, clear the TE bit to 0.

Note: Hatched boxes represent SSU internal operations.

Figure 18.14 Flowchart Example of Transmission Operation (Clock Synchronous Communication Mode)

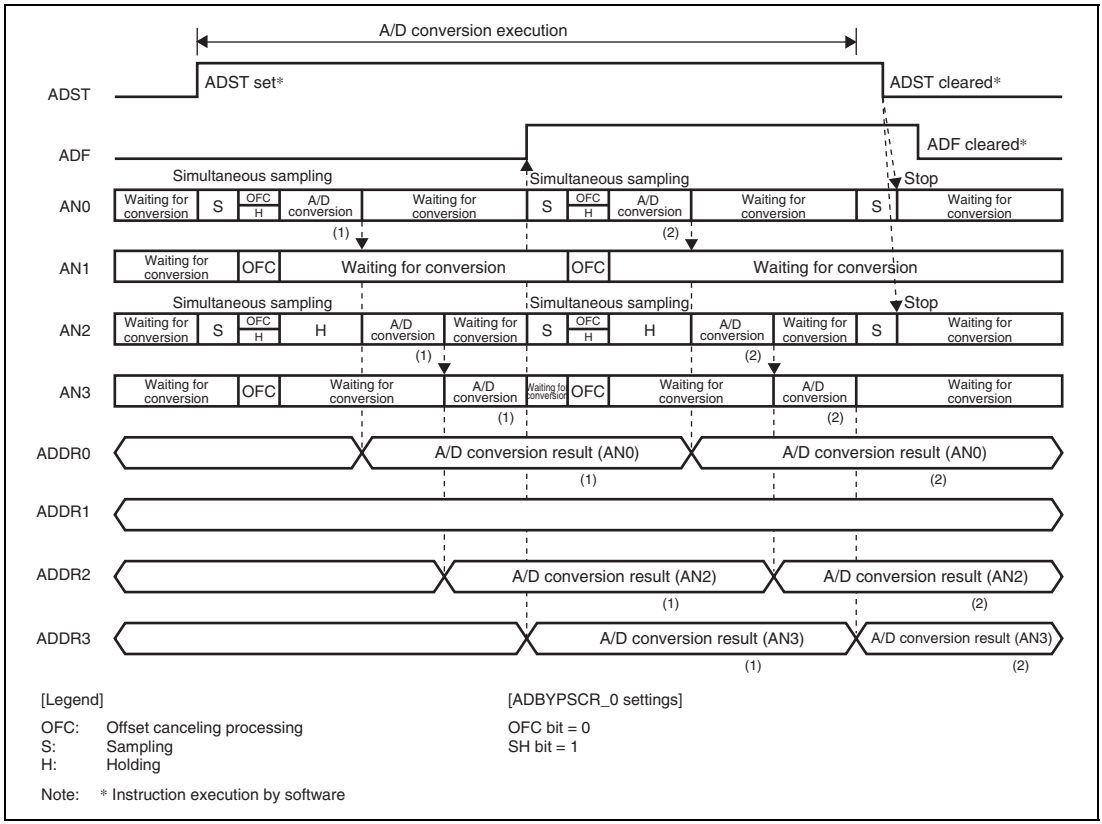


Figure 20.6 Example 1 of A/D Converter Operation (Continuous Scan Mode, Sample-and-Hold Circuit Enabled, and Offset Canceling Circuit Enabled)

(4) Abort Acknowledge Register (ABACK0)

The ABACK0 is a 16-bit read / conditionally-write registers. This register is used to signal to the CPU that a mailbox transmission has been aborted as per its request. When an abort has succeeded the RCAN-ET sets the corresponding bit in the ABACK register. The CPU may clear the Abort Acknowledge bit by writing a '1' to the corresponding bit location. Writing a '0' has no effect. An ABACK bit position is set by the RCAN-ET to acknowledge that a TXPR bit has been cleared by the corresponding TXCR bit.

- ABACK0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ABACK0[15:1]															0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	-

Note : * Only when writing a ‘1’ to clear.

Bit 15 to 1 — notifies that the requested transmission cancellation of the corresponding Mailbox has been performed successfully. The bit 15 to 1 corresponds to Mailbox-15 to 1 respectively.

Bit[15:1]:ABACK0	Description
0	[Clearing Condition] Writing ‘1’ (Initial value)
1	Corresponding Mailbox has cancelled transmission of message (Data or Remote Frame) [Setting Condition] Completion of transmission cancellation for corresponding mailbox

Bit 0 — This bit is always ‘0’ as this is a receive-only mailbox. Writing a '1' to this bit position has no effect and always read back as a ‘0’.

(5) Data Frame Receive Pending Register (RXPR0)

The RXPR0 is a 16-bit read / conditionally-write registers. The RXPR is a register that contains the received Data Frames pending flags associated with the configured Receive Mailboxes. When a CAN Data Frame is successfully stored in a receive mailbox the corresponding bit is set in the RXPR. The bit may be cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. However, the bit may only be set if the mailbox is configured by its MBC (Mailbox Configuration) to receive Data Frames. When a RXPR bit is set, it also sets IRR1 (Data Frame Received Interrupt Flag) if its MBIMR (Mailbox Interrupt Mask Register) is not set, and the interrupt signal is generated if IMR1 is not set. Please note that these bits are only set by receiving Data Frames and not by receiving Remote frames.

Bit	Bit Name	Initial Value	R/W	Description
7	PA23PCR	0	R/W	The corresponding input pull-up MOS turns on when one of these bits is set to 1.
6	PA22PCR	0	R/W	
5	PA21PCR	0	R/W	
4 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

- Port A Pull-Up MOS Control Register L (PAPCRL)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PA15 PCR	PA14 PCR	PA13 PCR	PA12 PCR	-	-	PA9 PCR	PA8 PCR	PA7 PCR	PA6 PCR	PA5 PCR	PA4 PCR	PA3 PCR	PA2 PCR	PA1 PCR	PA0 PCR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PA15PCR	0	R/W	The corresponding input pull-up MOS turns on when one of these bits is set to 1.
14	PA14PCR	0	R/W	
13	PA13PCR	0	R/W	
12	PA12PCR	0	R/W	
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

- Port B Control Register L4 (PBCRL4)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	PB12MD[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0*
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Note: * The initial value is 1 during the on-chip ROM disabled external extension mode.

Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	PB12MD[2:0]	000*	R/W	PB12 Mode Select the function of the PB12/$\overline{CS1}$/$\overline{CS7}$/IRQ1/TXD2/$\overline{CS3}$ pin. 000: PB12 I/O (port) 001: CKE output (BSC) 010: CKE output (BSC) 011: IRQ1 input (INTC) 100: Setting prohibited 101: TXD2 output (SCI) 110: Setting prohibited 111: $\overline{CS3}$ output (BSC)

Note: * The initial value is 1 during the on-chip ROM disabled external extension mode.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	PD5MD[2:0]	000*	R/W	PD5 Mode Select the function of the PD5/D5/TIC5US pin. 000: PD5 I/O (port) 001: D5 I/O (BSC) 010: Setting prohibited 011: Setting prohibited 100: TIC5US input (MTU2S) 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	PD4MD[2:0]	000*	R/W	PD4 Mode Select the function of the PD4/D4/TIC5W pin. 000: PD4 I/O (port) 001: D4 I/O (BSC) 010: Setting prohibited 011: Setting prohibited 100: Setting prohibited 101: Setting prohibited 110: TIC5W input (MTU2) 111: Setting prohibited

Note: * The initial value is 1 during the on-chip ROM disabled external extension mode.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	PE1MD[2:0]	000	R/W	PE1 Mode Select the function of the PE1/TEND0/TIOC4BS/TIOC0B pin. 000: PE1 I/O (port) 001: Setting prohibited 010: TEND0 output (DMAC) 011: Setting prohibited 100: TIOC4BS I/O (MTU2S) 101: Setting prohibited 110: TIOC0B I/O (MTU2) 111: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	PE0MD[2:0]	000	R/W	PE0 Mode Select the function of the PE0/DREQ0/TIOC4AS/TIOC0A pin. 000: PE0 I/O (port) 001: Setting prohibited 010: DREQ0 input (DMAC) 011: Setting prohibited 100: TIOC4AS I/O (MTU2S) 101: Setting prohibited 110: TIOC0A I/O (MTU2) 111: Setting prohibited

24.2.2 Port B Data Registers H and L (PBDRH and PBDRL)

PBDRH and PBDRL are 16-bit readable/writable registers that store port B data. In SH7243, bits PB12DR, PB11DR, PB8DR to PB6DR, PB1DR and PB0DR correspond to pins PB12, PB11, PB8 to PB6, PB1 and PB0 respectively (description of multiplexed functions are abbreviated here). In SH7285, bits PB12DR to PB6DR and PB3DR to PB0DR correspond to pins PB12 to PB6, and PB3 to PB0 respectively (description of multiplexed functions are abbreviated here). In SH7286, bits PB19DR to PB6DR and PB3DR to PB0DR correspond to pins PB19 to PB6 and PB3 to PB0 respectively (description of multiplexed functions are abbreviated here).

When a pin function is general output, if a value is written to PBDRH or PBDRL, the value is output directly from the pin, and if PBDRH or PBDRL is read, the register value is returned directly regardless of the pin state.

When a pin function is general input, if PBDRH or PBDRL is read, the pin state, not the register value, is returned directly. If a value is written to PBDRH or PBDRL, although that value is written into PBDRH or PBDRL, it does not affect the pin state. Table 24.4 summarizes read/write operations of port B data register.

(2) Programming Procedure in User Program Mode

The procedures for download, initialization, and programming are shown in figure 26.13.

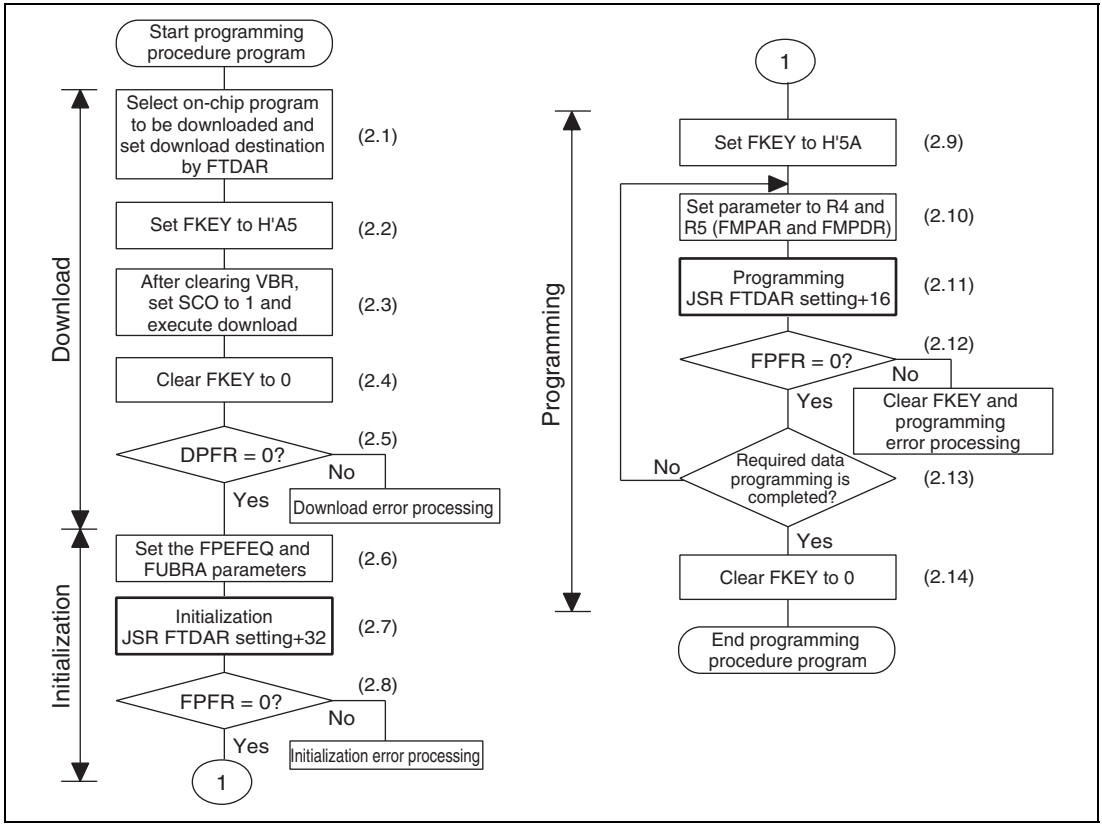


Figure 26.13 Programming Procedure

The details of the programming procedure are described below. The procedure program must be executed in an area other than the flash memory to be programmed. Especially the part where the SCO bit in FCCS is set to 1 for downloading must be executed in the on-chip RAM. Specify Iϕ = Bϕ = Pϕ as the frequency division ratio of an internal clock (Iϕ), a bus clock (Bϕ), and a peripheral clock (Pϕ) through the frequency control register (FRQCR).

After downloading has been completed and the SCO bit has been cleared to 0, FRQCR can be changed to a desired value.

(l) Transition to the Programming/Erasure State

In response to the transition to the programming/erasure state command, the boot program transfers the erasing program and runs it to erase any data in the user MAT and then the user boot MAT. On completion of this erasure, the boot program returns the ACK code and enters the programming/erasure state.

Before sending the programming selection command and data for programming, the host must select the device, clock mode, and new bit rate for the LSI by issuing the device selection command, clock-mode selection command, new-bit-rate selection command, and then initiate the transition to the programming/erasure state by sending the corresponding command to the boot program.

Command	H'40

- Command H'40 (1 byte): Transition to programming/erasure state

Response	H'06

- Response H'06 (1 byte): Response to the transition-to-programming/erasure state command This is returned as ACK when erasure of the user boot MAT and user MAT has succeeded after transfer of the erasure program.

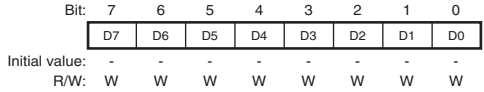
Error response	H'C0	H'51

- Error response H'C0 (1 byte): Error response to the transition-to-programming/erasure state command
- ERROR (1 byte): Error code
  H'51: Erasure error (Erasure did not succeed because of an error.)

Module Name	Register Name	Abbreviation	Number of Bits	Address	Access Size
MTU2S	Timer waveform control register S	TWCRS	8	H'FFFE4A60	8
	Timer output level buffer register S	TOLBRS	8	H'FFFE4A36	8
POE2	Input level control/status register 1	ICSR1	16	H'FFFE5000	16
	Output level control/status register 1	OCSR1	16	H'FFFE5002	16
	Input level control/status register 2	ICSR2	16	H'FFFE5004	16
	Output level control/status register 2	OCSR2	16	H'FFFE5006	16
	Input level control/status register 3	ICSR3	16	H'FFFE5008	16
	Software port output enable register	SPOER	8	H'FFFE500A	8
	Port output enable control register 1	POECR1	8	H'FFFE500B	8
	Port output enable control register 2	POECR2	16	H'FFFE500C	16
CMT	Compare match timer start register	CMSTR	16	H'FFFEC000	16
	Compare match timer control/status register_0	CMCSR_0	16	H'FFFEC002	16
	Compare match counter_0	CMCNT_0	16	H'FFFEC004	16
	Compare match constant register_0	CMCOR_0	16	H'FFFEC006	16
	Compare match timer control/status register_1	CMCSR_1	16	H'FFFEC008	16
	Compare match counter_1	CMCNT_1	16	H'FFFEC00A	16
	Compare match constant register_1	CMCOR_1	16	H'FFFEC00C	16
WDT	Watchdog timer control/status register	WTCSR	16	H'FFFE0000	*
	Watchdog timer counter	WTCNT	16	H'FFFE0002	*
	Watchdog reset control/status register	WRCSR	16	H'FFFE0004	*
SCI (channel 0)	Serial mode register_0	SCSMR_0	8	H'FFFF8000	8
	Bit rate register_0	SCBRR_0	8	H'FFFF8002	8
	Serial control register_0	SCSCR_0	8	H'FFFF8004	8
	Transmit data register_0	SCTDR_0	8	H'FFFF8006	8
	Serial status register_0	SCSSR_0	8	H'FFFF8008	8
	Receive data register_0	SCRDR_0	8	H'FFFF800A	8
	Serial direction control register_0	SCSDCR_0	8	H'FFFF800C	8
	Serial port register_0	SCSPTR_0	8	H'FFFF800E	8
SCI (channel 1)	Serial mode register_1	SCSMR_1	8	H'FFFF8800	8
	Bit rate register_1	SCBRR_1	8	H'FFFF8802	8
	Serial control register_1	SCSCR_1	8	H'FFFF8804	8

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
DMAC	CHCR_2	TC	—	—	RLD	—	—	—	—
		DO	—	—	—	HE	HIE	AM	AL
		DM[1:0]		SM[1:0]		RS[3:0]			
		DL	DS	TB	TS[1:0]		IE	TE	DE
	RSAR_2								
	RDAR_2								
	RDMATCR_2								
	SAR_3								
	DAR_3								
	DMATCR_3								
	CHCR_3	TC	—	—	RLD	—	—	—	—
		DO	—	—	—	HE	HIE	AM	AL
		DM[1:0]		SM[1:0]		RS[3:0]			
		DL	DS	TB	TS[1:0]		IE	TE	DE
	RSAR_3								

Pin Function		Pin State									
		Reset State					Power-Down State				
		Power-On									
Type	Pin Name	Expansion without ROM 8 bits	Expansion without ROM 16 bits	Expansion with ROM	Single-chip	Manual	Software Standby	Sleep	Bus Master-ship Release	Oscillation Stop Detected	POE Function Used
Bus control	$\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$ to $\overline{CS7}$	Z				O	Z*3	O	Z	O	O
	$\overline{BS}$	Z				O	Z*3	O	Z	O	O
	$\overline{RASU}$, $\overline{RASL}$	Z				O	Z*2	O	Z*2	O	O
	$\overline{CASU}$, $\overline{CASL}$	Z				O	Z*2	O	Z*2	O	O
	DQMUU, DQMUL, DQMLU, DQMLL	Z				O	Z*3	O	Z	O	O
	$\overline{AH}$	Z				O	Z*3	O	Z	O	O
	$\overline{AH}$ (PE14)	Z				O	Z (MZIZEH in HCPCR = 0) Z*3 (MZIZEH in HCPCR = 1)	O	Z	O*7	O
	$\overline{REFOUT}$	Z				O	H/Z*1	O	O	Z	H/Z*1
	$\overline{FRAME}$	Z				O	Z*3	O	Z	O	O
	RDWR	Z				O	Z*3	O	Z	O	O
	$\overline{RD}$	H		Z		O	Z*3	O	Z	O	O
	$\overline{WRHH}$, $\overline{WRHL}$	Z		H		O	Z*3	O	Z	O	O
	$\overline{WRH}$, $\overline{WRL}$	H		Z		O	Z*3	O	Z	O	O
	CKE	Z				O	Z*2	O	Z*2	O	O
DMAC	DREQ0 (PD24), DREQ1 (PD25)	Z				I	Z	I	I	I/O*5	I
	DREQ0 (PE0), DREQ1 (PE2)	Z				I	Z	I	I	I*8	I
	DREQ2, DREQ3	Z				I	Z	I	I	I	I
	DACK0 (PD26), DACK1 (PD27)	Z				O	Z (MZIZDH in HCPCR = 0) O*1 (MZIZDH in HCPCR = 1)	O	O	O*5	O

Item	Page	Revision (See Manual for Details)
25.3.10 USBEP1 Data Register (USBEPDR1)	1360	Amended  **Bit** / **Bit Name** / **Initial Value** / **R/W** / **Description** 7 to 0 / D7 to D0 / Undefined / R / Data register for endpoint 1 transfer ~~Note: * 7 to 0 bits for DMA or DTC transfer.~~
25.3.11 USBEP2 Data Register (USBEPDR2)	1361	Amended  **Bit** / **Bit Name** / **Initial Value** / **R/W** / **Description** 7 to 0 / D7 to D0 / Undefined / W / Data register for endpoint 2 transfer ~~Note: * 7 to 0 bits for DMA or DTC transfer.~~
25.3.18 USBDMA Transfer Setting Register (USBDMAR)	1369	Added Notes: 1. Before setting this bit, set the DME bit in DMAOR to start DMA transfer or set the DTCE0 bit in DTCERA to start DTC transfer. If the DME bit in DMAOR and the DTCE0 bit in DTCERA are not set, an EP2-FIFO empty DTC transfer end interrupt (TXF bit in USDTENDRR) is generated. 2. Before setting this bit, set the DME bit in DMAOR to start DMA transfer or set the DTCE1 bit in DTCERA to start DTC transfer. If the DME bit in DMAOR and the DTCE1 bit in DTCERA are not set, an EP1-FIFO full DTC transfer end interrupt (RXF bit in USDTENDRR) is generated.
Table 25.3 Interrupt Sources	1371	Amended **Register** / **Bit** / **Transfer Type** / **DMAC/DTC Activation by USB Request** USBIFR0 / 6 / Bulk-OUT (EP1) / USBRXI*1 5 / Bulk-IN (EP2) / × 4 / / USBTXI*2
25.5.1 Initial Settings	1372	Added