Renesas Electronics America Inc - R5F72865N100FP#U2 Datasheet

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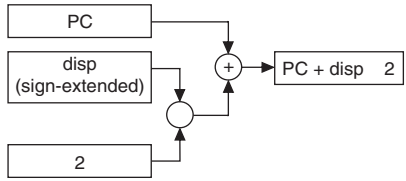
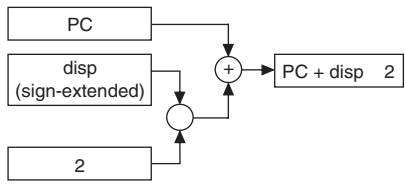
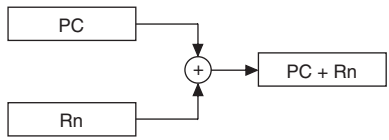
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH2A
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, SCI, SSU, USB
Peripherals	DMA, PWM, WDT
Number of I/O	101
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x12b, 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f72865n100fp-u2

Addressing Mode	Instruction Format	Effective Address Calculation	Equation
PC relative	disp:8	The effective address is the sum of PC value and the value that is obtained by doubling the sign-extended 8-bit displacement (disp). 	PC + disp × 2
	disp:12	The effective address is the sum of PC value and the value that is obtained by doubling the sign-extended 12-bit displacement (disp). 	PC + disp × 2
	Rn	The effective address is the sum of PC value and Rn. 	PC + Rn

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 8	STC[2:0]	011	R/W	Bus Clock (Bφ) Frequency Division Ratio These bits specify the frequency division ratio of the bus clock. 000: × 1 001: × 1/2 010: Setting prohibited 011: × 1/4 100: Setting prohibited 101: × 1/8 Others: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	IFC[2:0]	011	R/W	Internal Clock (Iφ) Frequency Division Ratio These bits specify the frequency division ratio of the internal clock. 000: × 1 001: × 1/2 010: Setting prohibited 011: × 1/4 100: Setting prohibited 101: × 1/8 Others: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

7.2 Input/Output Pin

Table 7.1 shows the pin configuration of the UBC.

Table 7.1 Pin Configuration

Pin Name	Symbol	I/O	Function
UBC trigger	$\overline{\text{UBCTRG}}$	Output	Indicates that a setting condition is satisfied on either channel 0, 1, 2, or 3 of the UBC.

Bit	Bit Name	Initial Value	R/W	Description
21	SZSEL	0	R/W	MPX-I/O Interface Bus Width Specification Specifies an address to select the bus width when the BSZ[1:0] of CS5BCR are specified as 11. This bit is valid only when area 5 is specified as MPX-I/O. Always set this bit to 0 in the SH7285 and SH7243. 0: Selects the bus width by address A14 1: Selects the bus width by address A21 The relationship between the SZSEL bit and bus width selected by A14 or A21 are summarized below.

SZSEL	A14	A21	Bus Width
0	0	Not affected	8 bits
0	1	Not affected	16 bits
1	Not affected	0	8 bits
1	Not affected	1	16 bits

20	MPXW	0	R/W	MPX-I/O Interface Address Wait This bit setting is valid only when area 5 is specified as MPX-I/O. Specifies the address cycle insertion wait for MPX-I/O interface. 0: Inserts no wait cycle 1: Inserts 1 wait cycle
	BAS	0	R/W	SRAM with Byte Selection Byte Access Select This bit setting is valid only when area 5 is specified as SRAM with byte selection. Specifies the $\overline{\text{WRxx}}$ and RD/$\overline{\text{WR}}$ signal timing when the SRAM interface with byte selection is used. 0: Asserts the $\overline{\text{WRxx}}$ signal at the read timing and asserts the RD/$\overline{\text{WR}}$ signal during the write access cycle. 1: Asserts the $\overline{\text{WRxx}}$ signal during the read access cycle and asserts the RD/$\overline{\text{WR}}$ signal at the write timing.
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

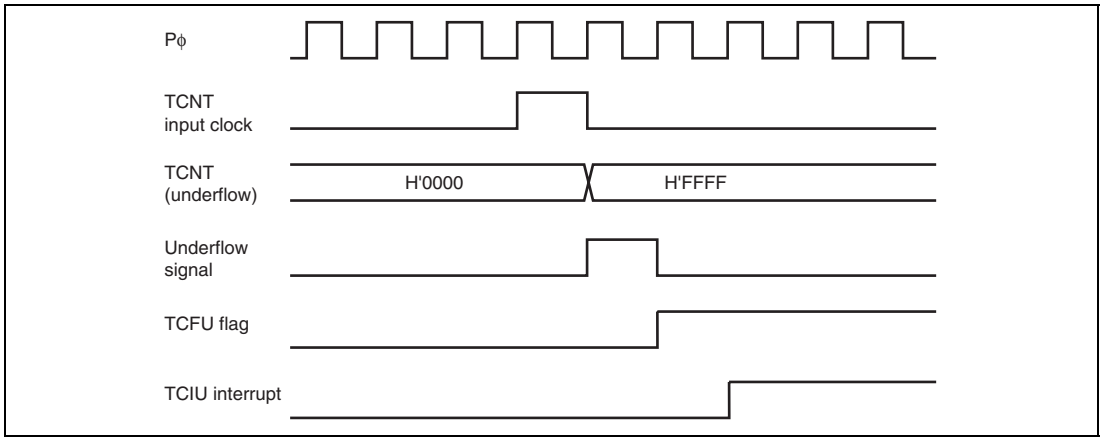


Figure 11.114 TCIU Interrupt Setting Timing

(4) Status Flag Clearing Timing

After a status flag is read as 1 by the CPU, it is cleared by writing 0 to it. When the DMAC is activated, the flag is cleared automatically. Figures 11.115 and 116 show the timing for status flag clearing by the CPU, and figure 11.117 shows the timing for status flag clearing by the DMAC.

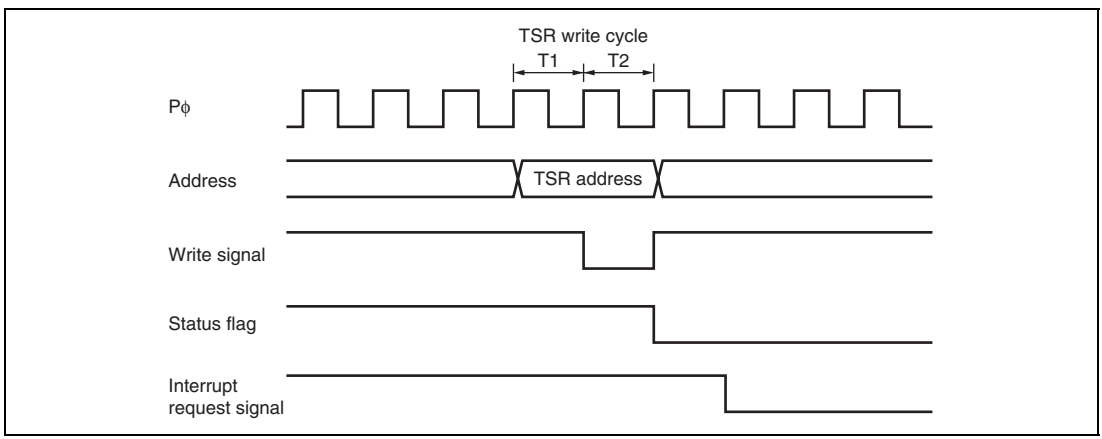


Figure 11.115 Timing for Status Flag Clearing by CPU (Channels 0 to 4)

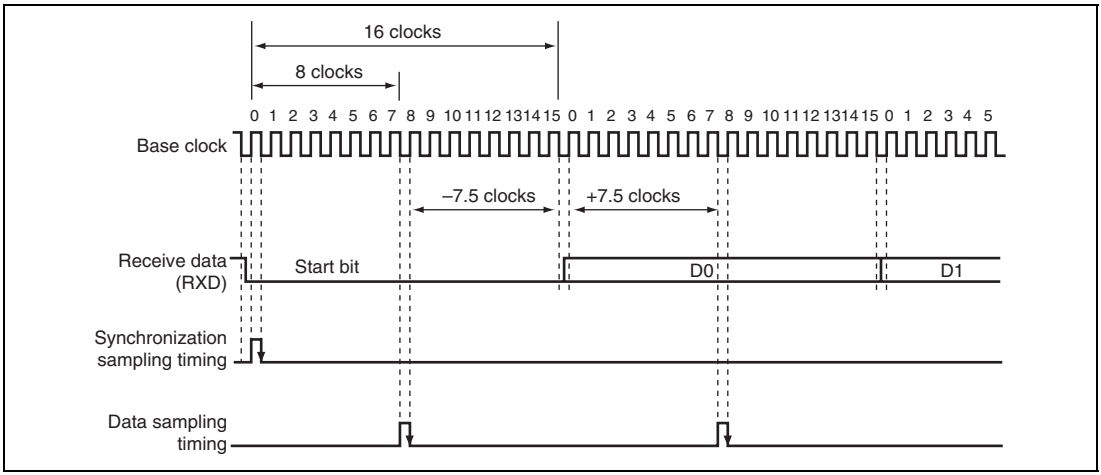


Figure 16.21 Receive Data Sampling Timing in Asynchronous Mode

The receive margin in asynchronous mode can therefore be expressed as shown in equation 1.

Equation 1:

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5) F - \frac{|D - 0.5|}{N} (1+F) \right| \times 100\ \%$$

Where: M: Receive margin (%)
N: Ratio of bit rate to clock (N = 16)
D: Clock duty (D = 0 to 1.0)
L: Frame length (L = 9 to 12)
F: Absolute deviation of clock frequency

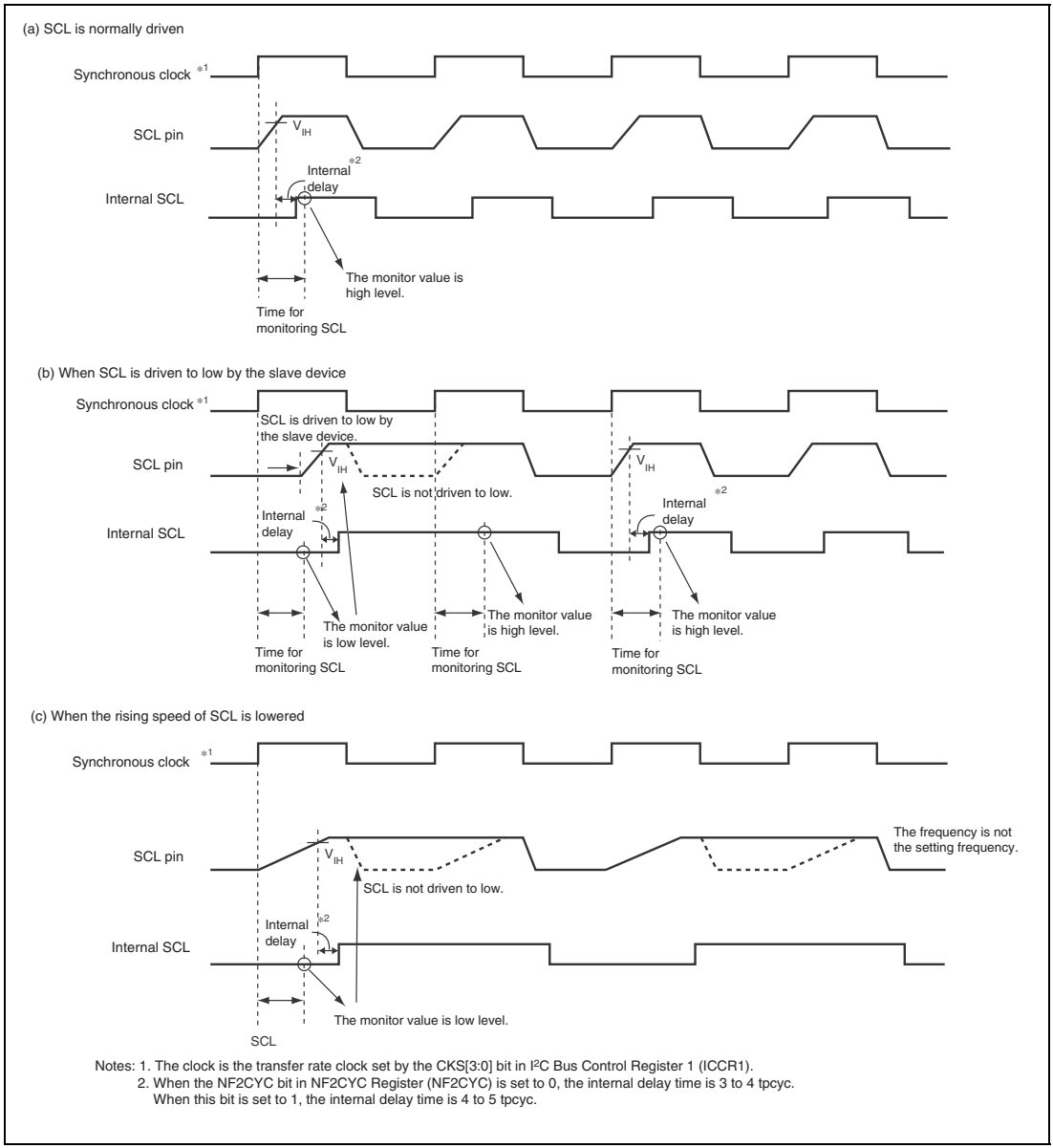
From equation 1, if F = 0 and D = 0.5, the receive margin is 46.875%, as given by equation 2.

Equation 2:

When D = 0.5 and F = 0:

$M = (0.5 - 1/(2 \times 16)) \times 100\%$
$= 46.875\%$

This is a theoretical value. A reasonable margin to allow in system designs is 20% to 30%.



Notes: 1. The clock is the transfer rate clock set by the CKS[3:0] bit in I²C Bus Control Register 1 (ICCR1).
2. When the NF2CYC bit in NF2CYC Register (NF2CYC) is set to 0, the internal delay time is 3 to 4 tpcyc. When this bit is set to 1, the internal delay time is 4 to 5 tpcyc.

Figure 19.23 Bit Synchronous Circuit Timing

20.3.1 A/D Control Registers 0 to 2 (ADCR_0 to ADCR_2)

ADCR is an 8-bit readable/writable register that selects A/D conversion mode and others.

Bit:	7	6	5	4	3	2	1	0
	ADST	ADCS	ACE	ADIE	-	-	TRGE	EXTRG
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	ADST	0	R/W	A/D Start When this bit is cleared to 0, A/D conversion is stopped and the A/D converter enters the idle state. When this bit is set to 1, A/D conversion is started. In single-cycle scan mode, this bit is automatically cleared to 0 when A/D conversion ends on the selected single channel. In continuous scan mode, A/D conversion is continuously performed for the selected channels in sequence until this bit is cleared by software, a reset, or in software standby mode.
6	ADCS	0	R/W	A/D Continuous Scan Selects either a single-cycle or a continuous scan in scan mode. This bit is valid only when scan mode is selected. 0: Single-cycle scan 1: Continuous scan When changing the operating mode, first clear the ADST bit to 0.
5	ACE	0	R/W	Automatic Clear Enable Enables or disables the automatic clearing of ADDR after ADDR is read by the CPU or DMAC. When this bit is set to 1, ADDR is automatically cleared to H'0000 after the CPU or DMAC reads ADDR. This function allows the detection of any renewal failures of ADDR. 0: Automatic clearing of ADDR after being read is disabled. 1: Automatic clearing of ADDR after being read is enabled.

- Port A Control Register L3 (PACRL3)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	PA11MD[2:0]			-	PA10MD[2:0]			-	PA9MD[2:0]			-	PA8MD[2:0]		
Initial value:	0	0	0	0*	0	0	0	0*	0	0	0	0	0	0	0	0*
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Note: * The initial value is 1 during the on-chip ROM disabled 32-bit external extension mode

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	PA11MD [2:0]	000*	R/W	PA11 Mode Select the function of the PA11/$\overline{\text{WRHH}}$ /DQMUU/$\overline{\text{AH}}$ pin. 000: PA11 I/O (port) 001: $\overline{\text{WRHH}}$ output, DQMUU output and $\overline{\text{AH}}$ output (BSC) 010: Setting prohibited 011: Setting prohibited 100: Setting prohibited 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

- Port B Control Register L2 (PBCRL2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	PB7MD[2:0]			-	PB6MD[2:0]			-	-	-	-	-	-	-	-
Initial value:	0	0	0	0*	0	0	0	0*	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Note: * The initial value is 1 during the on-chip ROM disabled external extension mode.

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	PB7MD[2:0]	000*	R/W	PB7 Mode Select the function of the PB7/A19/$\overline{\text{BREQ}}$/IRQ6/$\overline{\text{POE4}}$/TXD0 pin. 000: PB7 I/O (port) 001: A19 output (BSC) 010: $\overline{\text{BREQ}}$ output (BSC) 011: IRQ6 input (INTC) 100: $\overline{\text{POE4}}$ I/O (POE2) 101: TXD0 output (SCI) 110: Setting prohibited 111: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6 to 4	PC13MD[2:0]	000*	R/W	PC13 Mode Select the function of the PC13/A13/IRQ0 pin. 000: PC13 I/O (port) 001: A13 output (BSC) 010: Setting prohibited 011: IRQ0 input (INTC) 100: Setting prohibited 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	PC12MD[2:0]	000*	R/W	PC12 Mode Select the function of the PC12/A12 pin. 000: PC12 I/O (port) 001: A12 output (BSC) 010: Setting prohibited 011: Setting prohibited 100: Setting prohibited 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited

Note: * The initial value is 1 during the on-chip ROM disabled external extension mode.

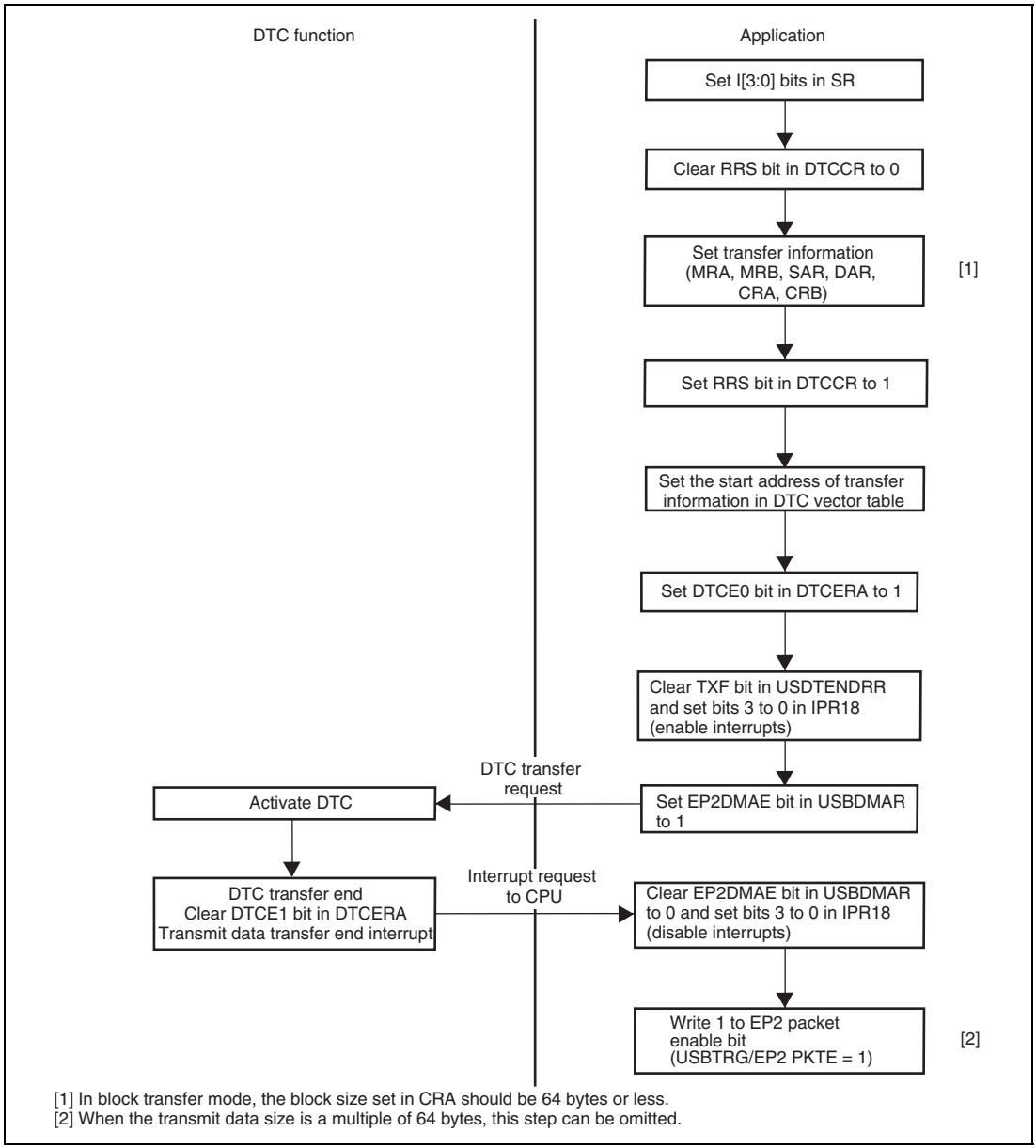


Figure 25.26 Example of DTC Transfer for Bulk-IN Transfer (EP2) (When Transmit Data Size is Determined Before Receiving IN Token)

(2) Programming/Erasing Initialization

The on-chip programming/erasing program to be downloaded includes the initialization program.

The specified period pulse must be applied when programming or erasing. The specified pulse width is made by the method in which wait loop is configured by the CPU instruction. The operating frequency of the CPU must be set. Since the user branch function is supported, the user branch destination address must be set.

The initial program is set as a parameter of the programming/erasing program which has downloaded these settings.

(2.1) Flash Programming/Erasing Frequency Parameter (FPEFEQ: General Register R4 of CPU)

This parameter sets the operating frequency of the CPU.

For the operating frequency of this LSI, see section 31.3.1, Clock Timing.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

(2) Programming Procedure in User Program Mode

The procedures for download, initialization, and programming are shown in figure 26.13.

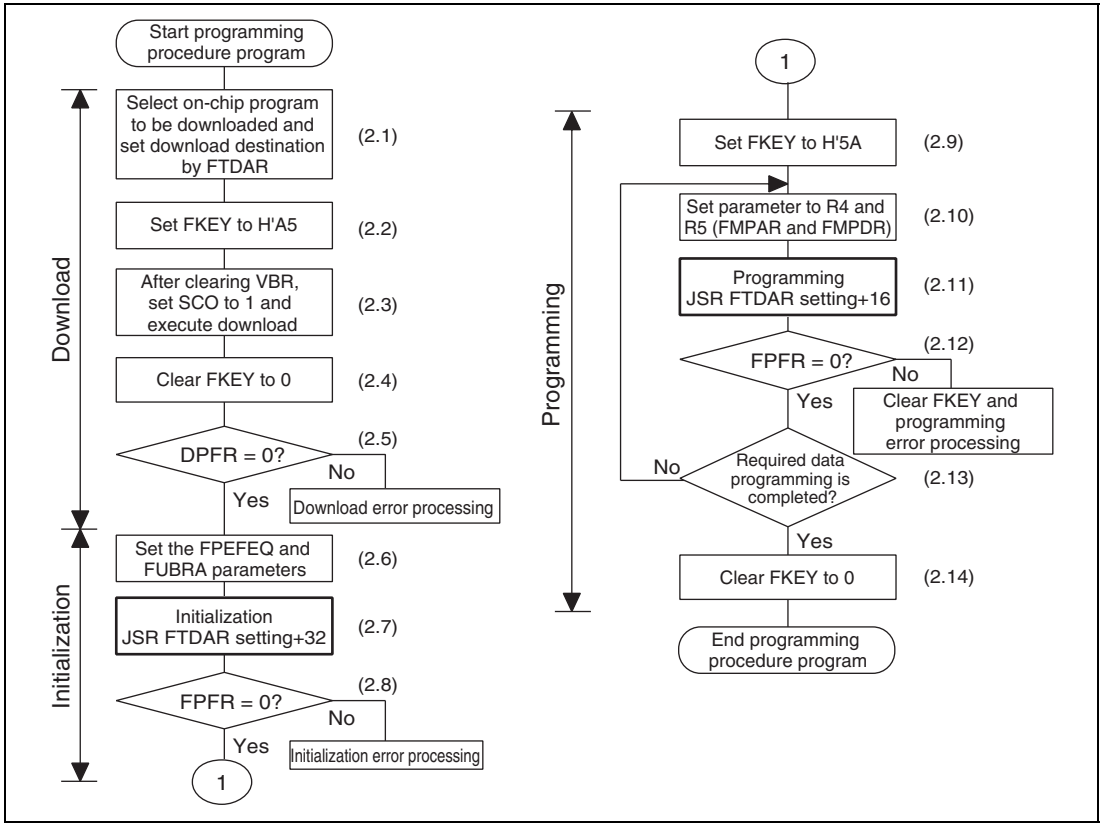


Figure 26.13 Programming Procedure

The details of the programming procedure are described below. The procedure program must be executed in an area other than the flash memory to be programmed. Especially the part where the SCO bit in FCCS is set to 1 for downloading must be executed in the on-chip RAM. Specify Iϕ = Bϕ = Pϕ as the frequency division ratio of an internal clock (Iϕ), a bus clock (Bϕ), and a peripheral clock (Pϕ) through the frequency control register (FRQCR).

After downloading has been completed and the SCO bit has been cleared to 0, FRQCR can be changed to a desired value.

(2) Interrupts during Programming/Erasing

Do not generate NMI, IRQ, and all other interrupts during programming/erasing of the downloaded on-chip program.

26.7.3 Other Notes

(1) Download Time of On-Chip Program

The programming program that includes the initialization routine and the erasing program that includes the initialization routine are each 3 Kbytes or less. Accordingly, when the CPU clock frequency is 40 MHz, the download for each program takes approximately 10 ms at maximum.

(2) User Branch Processing Intervals

The intervals for executing the user branch processing differs in programming and erasing. The processing phase also differs. Table 26.11 lists the maximum and minimum intervals for initiating the user branch processing when the CPU clock frequency is 40 MHz.

Table 26.11 Initiation Intervals of User Branch Processing

Processing Name	Maximum Interval
Programming	1.6 ms
Erasing	12 ms

However, when operation is done with CPU clock of 40 MHz, maximum and minimum values of the time until first user branch processing are as shown in table 26.12.

Table 26.12 Initial User Branch Processing Time

Processing Name	Maximum
Programming	1.6 ms
Erasing	12 ms

(3) Write to Flash-Memory Related Registers by DMAC

While an instruction in on-chip RAM is being executed, the DMAC can write to the SCO bit in FCCS that is used for a download request or FMATS that is used for MAT switching. Make sure that these registers are not accidentally written to, otherwise an on-chip program may be downloaded and destroy RAM or a MAT switchover may occur and the CPU get out of control.

(2) Bit-Rate Matching State

In bit-rate matching, the boot program measures the low-level intervals in a signal carrying H'00 data that is transmitted by the host, and calculates the bit rate from this. The bit rate can be changed by the new-bit-rate selection command. On completion of bit-rate matching, the boot program goes to the inquiry and selection state. The sequence of processing in bit-rate matching is shown in figure 26.22.

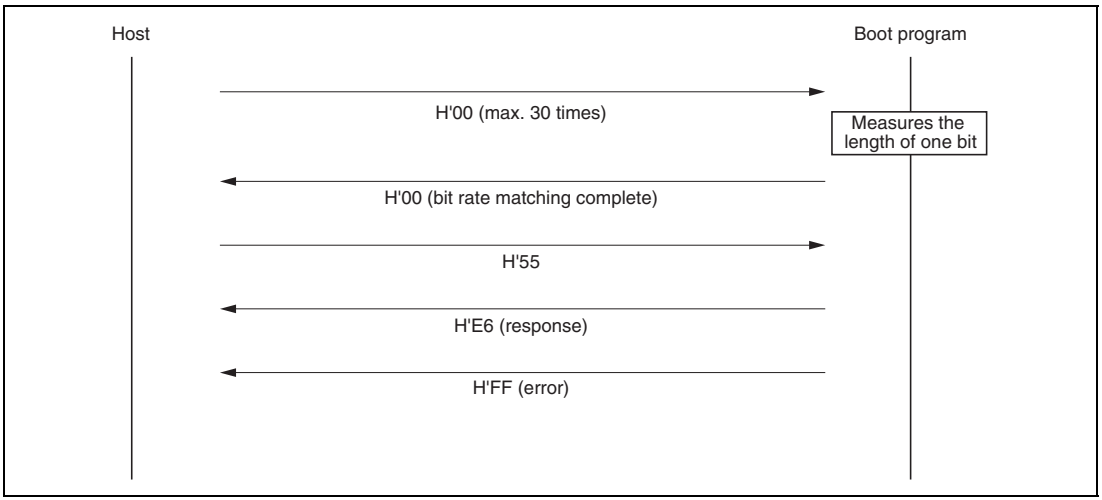


Figure 26.22 Sequence of Bit-Rate Matching

(3) Communications Protocol

Formats in the communications protocol between the host and boot program after completion of the bit-rate matching are as follows.

1. One-character command or one-character response

   A command or response consisting of a single character used for an inquiry or the ACK code indicating normal completion.
2. n-character command or n-character response

   A command or response that requires n bytes of data, which is used as a selection command or response to an inquiry. The length of programming data is treated separately below.
3. Error response

   Response to a command in case of an error: two bytes, consisting of the error response and error code.

Bit	Bit Name	Initial Value	R/W	Description
2	RAMWE2	1	R/W	RAM Write Enable 2 (corresponding RAM addresses: H'FFF84000 to H'FFF85FFF) 0: On-chip RAM write disabled 1: On-chip RAM write enabled Note: Write 1 to this bit in the SH7243.
1	RAMWE1	1	R/W	RAM Write Enable 1 (SH7286/SH7285: H'FFF82000 to H'FFF83FFF, SH7243: H'FFF82000 to H'FFF82FFF) 0: On-chip RAM write disabled 1: On-chip RAM write enabled
0	RAMWE0	1	R/W	RAM Write Enable 0 (corresponding RAM addresses: H'FFF80000 to H'FFF81FFF) 0: On-chip RAM write disabled 1: On-chip RAM write enabled

30.2 Register Bits

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
CPG	FRQCR	—	—	—	—	—	STC[2:0]		
		—	IFC[2:0]			—	PFC[2:0]		
	MCLKCR	—	—	—	—	—	—	MSDIVS[1:0]	
	ACLKCR	—	—	—	—	—	—	ASDIVS[1:0]	
	OSCCR	—	—	—	—	—	OSCSTOP		OSCERS
INTC	ICR0	NMIL	—	—	—	—	—	—	NMIE
		—	—	—	—	—	—	—	—
	ICR1	IRQ71S	IRQ70S	IRQ61S	IRQ60S	IRQ51S	IRQ50S	IRQ41S	IRQ40S
		IRQ31S	IRQ30S	IRQ21S	IRQ20S	IRQ11S	IRQ10S	IRQ01S	IRQ00S
	IRQRR	—	—	—	—	—	—	—	—
		IRQ7F	IRQ6F	IRQ5F	IRQ4F	IRQ3F	IRQ2F	IRQ1F	IRQ0F
	IBCR	E15	E14	E13	E12	E11	E10	E9	E8
		E7	E6	E5	E4	E3	E2	E1	—
	IBNR	BE[1:0]		BOVE	—	—	—	—	—
		—	—	—	—	BN[3:0]			
	IPR01	IRQ0				IRQ1			
		IRQ2				IRQ3			
	IPR02	IRQ4				IRQ5			
		IRQ6				IRQ7			
	IPR05	—	—	—	—	—	—	—	—
		ADI0				ADI1			
	IPR06	DMAC0				DMAC1			
		DMAC2				DMAC3			
	IPR07	DMAC4				DMAC5			
		DMAC6				DMAC7			
	IPR08	CMT0				CMT1			
		BSC				WDT			
	IPR09	MTU0				MTU0			
		MTU1				MTU1			
	IPR10	MTU2				MTU2			
		MTU3				MTU3			
	IPR11	MTU4				MTU4			
		MTU5				POE2			

31.2 DC Characteristics

Tables 31.2 and 31.3 list DC characteristics.

Table 31.2 DC Characteristics (1) [Common Items]

Conditions: Ta = −20°C to +85°C (Consumer specifications),
Ta = −40°C to +85°C (Industrial specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power supply voltage		V_{CC}	3.0	5.0	5.5	V	
Analog power supply voltage		AV_{CC}	4.5	5.0	5.5	V	
USB power supply*3		DrV_{CC}	3.0	3.3	3.6	V	
Supply current*1	Normal operation	I_{CC}	—	155	180	mA	Iϕ = 100 MHz Bϕ = 50 MHz Pϕ = 50 MHz (SH7286, SH7285)
		I_{CC}	—	125	140	mA	Iϕ = 100 MHz Bϕ = 50 MHz Pϕ = 50 MHz (SH7243)
	Software standby mode	I_{stby}	—	10	20	mA	V_{CC} = 5.0 V
	Sleep mode	I_{sleep}	—	80	120	mA	SH7286 SH7285
				70	100		SH7243
Input leakage current	All input pins	$\|I_{in}\|$	—	—	1	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
Three-state leakage current	Input/output pins, all output pins (off state)	$\|I_{STI}\|$	—	—	1	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
Input capacitance	All pins	C_{in}	—	—	20	pF	
Analog power supply current	During A/D or D/A conversion	AI_{CC}	—	3.0	5.0	mA	Per 1 module
	Waiting for A/D or D/A conversion		—	30	50	µA	Per 1 module