Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	SSC, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	52KB (52K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc858ca-13ffi-ac

1 Summary of Features

The XC858 has the following features:

- High-performance XC800 Core
  - compatible with standard 8051 processor
  - two clocks per machine cycle architecture (for memory access without wait state)
  - two data pointers
- On-chip memory
  - 8 Kbytes of Boot ROM
  - 256 bytes of RAM
  - 3 Kbytes of XRAM
  - 64/52/36 Kbytes of Flash;
    (includes memory protection strategy)
- I/O port supply at 5.0 V and core logic supply at 2.5 V (generated by embedded voltage regulator)

(more features on next page)

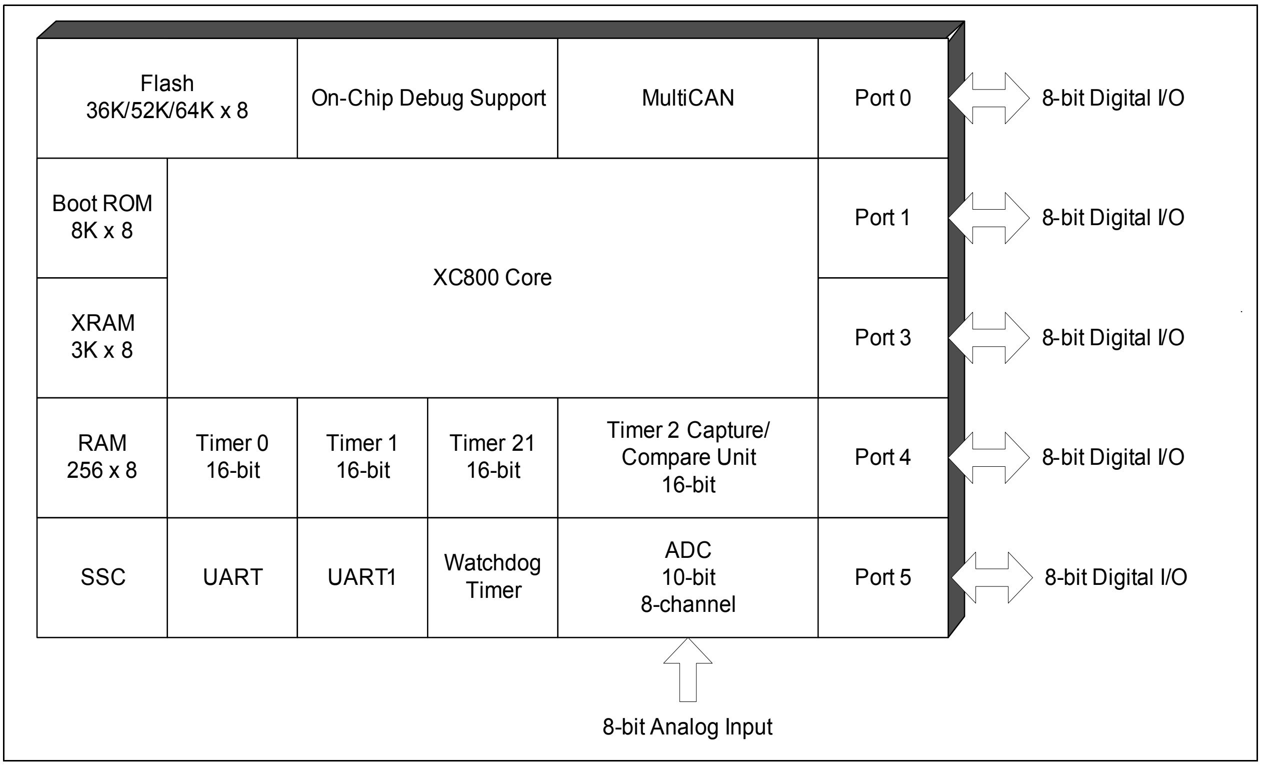


Figure 1 XC858 Functional Units

2 General Device Information

Chapter 2 contains the block diagram, pin configurations, definitions and functions of the XC858.

2.1 Block Diagram

The block diagram of the XC858 is shown in **Figure 2**.

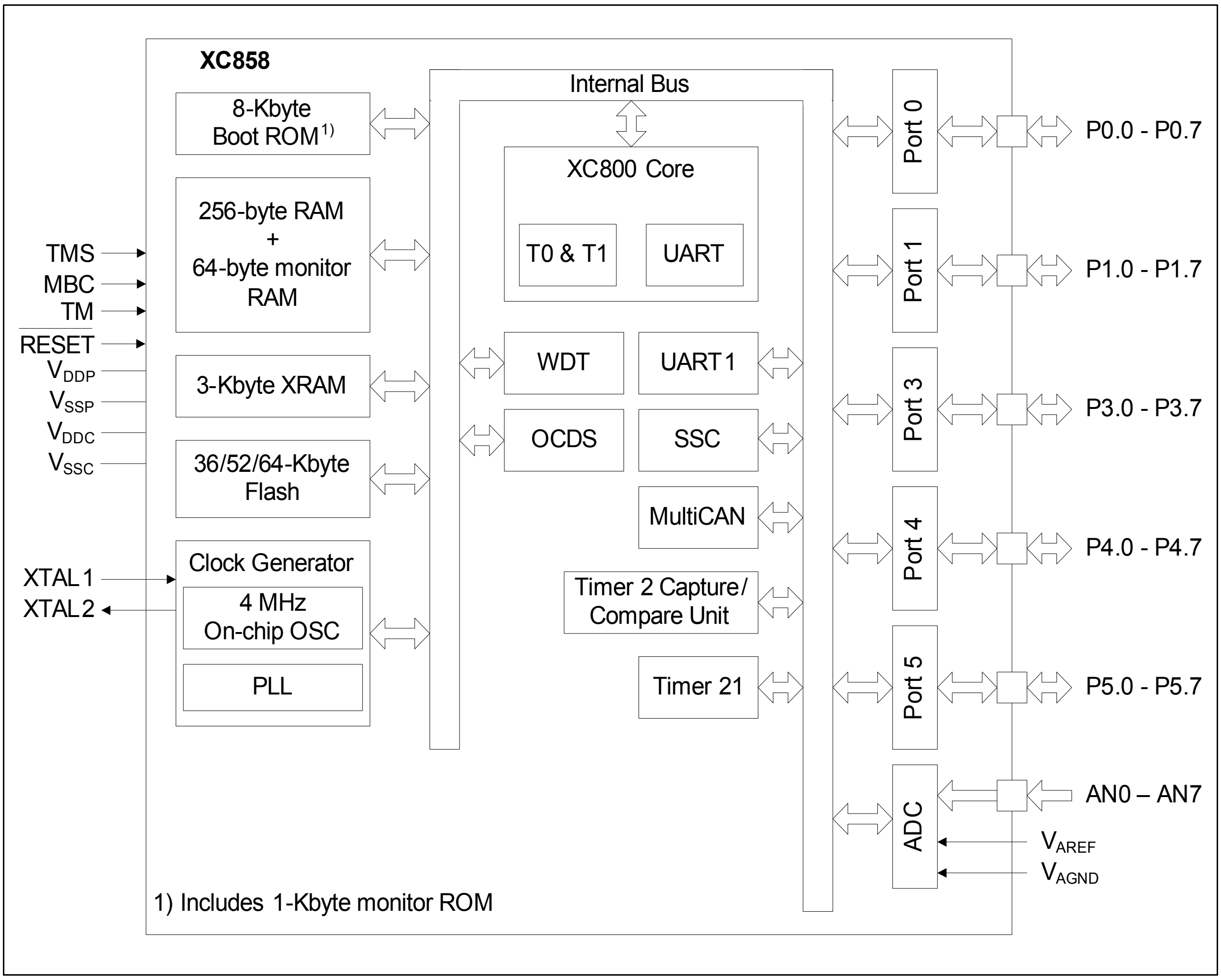


Figure 2 XC858 Block Diagram

General Device Information

General Device Information

3.2 Memory Organization

The XC858 CPU operates in the following address spaces:

- 8 Kbytes of Boot ROM program memory
- 256 bytes of internal RAM data memory
- 3 Kbytes of XRAM memory
  (XRAM can be read/written as program memory or external data memory)
- A 128-byte Special Function Register area
- 64/52/36 Kbytes of Flash program memory (Flash devices)

Figure 6, **Figure 7** and **Figure 8** illustrates the memory address spaces of the XC858 with 64Kbytes, 52Kbytes and 36Kbytes embedded Flash respectively.

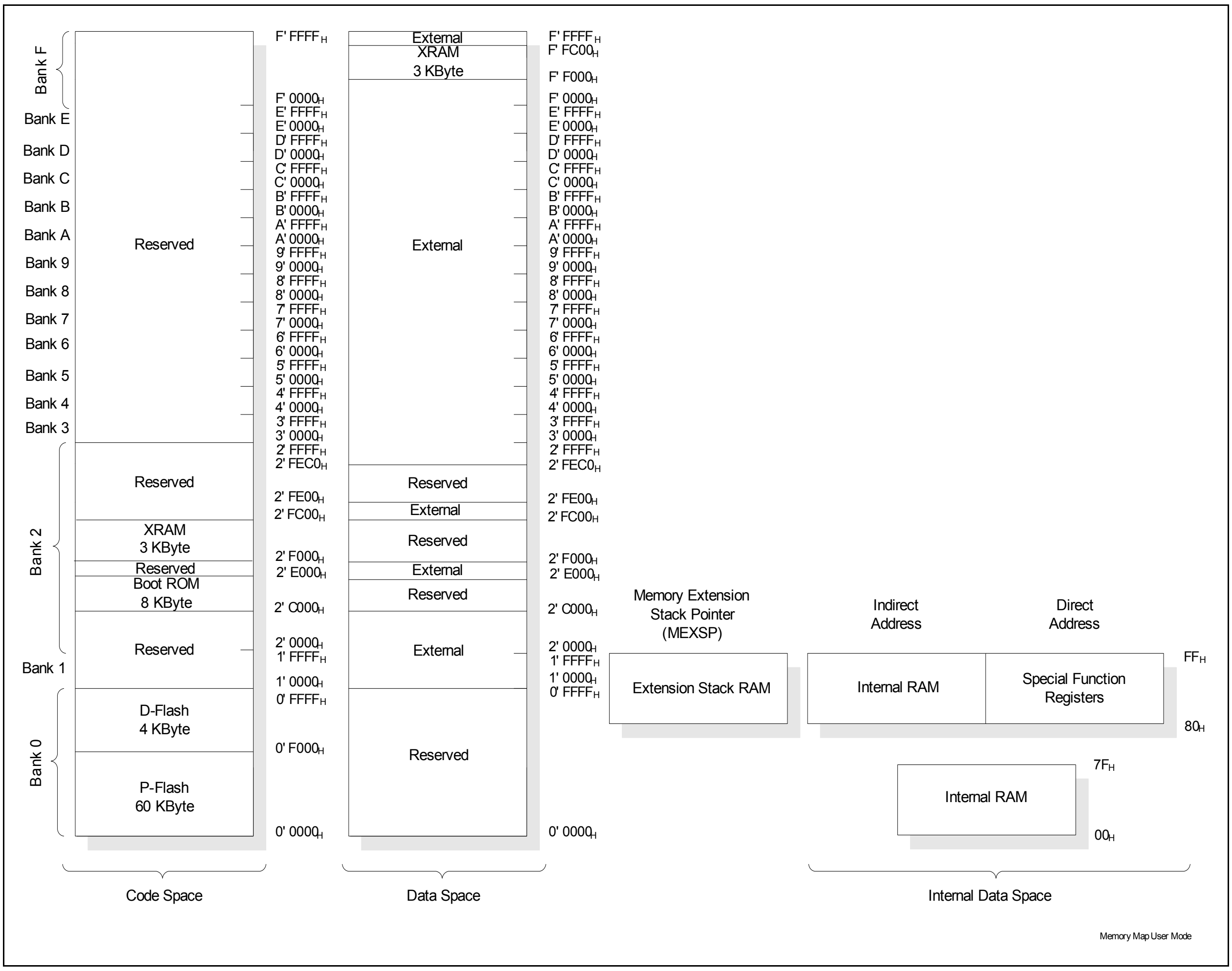


Figure 6 Memory Map of XC858 with 64K Flash Memory in user mode

3.2.2 Special Function Register

The Special Function Registers (SFRs) occupy direct internal data memory space in the range 80_H to FF_H. All registers, except the program counter, reside in the SFR area. The SFRs include pointers and registers that provide an interface between the CPU and the on-chip peripherals. As the 128-SFR range is less than the total number of registers required, address extension mechanisms are required to increase the number of addressable SFRs. The address extension mechanisms include:

- Mapping
- Paging

3.2.2.1 Address Extension by Mapping

Address extension is performed at the system level by mapping. The SFR area is extended into two portions: the standard (non-mapped) SFR area and the mapped SFR area. Each portion supports the same address range 80_H to FF_H, bringing the number of addressable SFRs to 256. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit RMAP in the system control register SYSCON0 at address $8F_H$. To access SFRs in the mapped area, bit RMAP in SFR SYSCON0 must be set. Alternatively, the SFRs in the standard area can be accessed by clearing bit RMAP. The SFR area can be selected as shown in **Figure 9**.

As long as bit RMAP is set, the mapped SFR area can be accessed. This bit is not cleared automatically by hardware. Thus, before standard/mapped registers are accessed, bit RMAP must be cleared/set, respectively, by software.

Table 8 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CF$_H$	**ADC_ETRCR** **Reset: 00$_H$** External Trigger Control Register	Bit Field	SYNEN1	SYNEN0	ETRSEL1			ETRSEL0		
		Type	rw	rw	rw			rw		
RMAP = 0, PAGE 1										
CA$_H$	**ADC_CHCTR0** **Reset: 00$_H$** Channel Control Register 0	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
CB$_H$	**ADC_CHCTR1** **Reset: 00$_H$** Channel Control Register 1	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
CC$_H$	**ADC_CHCTR2** **Reset: 00$_H$** Channel Control Register 2	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
CD$_H$	**ADC_CHCTR3** **Reset: 00$_H$** Channel Control Register 3	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
CE$_H$	**ADC_CHCTR4** **Reset: 00$_H$** Channel Control Register 4	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
CF$_H$	**ADC_CHCTR5** **Reset: 00$_H$** Channel Control Register 5	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
D2$_H$	**ADC_CHCTR6** **Reset: 00$_H$** Channel Control Register 6	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
D3$_H$	**ADC_CHCTR7** **Reset: 00$_H$** Channel Control Register 7	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
RMAP = 0, PAGE 2										
CA$_H$	**ADC_RESR0L** **Reset: 00$_H$** Result Register 0 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CB$_H$	**ADC_RESR0H** **Reset: 00$_H$** Result Register 0 High	Bit Field	RESULT							
		Type	rh							
CC$_H$	**ADC_RESR1L** **Reset: 00$_H$** Result Register 1 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CD$_H$	**ADC_RESR1H** **Reset: 00$_H$** Result Register 1 High	Bit Field	RESULT							
		Type	rh							
CE$_H$	**ADC_RESR2L** **Reset: 00$_H$** Result Register 2 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CF$_H$	**ADC_RESR2H** **Reset: 00$_H$** Result Register 2 High	Bit Field	RESULT							
		Type	rh							
D2$_H$	**ADC_RESR3L** **Reset: 00$_H$** Result Register 3 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
D3$_H$	**ADC_RESR3H** **Reset: 00$_H$** Result Register 3 High	Bit Field	RESULT							
		Type	rh							
RMAP = 0, PAGE 3										

Table 8 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CD_H	**ADC_CHINPR** **Reset: 00_H** Channel Interrupt Node Pointer Register	Bit Field	CHINP 7	CHINP 6	CHINP 5	CHINP 4	CHINP 3	CHINP 2	CHINP 1	CHINP 0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
CE_H	**ADC_EVINFR** **Reset: 00_H** Event Interrupt Flag Register	Bit Field	EVINF 7	EVINF 6	EVINF 5	EVINF 4	0		EVINF 1	EVINF 0
		Type	rh	rh	rh	rh	r		rh	rh
CF_H	**ADC_EVINCR** **Reset: 00_H** Event Interrupt Clear Flag Register	Bit Field	EVINC 7	EVINC 6	EVINC 5	EVINC 4	0		EVINC 1	EVINC 0
		Type	w	w	w	w	r		w	w
$D2_H$	**ADC_EVINSR** **Reset: 00_H** Event Interrupt Set Flag Register	Bit Field	EVINS 7	EVINS 6	EVINS 5	EVINS 4	0		EVINS 1	EVINS 0
		Type	w	w	w	w	r		w	w
$D3_H$	**ADC_EVINPR** **Reset: 00_H** Event Interrupt Node Pointer Register	Bit Field	EVINP 7	EVINP 6	EVINP 5	EVINP 4	0		EVINP 1	EVINP 0
		Type	rw	rw	rw	rw	r		rw	rw
RMAP = 0, PAGE 6										
CA_H	**ADC_CRCR1** **Reset: 00_H** Conversion Request Control Register 1	Bit Field	CH7	CH6	CH5	CH4	0			
		Type	rwh	rwh	rwh	rwh	r			
CB_H	**ADC_CRPR1** **Reset: 00_H** Conversion Request Pending Register 1	Bit Field	CHP7	CHP6	CHP5	CHP4	0			
		Type	rwh	rwh	rwh	rwh	r			
CC_H	**ADC_CRMR1** **Reset: 00_H** Conversion Request Mode Register 1	Bit Field	Rsv	LDEV	CLRP ND	SCAN	ENSI	ENTR	0	ENGT
		Type	r	w	w	rw	rw	rw	r	rw
CD_H	**ADC_QMR0** **Reset: 00_H** Queue Mode Register 0	Bit Field	CEV	TREV	FLUS H	CLRV	0	ENTR	0	ENGT
		Type	w	w	w	w	r	rw	r	rw
CE_H	**ADC_QSR0** **Reset: 20_H** Queue Status Register 0	Bit Field	Rsv	0	EMPT Y	EV	0		FILL	
		Type	r	r	rh	rh	r		rh	
CF_H	**ADC_Q0R0** **Reset: 00_H** Queue 0 Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
$D2_H$	**ADC_QBUR0** **Reset: 00_H** Queue Backup Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
$D2_H$	**ADC_QINR0** **Reset: 00_H** Queue Input Register 0	Bit Field	EXTR	ENSI	RF	0		REQCHNR		
		Type	w	w	w	r		w		

Table 11 UART1 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
$C8_H$	**SCON** **Reset: 00_H** Serial Channel Control Register	Bit Field	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
		Type	rw	rw	rw	rw	rw	rwh	rwh	rwh
$C9_H$	**SBUF** **Reset: 00_H** Serial Data Buffer Register	Bit Field	VAL							
		Type	rwh							
CA_H	**BCON** **Reset: 00_H** Baud Rate Control Register	Bit Field	0				BRPRE			R
		Type	r				rw			rw
CB_H	**BG** **Reset: 00_H** Baud Rate Timer/Reload Register	Bit Field	BR_VALUE							
		Type	rwh							
CC_H	**FDCON** **Reset: 00_H** Fractional Divider Control Register	Bit Field	0					NDOV	FDM	FDEN
		Type	r					rwh	rw	rw
CD_H	**FDSTEP** **Reset: 00_H** Fractional Divider Reload Register	Bit Field	STEP							
		Type	rw							
CE_H	**FDRES** **Reset: 00_H** Fractional Divider Result Register	Bit Field	RESULT							
		Type	rh							
CF_H	**SCON1** **Reset: 07_H** Serial Channel Control Register 1	Bit Field	0					NDOV EN	TIEN	RIEN
		Type	r					rw	rw	rw

3.2.4.9 SSC Registers

The SSC SFRs can be accessed in the standard memory area (RMAP = 0).

Table 12 SSC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$A9_H$	**SSC_PISEL** **Reset: 00_H** Port Input Select Register	Bit Field	0					CIS	SIS	MIS
		Type	r					rw	rw	rw
AA_H	**SSC_CONL** **Reset: 00_H** Control Register Low Programming Mode	Bit Field	LB	PO	PH	HB	BM			
		Type	rw	rw	rw	rw	rw			
AA_H	**SSC_CONL** **Reset: 00_H** Control Register Low Operating Mode	Bit Field	0				BC			
		Type	r				rh			
AB_H	**SSC_CONH** **Reset: 00_H** Control Register High Programming Mode	Bit Field	EN	MS	0	AREN	BEN	PEN	REN	TEN
		Type	rw	rw	r	rw	rw	rw	rw	rw
AB_H	**SSC_CONH** **Reset: 00_H** Control Register High Operating Mode	Bit Field	EN	MS	0	BSY	BE	PE	RE	TE
		Type	rw	rw	r	rh	rwh	rwh	rwh	rwh

Table 14 OCDS Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
$E9_H$	**MMCR2** **Reset: $8U_H$** Monitor Mode Control 2 Register	Bit Field	STMODE	EXBC	DSUSP	MBCON	ALTDI	MMEP	MMODE	JENA
		Type	rw	rw	rw	rwh	rw	rwh	rh	rh
EA_H	**MEXTCR** **Reset: $0U_H$** Memory Extension Control Register	Bit Field	0				BANKBPx			
		Type	r				rw			
EB_H	**MMWR1** **Reset: 00_H** Monitor Work Register 1	Bit Field	MMWR1							
		Type	rw							
EC_H	**MMWR2** **Reset: 00_H** Monitor Work Register 2	Bit Field	MMWR2							
		Type	rw							
$F1_H$	**MMCR** **Reset: 00_H** Monitor Mode Control Register	Bit Field	MEXIT_P	MEXIT	0	MSTEP	MRAMS_P	MRAMS	TRF	RRF
		Type	w	rwh	r	rw	w	rwh	rh	rh
$F2_H$	**MMSR** **Reset: 00_H** Monitor Mode Status Register	Bit Field	MBCAM	MBCIN	EXBF	SWBF	HWB3F	HWB2F	HWB1F	HWB0F
		Type	rw	rwh	rwh	rwh	rwh	rwh	rwh	rwh
$F3_H$	**MMBPCR** **Reset: 00_H** Breakpoints Control Register	Bit Field	SWBC	HWB3C		HWB2C		HWB1C	HWB0C	
		Type	rw	rw		rw		rw	rw	
$F4_H$	**MMICR** **Reset: 00_H** Monitor Mode Interrupt Control Register	Bit Field	DVECT	DRETR	COMRST	MSTSEL	MMUIE_P	MMUIE	RRIE_P	RRIE
		Type	rwh	rwh	rwh	rh	w	rw	w	rw
$F5_H$	**MMDR** **Reset: 00_H** Monitor Mode Data Transfer Register Receive	Bit Field	MMRR							
		Type	rh							
$F6_H$	**HWBPSR** **Reset: 00_H** Hardware Breakpoints Select Register	Bit Field	0			BPSEL_P	BPSEL			
		Type	r			w	rw			
$F7_H$	**HWBPDR** **Reset: 00_H** Hardware Breakpoints Data Register	Bit Field	HWBPxx							
		Type	rw							

Figure 18 shows the structure of a bidirectional port pin.

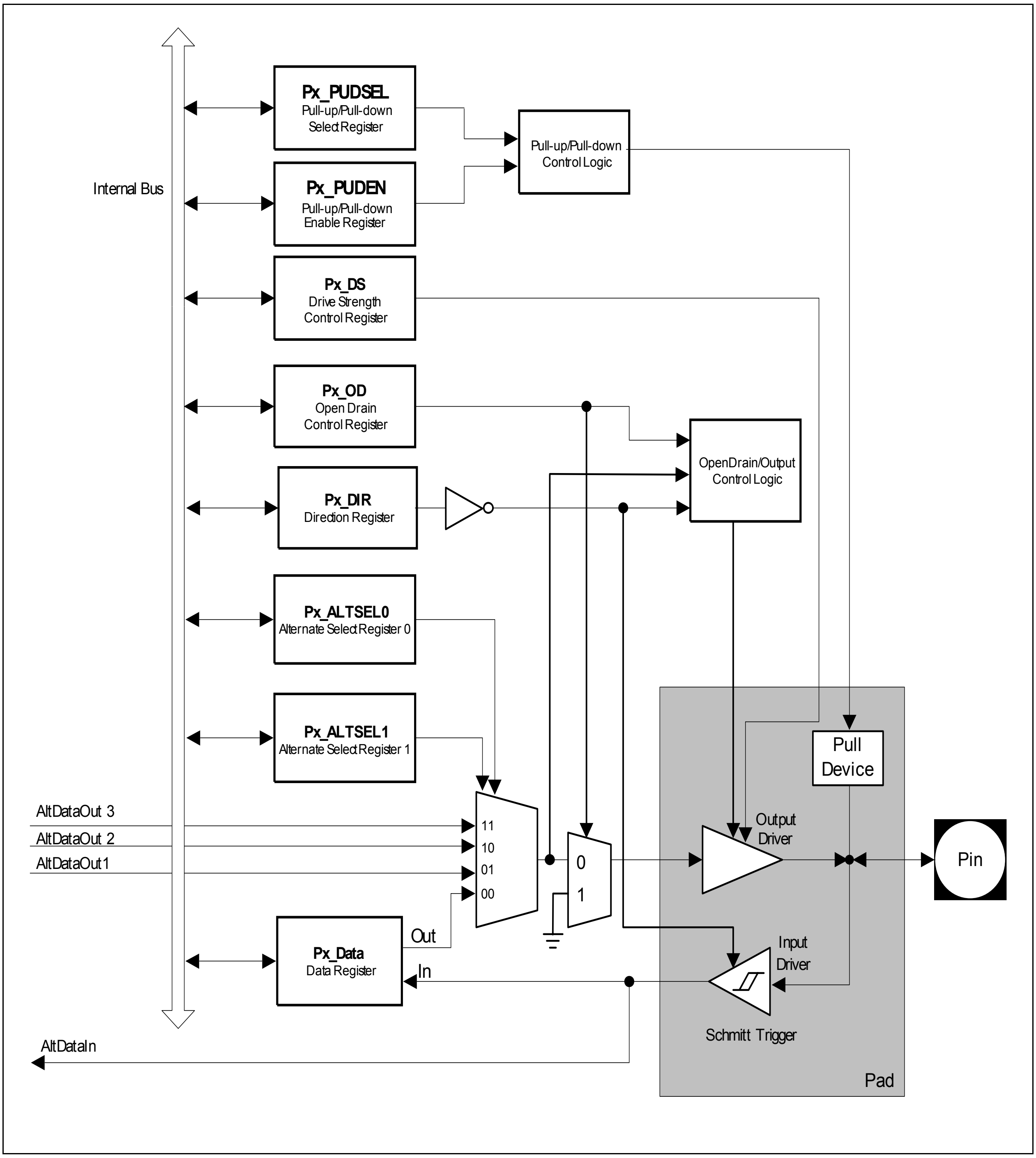


Figure 18 General Structure of Bidirectional Port

3.8 Clock Generation Unit

The Clock Generation Unit (CGU) allows great flexibility in the clock generation for the XC858. The power consumption is indirectly proportional to the frequency, whereas the performance of the microcontroller is directly proportional to the frequency. During user program execution, the frequency can be programmed for an optimal ratio between performance and power consumption. Therefore the power consumption can be adapted to the actual application state.

Features

- Phase-Locked Loop (PLL) for multiplying clock source by different factors
- PLL Base Mode
- Prescaler Mode
- PLL Mode
- Power-down mode support

The CGU consists of an oscillator circuit and a PLL. In the XC858, the oscillator can be from either of these two sources: the on-chip oscillator (4 MHz) or the external oscillator (2 MHz to 20 MHz). The term “oscillator” is used to refer to both on-chip oscillator and external oscillator, unless otherwise stated. After the reset, the on-chip oscillator will be used by default.The external oscillator can be selected via software. In addition, the PLL provides a fail-safe logic to perform oscillator run and loss-of-lock detection. This allows emergency routines to be executed for system recovery or to perform system shut down.

not be bypassed for this PLL mode. The PLL mode is used during normal system operation.

(3.2)

$$f_{SYS} \quad f_{OSC} \text{ x } \frac{NF}{NR \text{ x } OD}$$

System Frequency Selection

For the XC858, the value of NF, NR and OD can be selected by bits NDIV, PDIV and KDIV respectively for different oscillator inputs inorder to obtain the required fsys. But the combination of these factors must fulfill the following condition:

- 100 MHz < f_{VCO} < 175 MHz
- 800 kHz < f_{OSC} / (2 * NR) < 8 MHz

Table 21 provides examples on how the typical system frequency of fsys = 144 MHz and maximum frequency of 160 MHz (CPU clock = 24 MHz)can be obtained for the different oscillator sources.

Table 21 System frequency (f_{sys} = 144 MHz)

Oscillator	fosc	N	P	K	fsys
On-chip	4 MHz	72	2	1	144 MHz
	4 MHz	80	2	1	160 MHz
External	8 MHz	72	4	1	144 MHz
	6 MHz	72	3	1	144 MHz
	4 MHz	72	2	1	144 MHz

3.8.1 Recommended External Oscillator Circuits

The oscillator circuit, a Pierce oscillator, is designed to work with both, an external crystal oscillator or an external stable clock source. It basically consists of an inverting amplifier and a feedback element with XTAL1 as input, and XTAL2 as output.

When using a crystal, a proper external oscillator circuitry must be connected to both pins, XTAL1 and XTAL2. The crystal frequency can be within the range of 2 MHz to 20 MHz. Additionally, it is necessary to have two load capacitances C_{X1} and C_{X2}, and depending on the crystal type, a series resistor R_{X2}, to limit the current. A test resistor R_Q may be temporarily inserted to measure the oscillation allowance (negative resistance) of the oscillator circuitry. R_Q values are typically specified by the crystal vendor. An external feedback resistor R_f is also required in the external oscillator circuitry. The exact values and related operating range are dependent on the crystal frequency and have to be determined and optimized together with the crystal vendor using the negative

- Interrupt generation on the completion of a data transmission or reception

The UART modules can operate in the four modes shown in **Table 24**.

Table 24 UART Modes

Operating Mode	Baud Rate
Mode 0: 8-bit shift register	$f_{PCLK}/2$
Mode 1: 8-bit shift UART	Variable
Mode 2: 9-bit shift UART	$f_{PCLK}/32$ or $f_{PCLK}/64$[1)]
Mode 3: 9-bit shift UART	Variable

1) For UART1 module, the baud rate is fixed at $f_{PCLK}/64$.

There are several ways to generate the baud rate clock for the serial port, depending on the mode in which it is operating. In mode 0, the baud rate for the transfer is fixed at $f_{PCLK}/2$. In mode 2, the baud rate is generated internally based on the UART input clock and can be configured to either$f_{PCLK}/32$ or $f_{PCLK}/64$. For UART1 module, only $f_{PCLK}/64$ is available. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator. For UART module, the variable baud rate alternatively can be set by the overflow rate on Timer 1.

3.11.1 Baud-Rate Generator

Both UART modules have their own dedicated baud-rate generator, which is based on a programmable 8-bit reload value, and includes divider stages (i.e., prescaler and fractional divider) for generating a wide range of baud rates based on its input clock f_{PCLK}, see **Figure 26**.

3.17 Controller Area Network (MultiCAN)

The MultiCAN module contains two Full-CAN nodes operating independently or exchanging data and remote frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification V2.0 B active. Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Both CAN nodes share a common set of message objects, where each message object may be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects may be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double chained lists, where each CAN node has it's own list of message objects. A CAN node stores frames only into message objects that are allocated to the list of the CAN node. It only transmits messages from objects of this list. A powerful, command driven list controller performs all list operations.

The bit timings for the CAN nodes are derived from the peripheral clock (f_{CAN}) and are programmable up to a data rate of 1 MBaud. A pair of receive and transmit pins connects each CAN node to a bus transceiver.

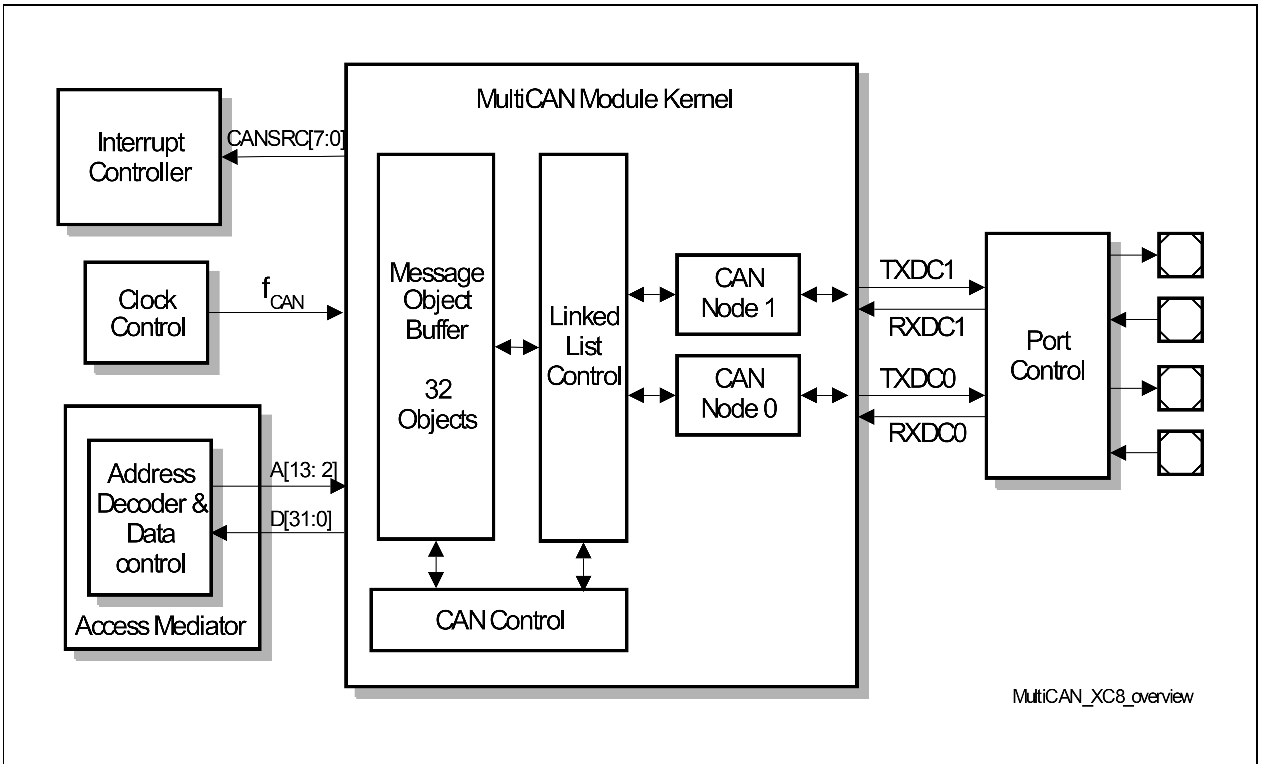


Figure 28 Overview of the MultiCAN

Features

- Compliant to ISO 11898.

Table 36 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5V Range)

Parameter	Symbol		Limit Values			Unit	Test Conditions/ Remarks
			min.	typ .	max.		
Input resistance of the reference input	R_{AREF}	CC	–	1	2	k :	1)
Input resistance of the selected analog channel	R_{AIN}	CC	–	1	3	k :	1)

1) Not subjected to production test, verified by design/characterization.

2) This value includes the maximum oscillator deviation.

3) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this, smaller capacitances are successively switched to the reference voltage.

4) The sampling capacity of the conversion C-Network is pre-charged to $V_{AREF}/2$ before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than $V_{AREF}/2$.

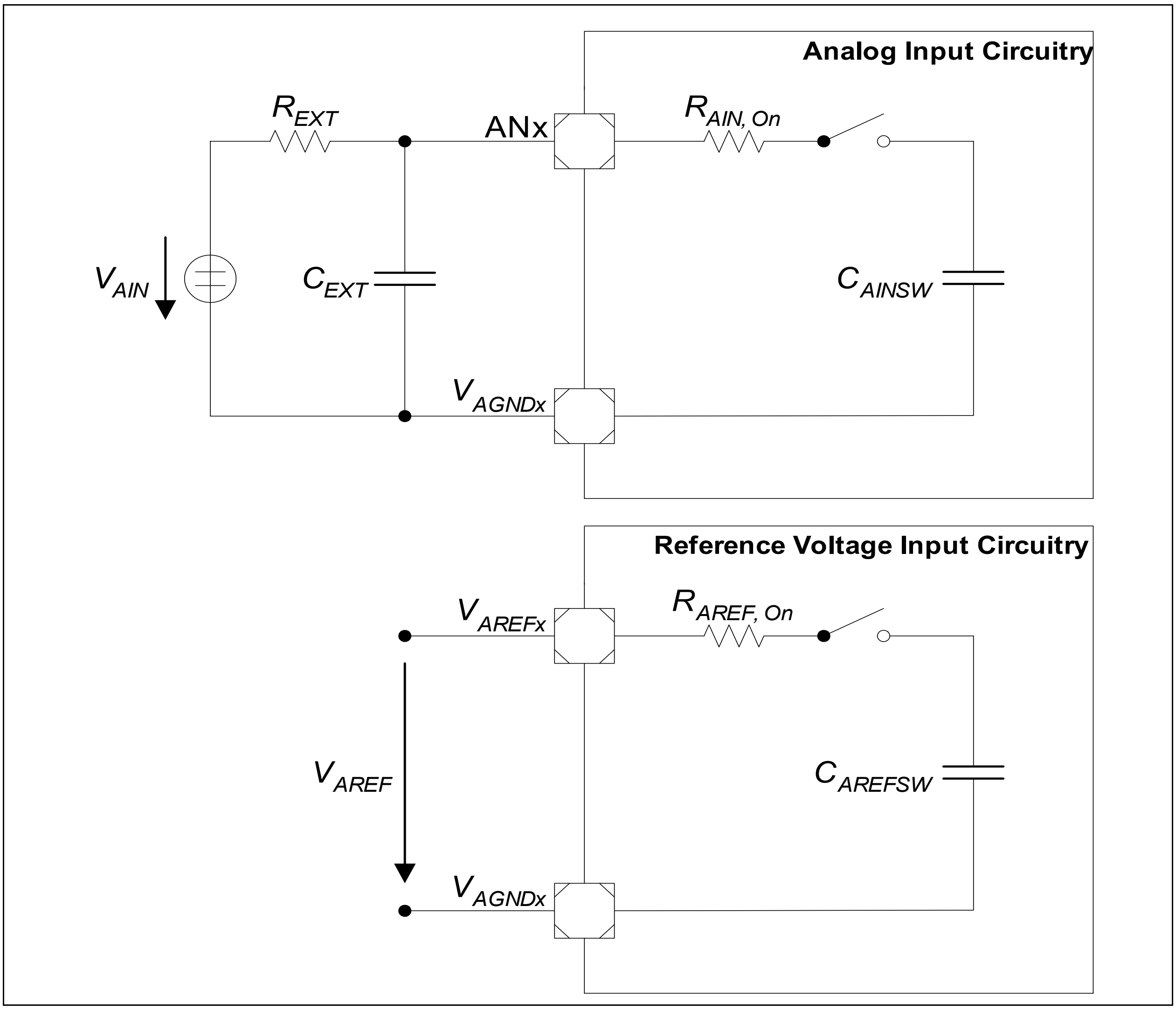


Figure 33 ADC Input Circuits

5 Package and Quality Declaration

Chapter 5 provides the information of the XC858 package and reliability section.

5.1 Package Parameters

Table 48 provides the thermal characteristics of the PG-LQFP-64-4 package used in XC858.

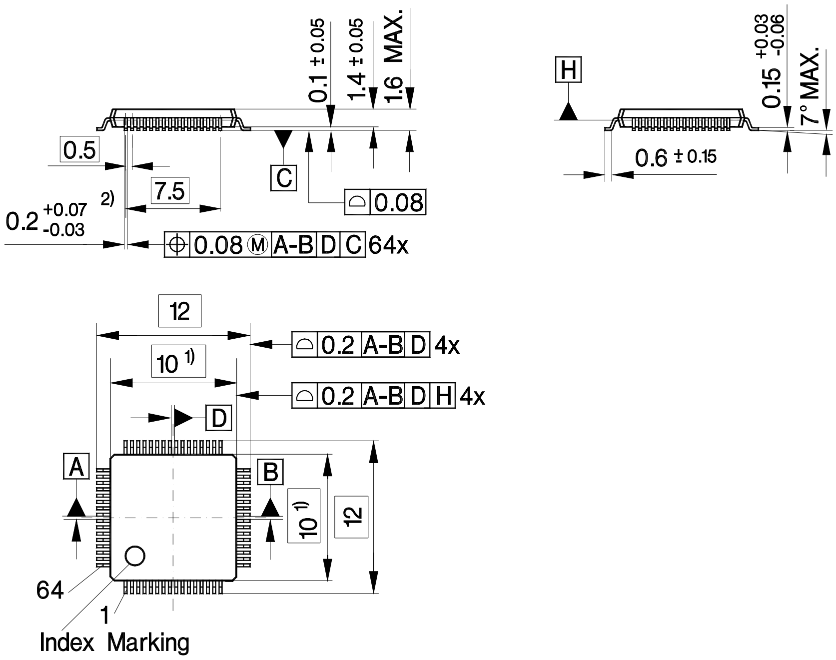
Table 48 Thermal Characteristics of the Packages

Parameter	Symbol		Limit Values		Unit	Notes
			Min.	Max.		
Thermal resistance junction case[1)]	R_{TJC}	CC	-	13.8	K/W	-
Thermal resistance junction lead[1)]	R_{TJL}	CC	-	34.6	K/W	-

1) The thermal resistances between the case and the ambient (R_{TCA}) , the lead and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case (R_{TJC}), the junction and the lead (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J=T_A+R_{TJA}$ uP_D, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances, by
a) simply adding only the two thermal resistances (junction lead and lead ambient), or
b) by taking all four resistances into account, depending on the precision needed.

5.2 Package Outline

Figure 45 shows the package outlines of the XC858.



1) Does not include plastic or metal protrusion of 0.25 max. per side

2) Does not include dambar protrusion of 0.08 max. per side

Figure 45 PG-LQFP-64-4 Package Outline