Infineon Technologies - SAF-XC858CA-16FFI AC Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	SSC, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc858ca-16ffi-ac

1 Summary of Features

The XC858 has the following features:

- High-performance XC800 Core
  - compatible with standard 8051 processor
  - two clocks per machine cycle architecture (for memory access without wait state)
  - two data pointers
- On-chip memory
  - 8 Kbytes of Boot ROM
  - 256 bytes of RAM
  - 3 Kbytes of XRAM
  - 64/52/36 Kbytes of Flash;
    (includes memory protection strategy)
- I/O port supply at 5.0 V and core logic supply at 2.5 V (generated by embedded voltage regulator)

(more features on next page)

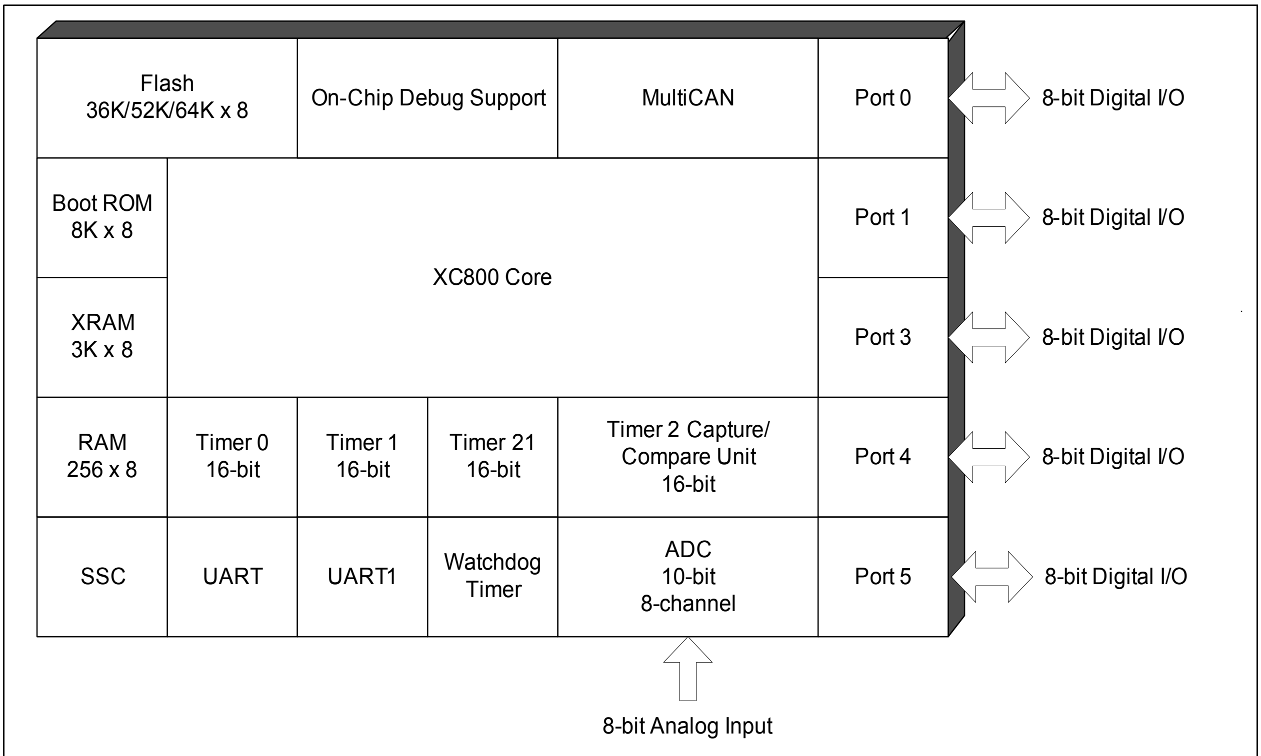


Figure 1 XC858 Functional Units

2.4 Pin Definitions and Functions

The functions and default states of the XC858 external pins are provided in Table 2.

Table 2 Pin Definitions and Functions

Symbol	Pin Number (LQFP-64)	Type	Reset State	Function	
P0		I/O		**Port 0** Port 0 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, UART, UART1, T2CCU, Timer 21, MultiCAN, SSC and External Interface.	
P0.0	17		Hi-Z	TCK_0 CLKOUT_0 RXDO_1	JTAG Clock Input Clock Output UART Transmit Data Output
P0.1	21		Hi-Z	TDI_0 RXD_1 RXDC1_0 EXF2_1	JTAG Serial Data Input UART Receive Data Input MultiCAN Node 1 Receiver Input Timer 2 External Flag Output
P0.2	18		PU	TDO_0 TXD_1 TXDC1_0	JTAG Serial Data Output UART Transmit Data Output/Clock Output MultiCAN Node 1 Transmitter Output
P0.3	63		Hi-Z	SCK_1 RXDO1_0 A17	SSC Clock Input/Output UART1 Transmit Data Output Address Line 17 Output
P0.4	64		Hi-Z	MTSR_1 TXD1_0 A18	SSC Master Transmit Output/ Slave Receive Input UART1 Transmit Data Output/Clock Output Address Line 18 Output
P0.5	1		Hi-Z	MRST_1 EXINT0_0 T2EX1_1 RXD1_0 A19	SSC Master Receive Input/Slave Transmit Output External Interrupt Input 0 Timer 21 External Trigger Input UART1 Receive Data Input Address Line 19 Output

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64)	Type	Reset State	Function	
P0.6	2		PU	T2CC4_1 $\overline{\text{WR}}$	Compare Output Channel 4 External Data Write Control Output
P0.7	62		PU	CLKOUT_1 T2CC5_1 $\overline{\text{RD}}$	Clock Output Compare Output Channel 5 External Data Read Control Output

Table 2 Pin Definitions and Functions (cont'd)

Symbol	**Pin Number (LQFP-64)**	**Type**	**Reset State**	**Function**	
P5		I/O		**Port 5** Port 5 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for UART, UART1, T2CCU, JTAG and External Interface.	
P5.0	8		PU	EXINT1_1 A0	External Interrupt Input 1 Address Line 0 Output
P5.1	9		PU	EXINT2_1 A1	External Interrupt Input 2 Address Line 1 Output
P5.2	12		PU	RXD_2 T2CC2_2/ EXINT5_3 A2	UART Receive Data Input External Interrupt Input 5/T2CCU Capture/Compare Channel 2 Address Line 2 Output
P5.3	13		PU	EXINT1_0 TXD_2 T2CC5_2 A3	External Interrupt Input 1 UART Transmit Data Output/Clock Output Compare Output Channel 5 Address Line 3 Output
P5.4	14		PU	EXINT2_0 RXDO_2 T2CC4_2 A4	External Interrupt Input 2 UART Transmit Data Output Compare Output Channel 4 Address Line 4 Output
P5.5	15		PU	TDO_1 TXD1_2 T2CC0_2/ EXINT3_3 A5	JTAG Serial Data Output UART1 Transmit Data Output/ Clock Output External Interrupt Input 3/T2CCU Capture/Compare Channel 0 Address Line 5 Output
P5.6	19		PU	TCK_1 RXDO1_2 T2CC1_2/ EXINT4_3 A6	JTAG Clock Input UART1 Transmit Data Output External Interrupt Input 4/T2CCU Capture/Compare Channel 1 Address Line 6 Output

Table 4 CPU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
97_H	**MEXSP** **Reset: $7F_H$** Memory Extension Stack Pointer Register	Bit Field	0	MXSP						
		Type	r	rwh						
98_H	**SCON** **Reset: 00_H** Serial Channel Control Register	Bit Field	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
		Type	rw	rw	rw	rw	rw	rwh	rwh	rwh
99_H	**SBUF** **Reset: 00_H** Serial Data Buffer Register	Bit Field	VAL							
		Type	rwh							
$A2_H$	**EO** **Reset: 00_H** Extended Operation Register	Bit Field	0			TRAP_EN	0			DPSEL0
		Type	r			rw	r			rw
$A8_H$	**IEN0** **Reset: 00_H** Interrupt Enable Register 0	Bit Field	EA	0	ET2	ES	ET1	EX1	ET0	EX0
		Type	rw	r	rw	rw	rw	rw	rw	rw
$B8_H$	**IP** **Reset: 00_H** Interrupt Priority Register	Bit Field	0		PT2	PS	PT1	PX1	PT0	PX0
		Type	r		rw	rw	rw	rw	rw	rw
$B9_H$	**IPH** **Reset: 00_H** Interrupt Priority High Register	Bit Field	0		PT2H	PSH	PT1H	PX1H	PT0H	PX0H
		Type	r		rw	rw	rw	rw	rw	rw
$D0_H$	**PSW** **Reset: 00_H** Program Status Word Register	Bit Field	CY	AC	F0	RS1	RS0	OV	F1	P
		Type	rwh	rwh	rw	rw	rw	rwh	rw	rh
$E0_H$	**ACC** **Reset: 00_H** Accumulator Register	Bit Field	ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$E8_H$	**IEN1** **Reset: 00_H** Interrupt Enable Register 1	Bit Field	ECCIP3	ECCIP2	ECCIP1	ECCIP0	EXM	EX2	ESSC	EADC
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$F0_H$	**B** **Reset: 00_H** B Register	Bit Field	B7	B6	B5	B4	B3	B2	B1	B0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$F8_H$	**IP1** **Reset: 00_H** Interrupt Priority 1 Register	Bit Field	PCCIP3	PCCIP2	PCCIP1	PCCIP0	PXM	PX2	PSSC	PADC
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$F9_H$	**IPH1** **Reset: 00_H** Interrupt Priority 1 High Register	Bit Field	PCCIP3H	PCCIP2H	PCCIP1H	PCCIP0H	PXMH	PX2H	PSSCH	PADCH
		Type	rw	rw	rw	rw	rw	rw	rw	rw

3.2.4.2 System Control Registers

The system control SFRs can be accessed in the mapped memory area (RMAP = 0).

Table 5 SCU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0 or 1										
$8F_H$	**SYSCON0** **Reset: 04_H** System Control Register 0	Bit Field	0			IMODE	0	1	0	RMAP
		Type	r			rw	r	r	r	rw

Table 7 Port Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
B0H	**P3_PUDSEL Reset: BFH** P3 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B1H	**P3_PUDEN Reset: 40H** P3 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C8H	**P4_PUDSEL Reset: FFH** P4 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C9H	**P4_PUDEN Reset: 04H** P4 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, PAGE 2										
80H	**P0_ALTSEL0 Reset: 00H** P0 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86H	**P0_ALTSEL1 Reset: 00H** P0 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90H	**P1_ALTSEL0 Reset: 00H** P1 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
91H	**P1_ALTSEL1 Reset: 00H** P1 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92H	**P5_ALTSEL0 Reset: 00H** P5 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
93H	**P5_ALTSEL1 Reset: 00H** P5 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B0H	**P3_ALTSEL0 Reset: 00H** P3 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B1H	**P3_ALTSEL1 Reset: 00H** P3 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C8H	**P4_ALTSEL0 Reset: 00H** P4 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C9H	**P4_ALTSEL1 Reset: 00H** P4 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, PAGE 3										
80H	**P0_OD Reset: 00H** P0 Open Drain Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86H	**P0_DS Reset: FFH** P0 Drive Strength Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90H	**P1_OD Reset: 00H** P1 Open Drain Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

Table 8 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CD$_H$	**ADC_CHINPR Reset: 00$_H$** Channel Interrupt Node Pointer Register	Bit Field	CHINP 7	CHINP 6	CHINP 5	CHINP 4	CHINP 3	CHINP 2	CHINP 1	CHINP 0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
CE$_H$	**ADC_EVINFR Reset: 00$_H$** Event Interrupt Flag Register	Bit Field	EVINF 7	EVINF 6	EVINF 5	EVINF 4	0		EVINF 1	EVINF 0
		Type	rh	rh	rh	rh	r		rh	rh
CF$_H$	**ADC_EVINCR Reset: 00$_H$** Event Interrupt Clear Flag Register	Bit Field	EVINC 7	EVINC 6	EVINC 5	EVINC 4	0		EVINC 1	EVINC 0
		Type	w	w	w	w	r		w	w
D2$_H$	**ADC_EVINSR Reset: 00$_H$** Event Interrupt Set Flag Register	Bit Field	EVINS 7	EVINS 6	EVINS 5	EVINS 4	0		EVINS 1	EVINS 0
		Type	w	w	w	w	r		w	w
D3$_H$	**ADC_EVINPR Reset: 00$_H$** Event Interrupt Node Pointer Register	Bit Field	EVINP 7	EVINP 6	EVINP 5	EVINP 4	0		EVINP 1	EVINP 0
		Type	rw	rw	rw	rw	r		rw	rw
RMAP = 0, PAGE 6										
CA$_H$	**ADC_CRCR1 Reset: 00$_H$** Conversion Request Control Register 1	Bit Field	CH7	CH6	CH5	CH4	0			
		Type	rwh	rwh	rwh	rwh	r			
CB$_H$	**ADC_CRPR1 Reset: 00$_H$** Conversion Request Pending Register 1	Bit Field	CHP7	CHP6	CHP5	CHP4	0			
		Type	rwh	rwh	rwh	rwh	r			
CC$_H$	**ADC_CRMR1 Reset: 00$_H$** Conversion Request Mode Register 1	Bit Field	Rsv	LDEV	CLRP ND	SCAN	ENSI	ENTR	0	ENGT
		Type	r	w	w	rw	rw	rw	r	rw
CD$_H$	**ADC_QMR0 Reset: 00$_H$** Queue Mode Register 0	Bit Field	CEV	TREV	FLUS H	CLRV	0	ENTR	0	ENGT
		Type	w	w	w	w	r	rw	r	rw
CE$_H$	**ADC_QSR0 Reset: 20$_H$** Queue Status Register 0	Bit Field	Rsv	0	EMPT Y	EV	0		FILL	
		Type	r	r	rh	rh	r		rh	
CF$_H$	**ADC_Q0R0 Reset: 00$_H$** Queue 0 Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
D2$_H$	**ADC_QBUR0 Reset: 00$_H$** Queue Backup Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
D2$_H$	**ADC_QINR0 Reset: 00$_H$** Queue Input Register 0	Bit Field	EXTR	ENSI	RF	0		REQCHNR		
		Type	w	w	w	r		w		

Table 12 SSC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
AC_H	**SSC_TBL** **Reset: 00_H** Transmitter Buffer Register Low	Bit Field	TB_VALUE							
		Type	rw							
AD_H	**SSC_RBL** **Reset: 00_H** Receiver Buffer Register Low	Bit Field	RB_VALUE							
		Type	rh							
AE_H	**SSC_BRL** **Reset: 00_H** Baud Rate Timer Reload Register Low	Bit Field	BR_VALUE							
		Type	rw							
AF_H	**SSC_BRH** **Reset: 00_H** Baud Rate Timer Reload Register High	Bit Field	BR_VALUE							
		Type	rw							

3.2.4.10 MultiCAN Registers

The MultiCAN SFRs can be accessed in the standard memory area (RMAP = 0).

Table 13 CAN Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$D8_H$	**ADCON** **Reset: 00_H** CAN Address/Data Control Register	Bit Field	V3	V2	V1	V0	AUAD		BSY	RWEN
		Type	rw	rw	rw	rw	rw		rh	rw
$D9_H$	**ADL** **Reset: 00_H** CAN Address Register Low	Bit Field	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
DA_H	**ADH** **Reset: 00_H** CAN Address Register High	Bit Field	0				CA13	CA12	CA11	CA10
		Type	r				rwh	rwh	rwh	rwh
DB_H	**DATA0** **Reset: 00_H** CAN Data Register 0	Bit Field	CD							
		Type	rwh							
DC_H	**DATA1** **Reset: 00_H** CAN Data Register 1	Bit Field	CD							
		Type	rwh							
DD_H	**DATA2** **Reset: 00_H** CAN Data Register 2	Bit Field	CD							
		Type	rwh							
DE_H	**DATA3** **Reset: 00_H** CAN Data Register 3	Bit Field	CD							
		Type	rwh							

3.2.4.11 OCDS Registers

The OCDS SFRs can be accessed in the mapped memory area (RMAP = 1).

3.4.3 Interrupt Priority

An interrupt that is currently being serviced can only be interrupted by a higher-priority interrupt, but not by another interrupt of the same or lower priority. Hence, an interrupt of the highest priority cannot be interrupted by any other interrupt request.

If two or more requests of different priority levels are received simultaneously, the request of the highest priority is serviced first. If requests of the same priority are received simultaneously, then an internal polling sequence determines which request is serviced first. Thus, within each priority level, there is a second priority structure determined by the polling sequence shown in **Table 18**.

Table 18 Priority Structure within Interrupt Level

Source	Level
Non-Maskable Interrupt (NMI)	(highest)
External Interrupt 0	1
Timer 0 Interrupt	2
External Interrupt 1	3
Timer 1 Interrupt	4
UART Interrupt	5
T2CCU,UART Normal Divider Overflow, MultiCAN Interrupt	6
ADC, MultiCAN Interrupt	7
SSC Interrupt	8
External Interrupt 2, Timer 21, UART1, UART1 Normal Divider Overflow Interrupt	9
External Interrupt [6:3], MultiCAN Interrupt	10
MultiCAN interrupt	11
MultiCAN Interrupt	12
MultiCAN Interrupt	13
MultiCAN Interrupt	14

3.5 Parallel Ports

The XC858 has 40 port pins organized into five parallel ports: Port 0 (P0), Port 1 (P1), Port 3 (P3), Port 4 (P4) and Port 5 (P5). Each pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. These ports are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected.

Bidirectional Port Features

- Configurable pin direction
- Configurable pull-up/pull-down devices
- Configurable open drain mode
- Configurable drive strength
- Transfer of data through digital inputs and outputs (general purpose I/O)
- Alternate input/output for on-chip peripherals

Figure 18 shows the structure of a bidirectional port pin.

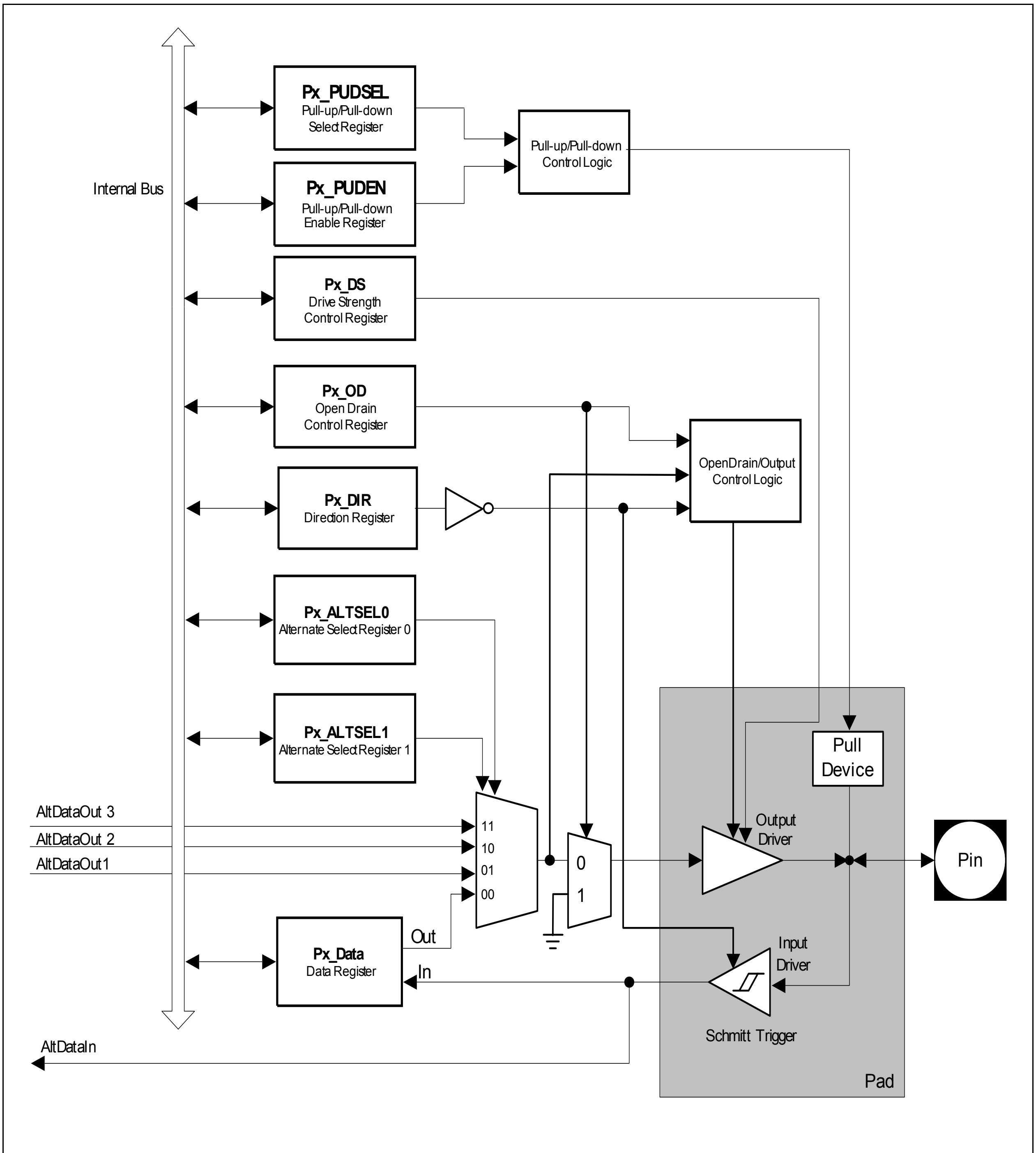


Figure 18 General Structure of Bidirectional Port

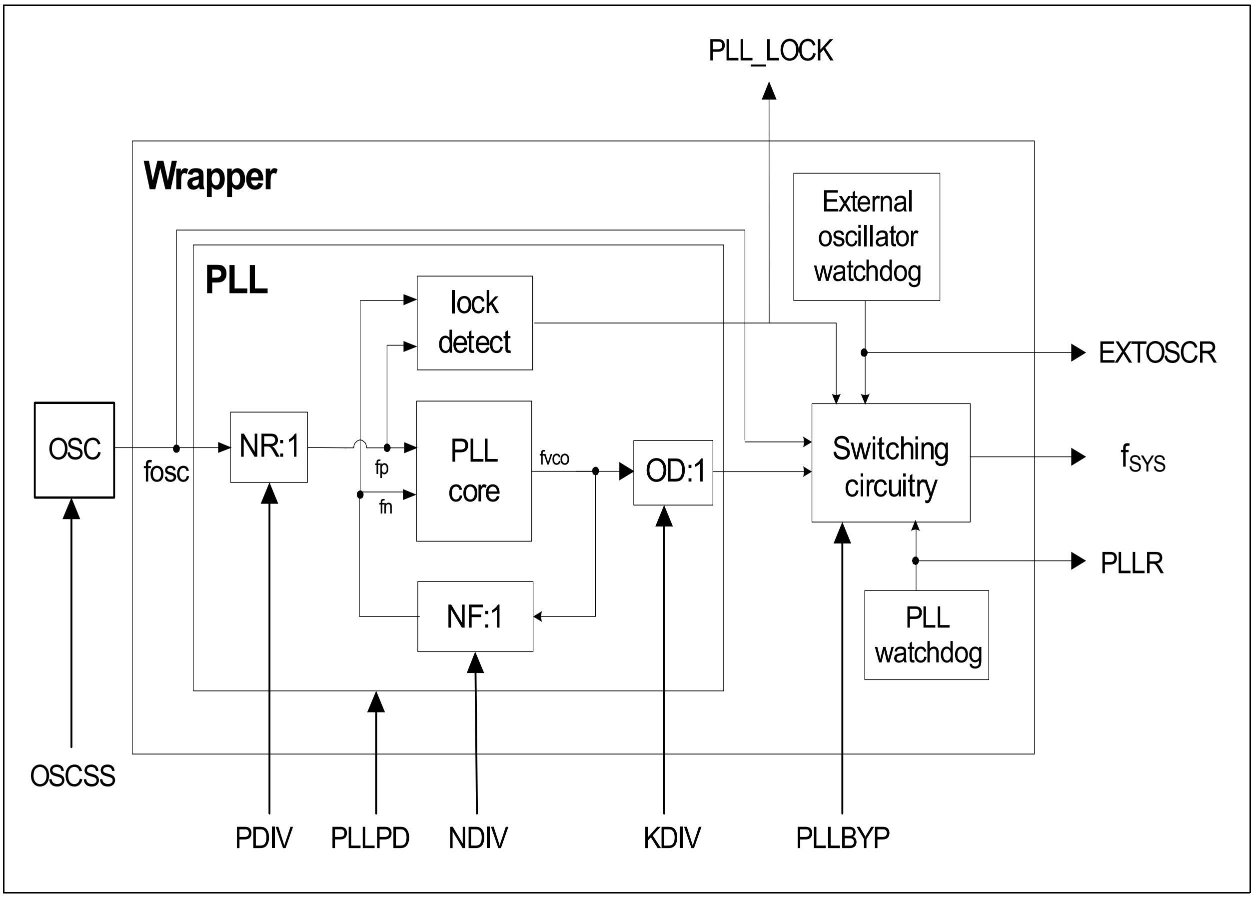


Figure 20 CGU Block Diagram

Direct Drive (PLL Bypass Operation)

During PLL bypass operation, the system clock has the same frequency as the external clock source.

$$f_{SYS} = f_{OSC} \tag{3.1}$$

PLL Mode

The CPU clock is derived from the oscillator clock, divided by the NR factor (PDIV), multiplied by the NF factor (NDIV), and divided by the OD factor (KDIV). PLL output must

3.14 Timer 0 and Timer 1

Timer 0 and Timer 1 can function as both timers or counters. When functioning as a timer, Timer 0 and Timer 1 are incremented every machine cycle, i.e. every 2 input clocks (or 2 PCLKs). When functioning as a counter, Timer 0 and Timer 1 are incremented in response to a 1-to-0 transition (falling edge) at their respective external input pins, T0 or T1.

Timer 0 and 1 are fully compatible and can be configured in four different operating modes for use in a variety of applications, see **Table 27**. In modes 0, 1 and 2, the two timers operate independently, but in mode 3, their functions are specialized.

Table 27 Timer 0 and Timer 1 Modes

Mode	Operation
0	**13-bit timer** The timer is essentially an 8-bit counter with a divide-by-32 prescaler. This mode is included solely for compatibility with Intel 8048 devices.
1	**16-bit timer** The timer registers, TLx and THx, are concatenated to form a 16-bit counter.
2	**8-bit timer with auto-reload** The timer register TLx is reloaded with a user-defined 8-bit value in THx upon overflow.
3	**Timer 0 operates as two 8-bit timers** The timer registers, TL0 and TH0, operate as two separate 8-bit counters. Timer 1 is halted and retains its count even if enabled.

3.17 Controller Area Network (MultiCAN)

The MultiCAN module contains two Full-CAN nodes operating independently or exchanging data and remote frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification V2.0 B active. Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Both CAN nodes share a common set of message objects, where each message object may be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects may be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double chained lists, where each CAN node has it's own list of message objects. A CAN node stores frames only into message objects that are allocated to the list of the CAN node. It only transmits messages from objects of this list. A powerful, command driven list controller performs all list operations.

The bit timings for the CAN nodes are derived from the peripheral clock (f_{CAN}) and are programmable up to a data rate of 1 MBaud. A pair of receive and transmit pins connects each CAN node to a bus transceiver.

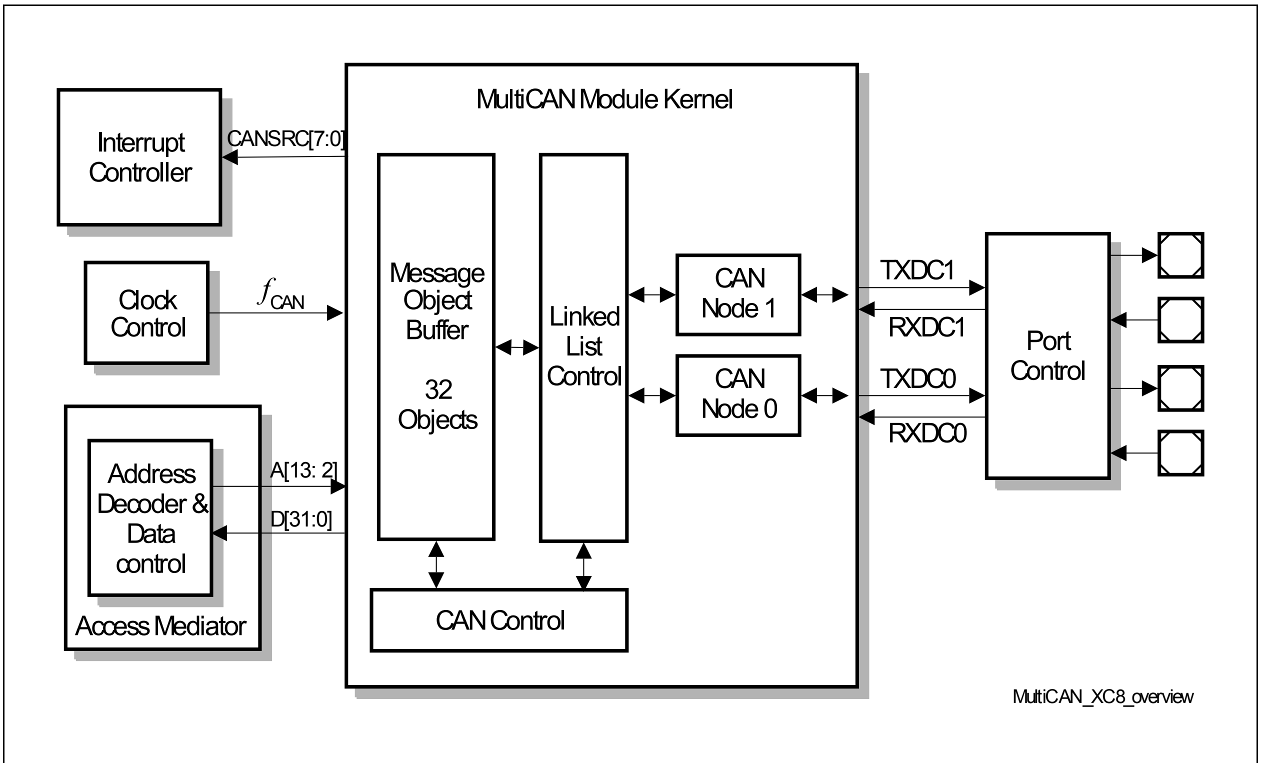


Figure 28 Overview of the MultiCAN

Features

- Compliant to ISO 11898.

3.18 Analog-to-Digital Converter

The XC858 includes a high-performance 10-bit Analog-to-Digital Converter (ADC) with eight multiplexed analog input channels. The ADC uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC are available at AN0 - AN7.

Features

- Successive approximation
- 8-bit or 10-bit resolution
- Eight analog channels
- Four independent result registers
- Result data protection for slow CPU access (wait-for-read mode)
- Single conversion mode
- Autoscan functionality
- Limit checking for conversion results
- Data reduction filter (accumulation of up to 2 conversion results)
- Two independent conversion request sources with programmable priority
- Selectable conversion request trigger
- Flexible interrupt generation with configurable service nodes
- Programmable sample time
- Programmable clock divider
- Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes

3.18.1 ADC Clocking Scheme

A common module clock f_{ADC} generates the various clock signals used by the analog and digital parts of the ADC module:

- f_{ADCA} is input clock for the analog part.
- f_{ADCI} is internal clock for the analog part (defines the time base for conversion length and the sample time). This clock is generated internally in the analog part, based on the input clock f_{ADCA} to generate a correct duty cycle for the analog components.
- f_{ADCD} is input clock for the digital part.

Figure 29 shows the clocking scheme of the ADC module. The prescaler ratio is selected by bit field CTC in register GLOBCTR. A prescaling ratio of 32 can be selected when the maximum performance of the ADC is not required.

- Synchronization phase (t_{SYN})
- Sample phase (t_S)
- Conversion phase
- Write result phase (t_{WR})

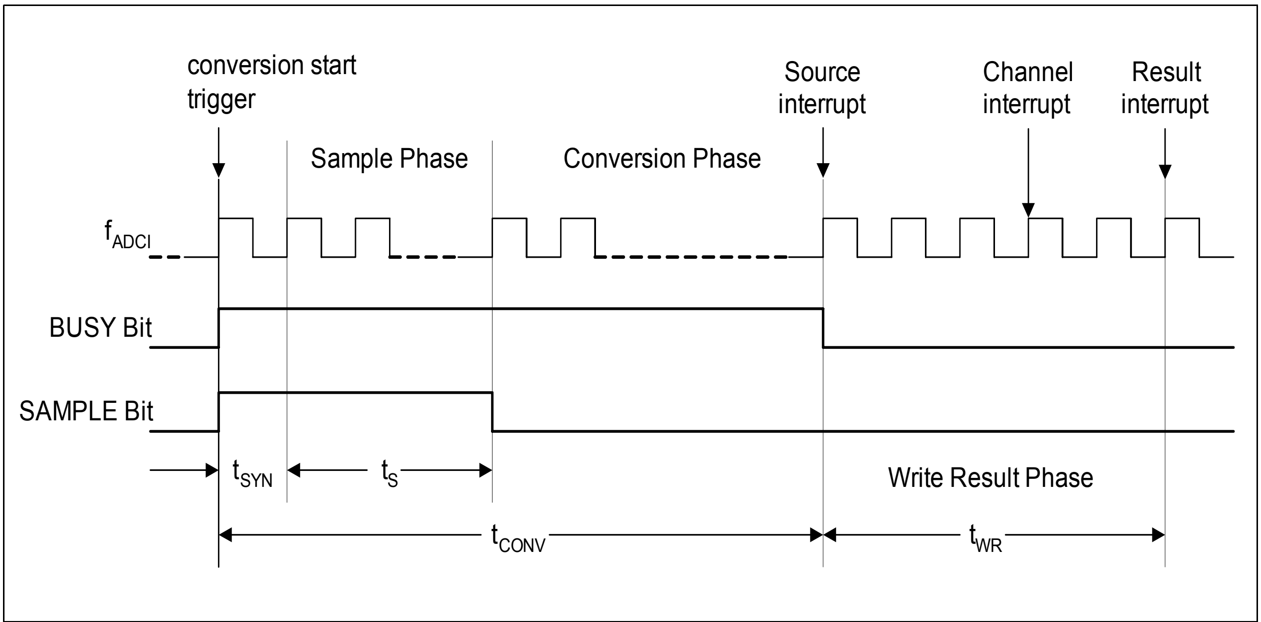


Figure 30 ADC Conversion Timing

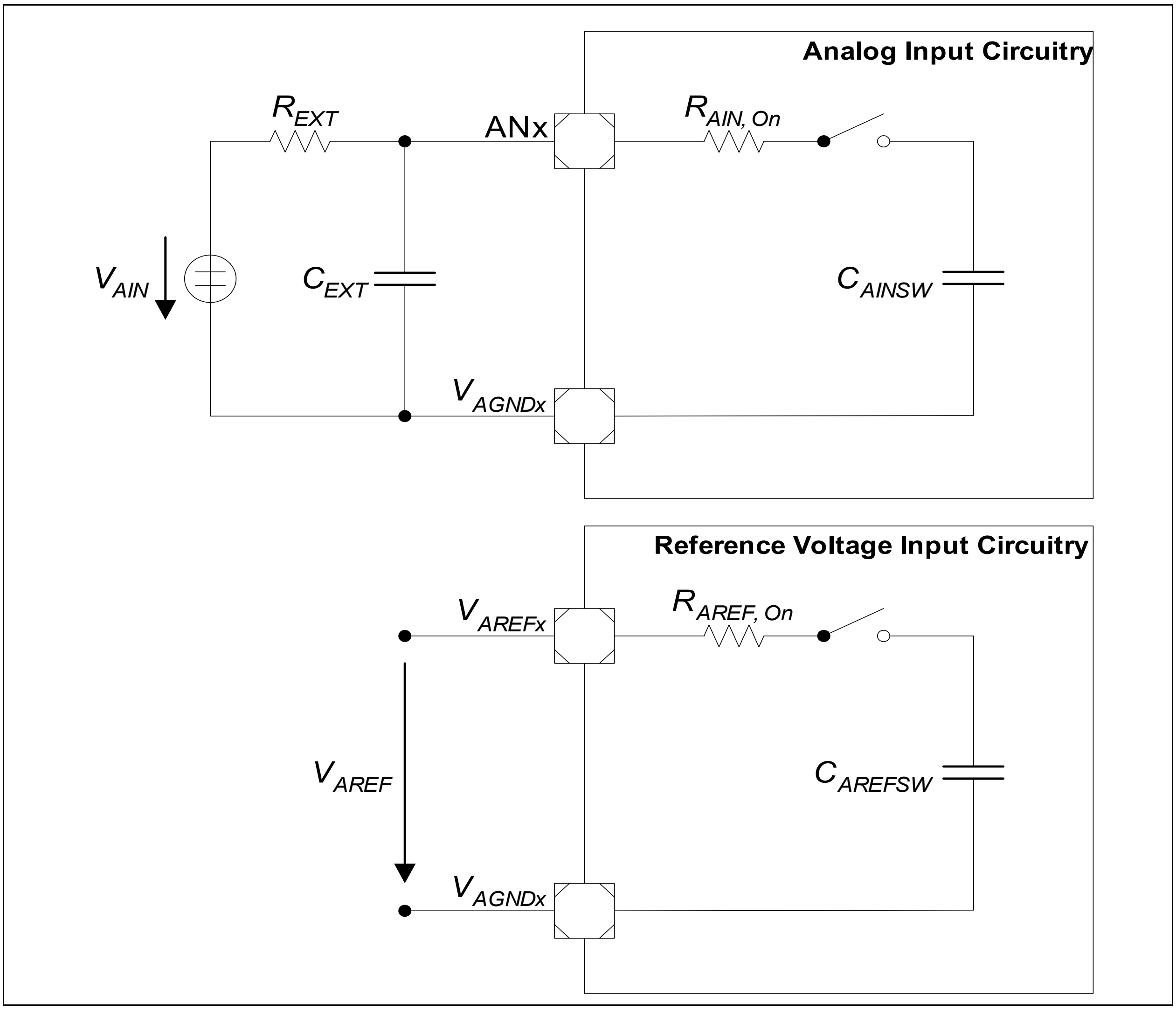


Figure 33 ADC Input Circuits

4.2.3.1 ADC Conversion Timing

Conversion time, $t_C = t_{ADC} \times (1 + r \times (3 + n + STC))$, where

r = CTC + 2 for CTC = 00_B, 01_B or 10_B,

r = 32 for CTC = 11_B,

CTC = Conversion Time Control (GLOBCTR.CTC),

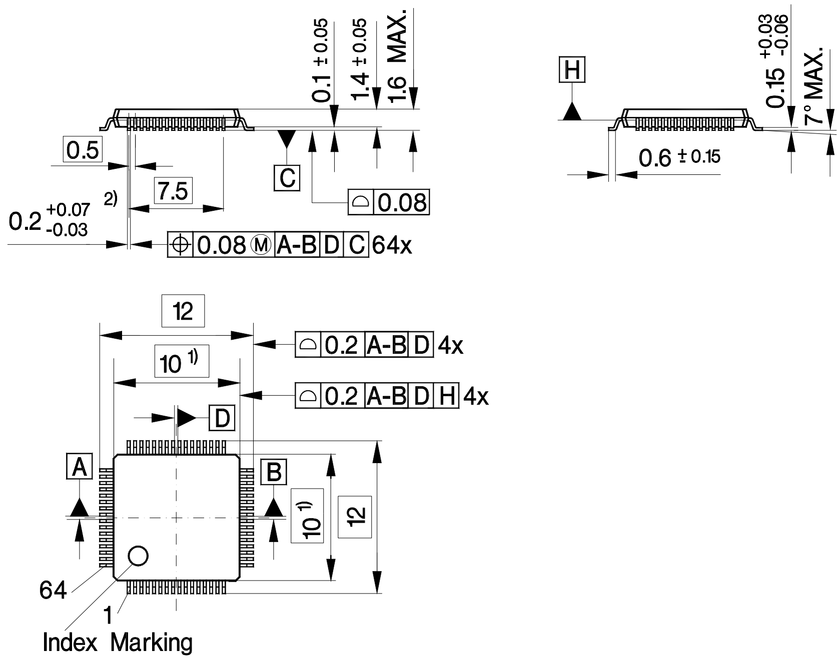
STC = Sample Time Control (INPCR0.STC),

n = 8 or 10 (for 8-bit and 10-bit conversion respectively),

$t_{ADC} = 1 / f_{ADC}$

5.2 Package Outline

Figure 45 shows the package outlines of the XC858.



1) Does not include plastic or metal protrusion of 0.25 max. per side

2) Does not include dambar protrusion of 0.08 max. per side

Figure 45 PG-LQFP-64-4 Package Outline

5.3 Quality Declaration

Table 49 shows the characteristics of the quality parameters in the XC858.

Table 49 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM}	-	500	V	Conforming to JESD22-C101-C