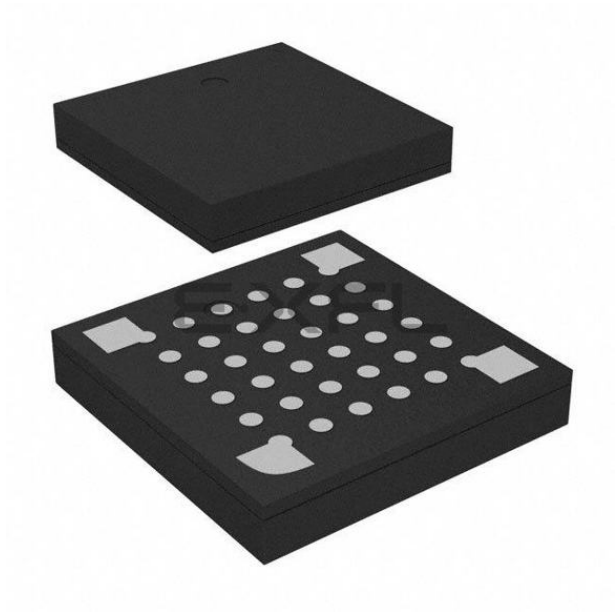
# Renesas Electronics America Inc - R7FS124762A01CLM#AC0 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | CANbus, I²C, SCI, SPI, UART/USART, USB |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 11x14b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 36-WFLGA |
| Supplier Device Package | 36-WFLGA (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs124762a01clm-ac0 |

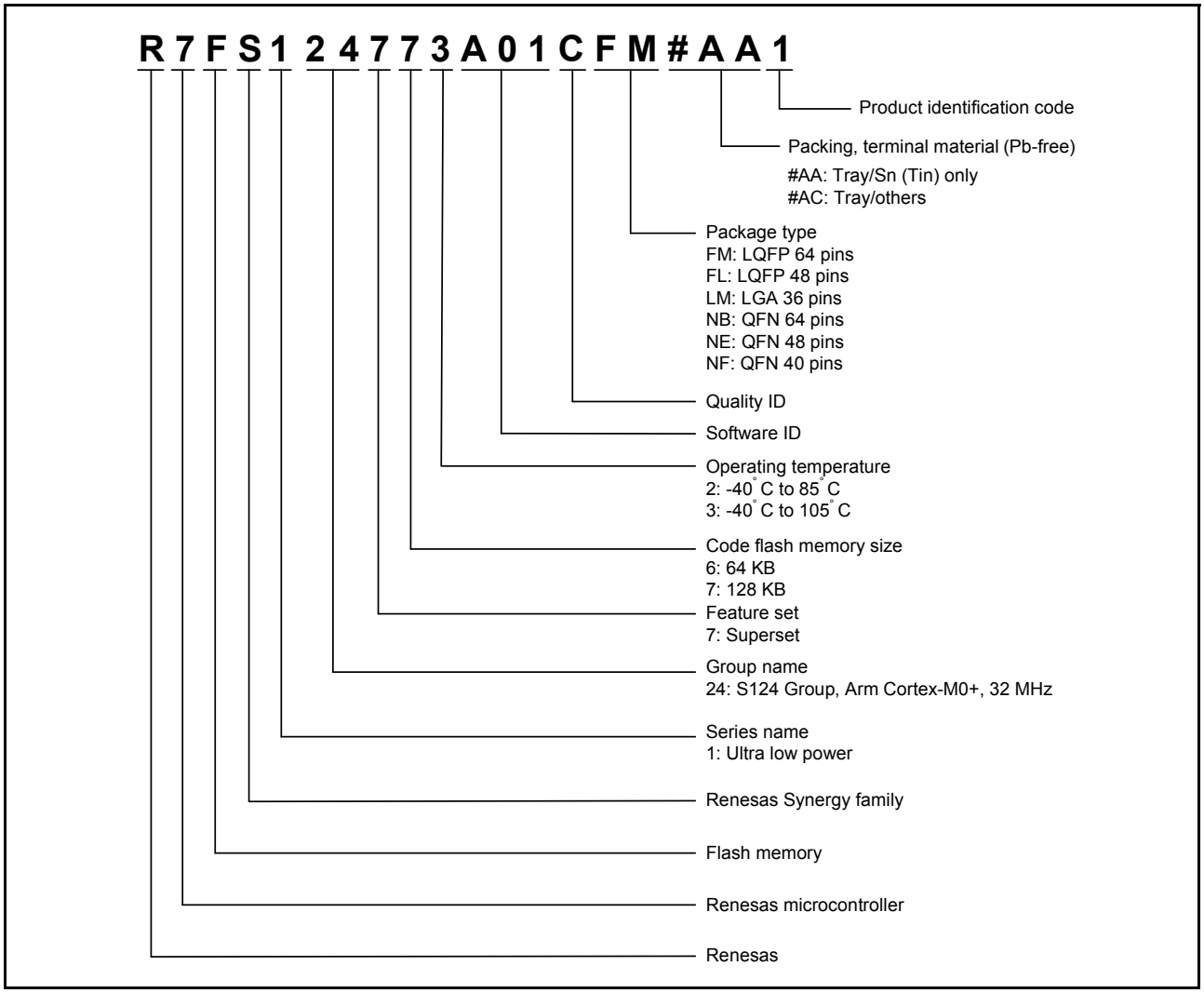



**Figure 1.2 Part numbering scheme**

**Table 1.12 Product list**

| Product part number | Orderable part number | Package code | Code flash | Data flash | SRAM | Operating temperature |
|---|---|---|---|---|---|---|
| R7FS124773A01CFM | R7FS124773A01CFM#AA1 | PLQP0064KB-C | 128 KB | 4 KB | 16 KB | –40 to +105°C |
| R7FS124773A01CNB | R7FS124773A01CNB#AC1 | PWQN0064LA-A | | | | –40 to +105°C |
| R7FS124773A01CFL | R7FS124773A01CFL#AA1 | PLQP0048KB-B | | | | –40 to +105°C |
| R7FS124773A01CNE | R7FS124773A01CNE#AC1 | PWQN0048KB-A | | | | –40 to +105°C |
| R7FS124773A01CNF | R7FS124773A01CNF#AC1 | PWQN0040KC-A | | | | –40 to +105°C |
| R7FS124772A01CLM | R7FS124772A01CLM#AC1 | PWLG0036KA-A | | | | –40 to +85°C |
| R7FS124763A01CFM | R7FS124763A01CFM#AA1 | PLQP0064KB-C | 64 KB | | | –40 to +105°C |
| R7FS124763A01CFL | R7FS124763A01CFL#AA1 | PLQP0048KB-B | | | | –40 to +105°C |
| R7FS124762A01CLM | R7FS124762A01CLM#AC1 | PWLG0036KA-A | | | | –40 to +85°C |

Note: Earlier products with orderable part number suffix AA0 and AC0 have a restriction in AES functions. If AES functions are required for your application, refer to the products with orderable part number suffix AA1 or AC1. For details on the differences of AES functions between AA0/AC0 and AA1/AC1 products, see *Technical Update (TN-SY*-A024A/E)*. Contact your Renesas sales representative for additional information.

**Table 1.14 Pin functions (3 of 3)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| ACMPLP | VCOUT | Output | Comparator output pin. |
| | CMPREF0, CMPREF1 | Input | Reference voltage input pins. |
| | CMPIN0, CMPIN1 | Input | Analog voltage input pins. |
| CTSU | TS00 to TS28, TS30, TS31 | Input | Capacitive touch detection pins (touch pins). |
| | TSCAP | - | Secondary power supply pin for the touch driver. |
| KINT | KR00 to KR07 | Input | Key interrupt input pins. |
| I/O ports | P000 to P004, P010 to P015 | I/O | General-purpose input/output pins. |
| | P100 to P113 | I/O | General-purpose input/output pins. |
| | P200 | Input | General-purpose input pin. |
| | P201, P204 to P206, P212, P213 | I/O | General-purpose input/output pins. |
| | P214, P215 | Input | General-purpose input pins. |
| | P300 to P304 | I/O | General-purpose input/output pins. |
| | P400 to P403, P407 to P411 | I/O | General-purpose input/output pins. |
| | P500 to P502 | I/O | General-purpose input/output pins. |

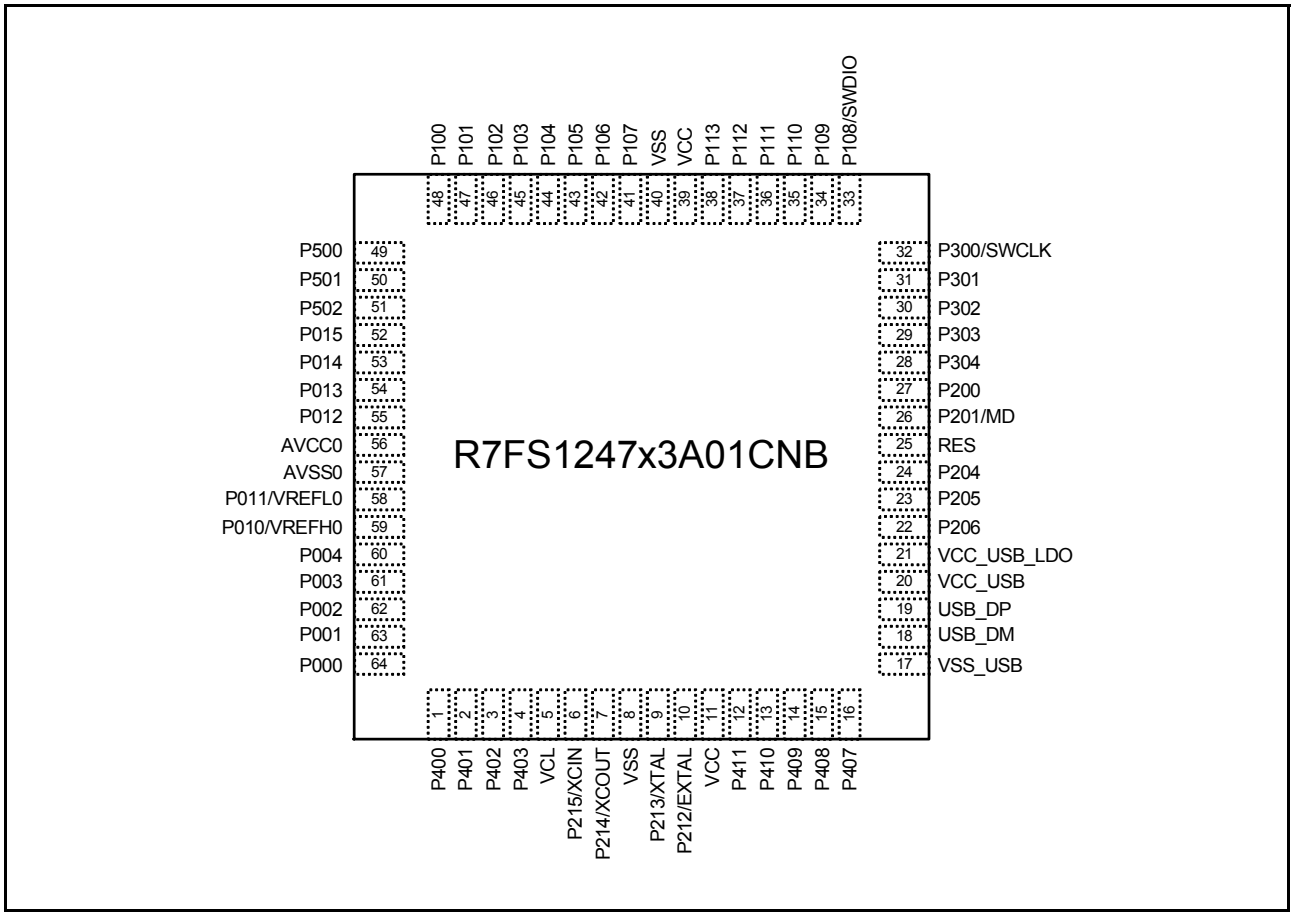



**Figure 1.4 Pin assignment for QFN 64-pin (top view)**

| Pin number | | | | | Power, System, Clock, Debug, CAC | I/O ports | Timers | | | | Communication Interfaces | | | | Analogs | | HMI | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64, QFN64 | LQFP48 | QFN48 | QFN40 | LGA36 | | | AGT | GPT_OPS, POEG | GPT | RTC | USBFS,CAN | SCI | IIC | SPI | ADC14 | DAC12, ACMPLP | CTSU | Interrupt |
| 35 | 27 | 27 | 23 | D5 | | P110 | | GTOVLO_A | GTIOC1B_A | | CRX0_A | CTS0_RTS0_C/SS0_C/RXD9_B/MISO9_B/SCL9_B | | MISOB_B | | VCOUT | TS11 | IRQ3 |
| 36 | 28 | 28 | 24 | D6 | | P111 | | | GTIOC3A_A | | | SCK0_C/SCK9_B | | RSPCKB_B | | | TS12 | IRQ4 |
| 37 | 29 | 29 | 25 | C6 | | P112 | | | GTIOC3B_A | | | TXD0_C/MOSI0_C/SDA0_C | | | | | TSCAP_C | |
| 38 | - | - | - | - | | P113 | | | | | | | | | | | | |
| 39 | 30 | 30 | - | - | VCC | | | | | | | | | | | | | |
| 40 | 31 | 31 | - | - | VSS | | | | | | | | | | | | | |
| 41 | - | - | - | - | | P107 | | | GTIOC0A_B | | | | | | | | | KR07 |
| 42 | - | - | - | - | | P106 | | | GTIOC0B_B | | | | | SSLA3_A | | | | KR06 |
| 43 | - | - | - | - | | P105 | | GTETRGA_C | | | | | | SSLA2_A | | | | KR05/IRQ0 |
| 44 | 32 | 32 | 26 | - | | P104 | | GTETRGB_B | | | | RXD0_C/MISO0_C/SCL0_C | | SSLA1_A | | | TS13 | KR04/IRQ1 |
| 45 | 33 | 33 | 27 | C3 | | P103 | | GTOWUP_A | GTIOC2A_A | | CTX0_C | CTS0_RTS0_A/SS0_A | | SSLA0_A | AN019 | CMPREF1 | TS14 | KR03 |
| 46 | 34 | 34 | 28 | C4 | | P102 | AGTO0 | GTOWLO_A | GTIOC2B_A | | CRX0_C | SCK0_A | | RSPCKA_A | AN020/ADTRG0_A | CMPIN1 | TS15 | KR02 |
| 47 | 35 | 35 | 29 | C5 | | P101 | AGTEE0 | GTETRGB_A | GTIOC5A_A | | | TXD0_A/MOSI0_A/SDA0_A/CTS1_RTS1_A/SS1_A | SDA1_B | MOSIA_A | AN021 | CMPREF0 | TS16 | KR01/IRQ1 |
| 48 | 36 | 36 | 30 | B6 | | P100 | AGTIO0_A | GTETRGA_A | GTIOC5B_A | | | RXD0_A/MISO0_A/SCL0_A/SCK1_A | SCL1_B | MISOA_A | AN022 | CMPIN0 | TS26 | KR00/IRQ2 |
| 49 | 37 | 37 | - | - | | P500 | AGTOA0 | GTIU_B | GTIOC2A_B | | | | | | AN016 | | TS27 | |
| 50 | - | - | - | - | | P501 | AGTOB0 | GTIV_B | GTIOC2B_B | | | | | | AN017 | | | |
| 51 | - | - | - | - | | P502 | | GTIW_B | GTIOC3B_B | | | | | | AN018 | | | |
| 52 | 38 | 38 | 31 | A6 | | P015 | | | | | | | | | AN010 | | TS28 | IRQ7 |
| 53 | 39 | 39 | 32 | A5 | | P014 | | | | | | | | | AN009 | DA0 | | |
| 54 | 40 | 40 | 33 | B5 | | P013 | | | | | | | | | AN008 | | | |
| 55 | 41 | 41 | 34 | B4 | | P012 | | | | | | | | | AN007 | | | |
| 56 | 42 | 42 | 35 | A4 | AVCC0 | | | | | | | | | | | | | |
| 57 | 43 | 43 | 36 | A3 | AVSS0 | | | | | | | | | | | | | |
| 58 | 44 | 44 | 37 | B3 | VREFL0 | P011 | | | | | | | | | AN006 | | TS31 | |
| 59 | 45 | 45 | 38 | A2 | VREFH0 | P010 | | | | | | | | | AN005 | | TS30 | |
| 60 | - | - | - | - | | P004 | | | | | | | | | AN004 | | TS25 | IRQ3 |
| 61 | - | - | - | - | | P003 | | | | | | | | | AN003 | | TS24 | |
| 62 | 46 | 46 | - | - | | P002 | | | | | | | | | AN002 | | TS23 | IRQ2 |
| 63 | 47 | 47 | 39 | - | | P001 | | | | | | | | | AN001 | | TS22 | IRQ7 |
| 64 | 48 | 48 | 40 | B2 | | P000 | | | | | | | | | AN000 | | TS21 | IRQ6 |

Note: Several pin names have the added suffix of _A, _B, _C, and _D. The suffix can be ignored when assigning functionality.

### 2.2.7 P408, P409 I/O Pin Output Characteristics of Middle Drive Capacity

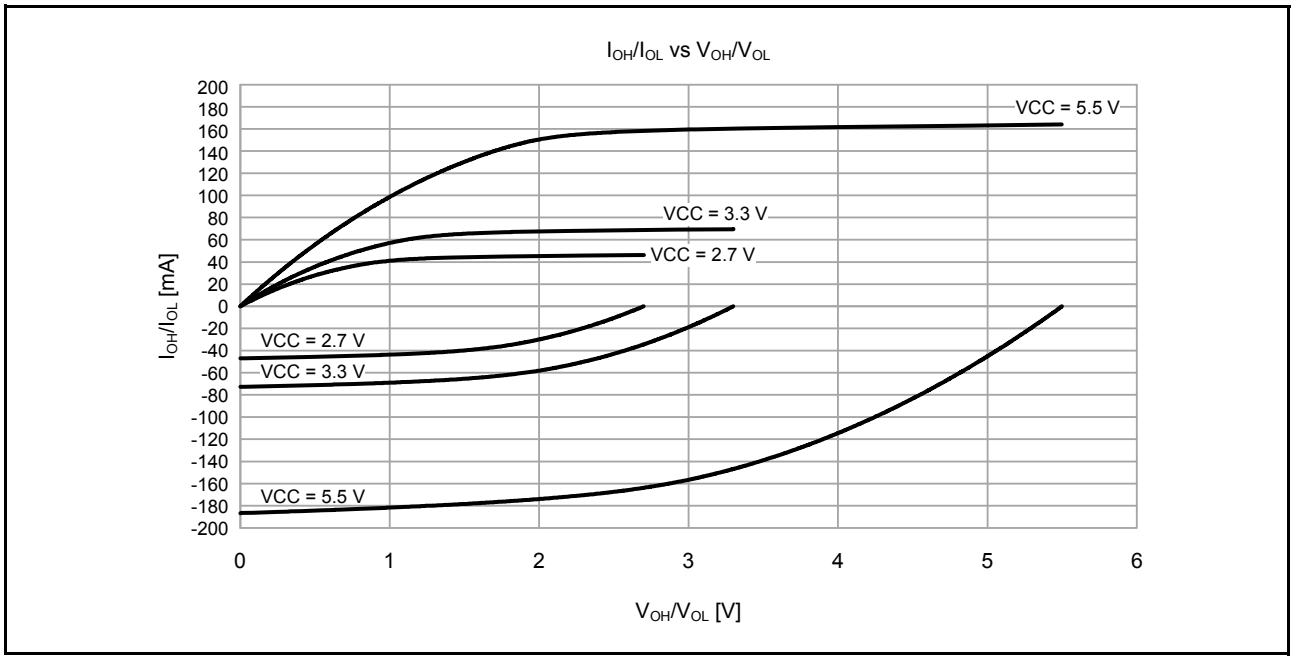



**Figure 2.12** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ voltage characteristics at Ta = 25°C when middle drive output is selected (reference data)**

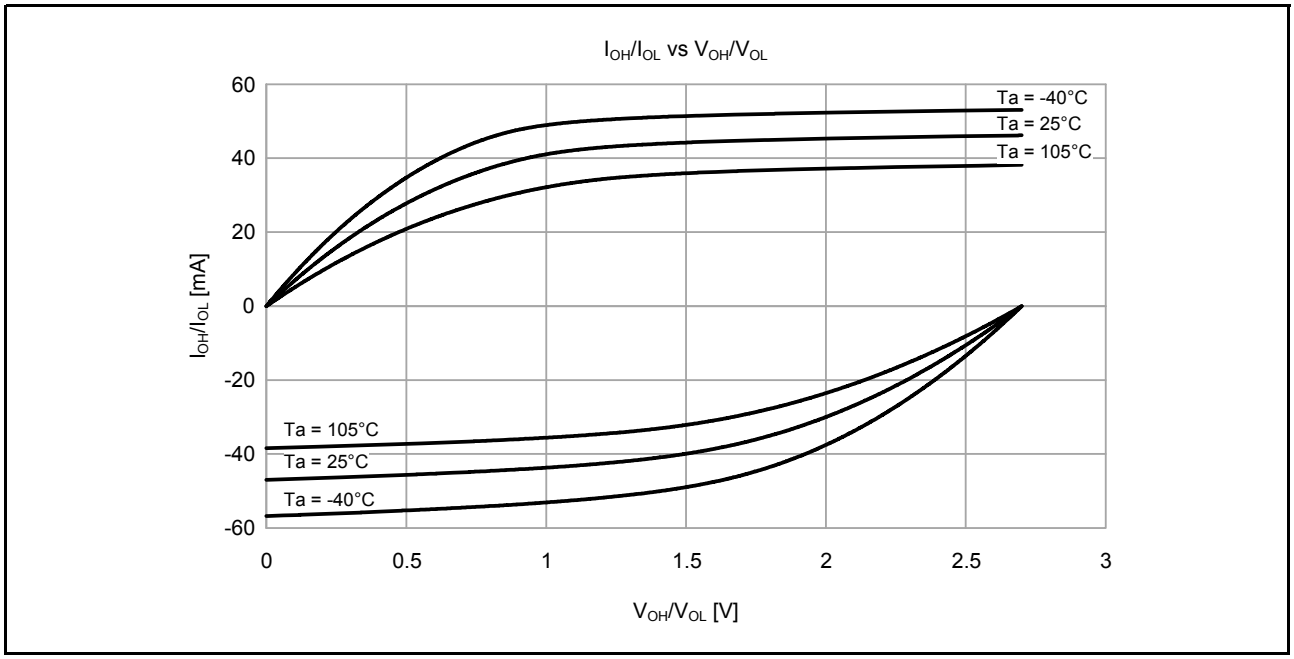
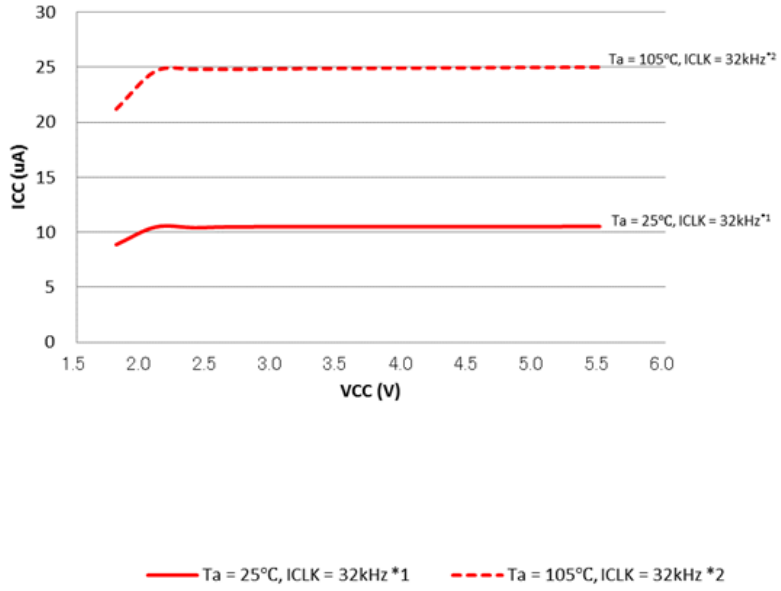



**Figure 2.13** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ temperature characteristics at VCC = 2.7 V when middle drive output is selected (reference data)**




Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.
Note 3. MOCO and DAC are stopped.

**Figure 2.21 Voltage dependency in subosc-speed operating mode (reference data)**

**Table 2.12 Operating and standby current (2)**
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

| Parameter | | | Symbol | Typ*3 | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Supply current*1 | Software Standby mode*2 | $T_a$ = 25°C | $I_{CC}$ | 0.4 | 1.5 | µA | - |
| | | $T_a$ = 55°C | | 0.6 | 5.5 | | |
| | | $T_a$ = 85°C | | 1.2 | 10.0 | | |
| | | $T_a$ = 105°C | | 2.6 | 40.0 | | |
| | Increment for RTC operation with low-speed on-chip oscillator*4 | | | 0.4 | - | | - |
| | Increment for RTC operation with sub-clock oscillator*4 | | | 0.5 | - | | SOMCR.SODRV[1:0] are 11b (Low power mode 3) |
| | | | | 1.3 | - | | SOMCR.SODRV[1:0] are 00b (normal mode) |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOS transistors are in the off state.
Note 2. The IWDT and LVD are not operating.
Note 3. VCC = 3.3 V.
Note 4. Includes the current of low-speed on-chip oscillator or sub-oscillation circuit.

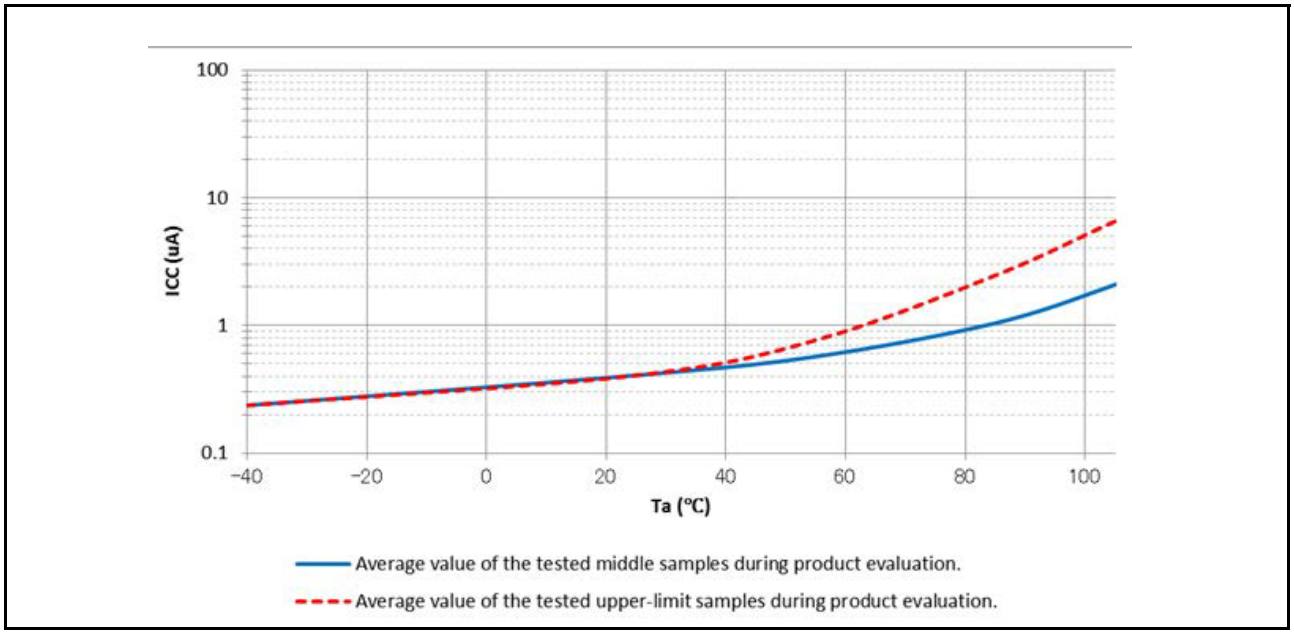



**Figure 2.22 Temperature dependency in Software Standby mode (reference data)**

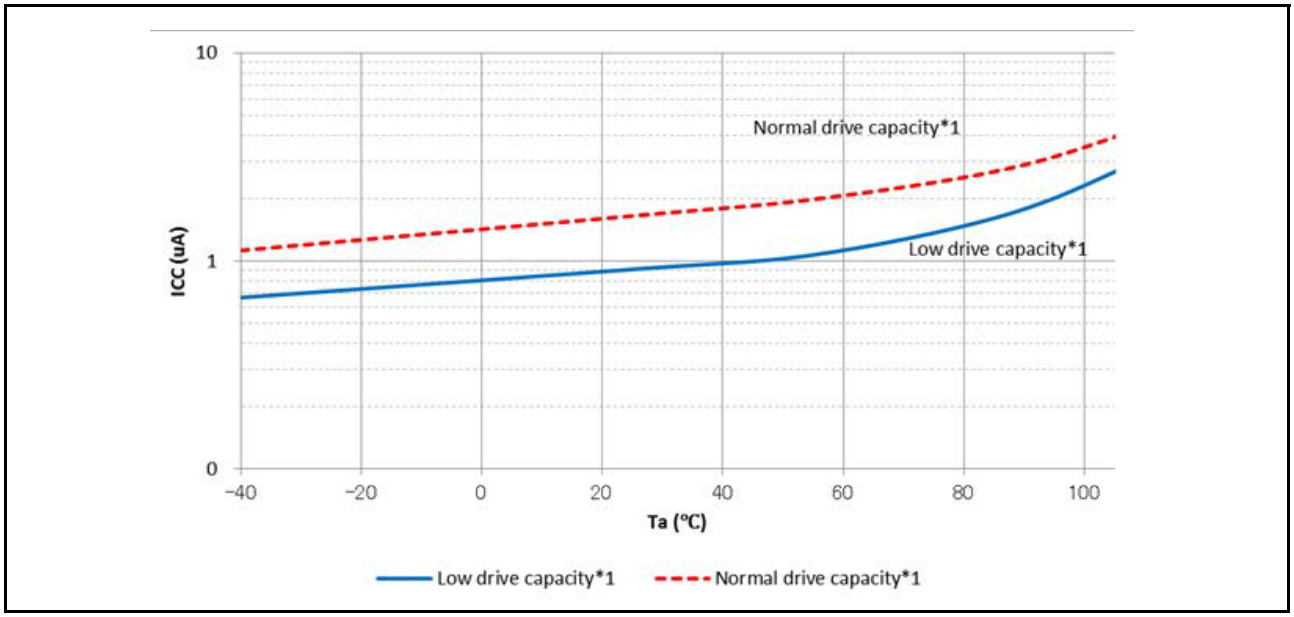



**Figure 2.23 Temperature dependency of RTC operation (reference data)**

**Table 2.13 Operating and standby current (3) (1 of 2)**

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Analog power supply current | During A/D conversion (at high-speed conversion) | $I_{AVCC}$ | - | - | 3.0 | mA | - |
| | During A/D conversion (at low-power conversion) | | - | - | 1.0 | mA | - |
| | During D/A conversion*1 | | - | 0.4 | 0.8 | mA | - |
| | Waiting for A/D and D/A conversion (all units)*5 | | - | - | 1.0 | µA | - |
| Reference power supply current | During A/D conversion | $I_{REFH0}$ | - | - | 150 | µA | - |
| | Waiting for A/D conversion (all units) | | - | - | 60 | nA | - |
| Temperature sensor | | $I_{TNS}$ | - | 75 | - | µA | - |

## 2.2.10 VCC Rise and Fall Gradient and Ripple Frequency

**Table 2.14 Rise and fall gradient characteristics**
Conditions: VCC = AVCC0 = 0 to 5.5 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Power-on VCC rising gradient | Voltage monitor 0 reset disabled at startup | SrVCC | 0.02 | - | 2 | ms/V | - |
| | Voltage monitor 0 reset enabled at startup*1, *2 | | 0.02 | - | - | | |
| | SCI Boot mode*2 | | 0.02 | - | 2 | | |

Note 1. When OFS1.LVDAS = 0.
Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

**Table 2.15 Rising and falling gradient and ripple frequency characteristics**
Conditions: VCC = AVCC0 = 1.6 to 5.5 V
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (1.6 V).
When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Allowable ripple frequency | $f_{r\ (VCC)}$ | - | - | 10 | kHz | Figure 2.24<br>$V_{r\ (VCC)} \leq VCC \times 0.2$ |
| | | - | - | 1 | MHz | Figure 2.24<br>$V_{r\ (VCC)} \leq VCC \times 0.08$ |
| | | - | - | 10 | MHz | Figure 2.24<br>$V_{r\ (VCC)} \leq VCC \times 0.06$ |
| Allowable voltage change rising and falling gradient | dt/dVCC | 1.0 | - | - | ms/V | When VCC change exceeds VCC ±10% |

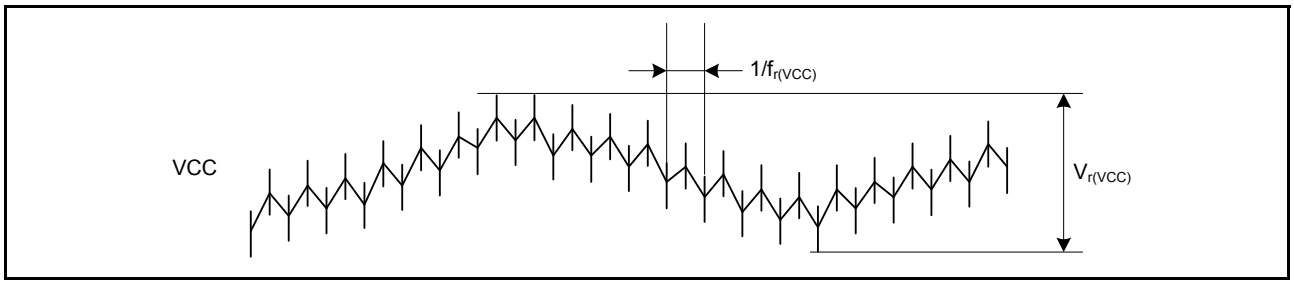



**Figure 2.24 Ripple waveform**

## 2.3.5 NMI and IRQ Noise Filter

**Table 2.29 NMI and IRQ noise filter**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | |
|---|---|---|---|---|---|---|---|
| NMI pulse width | $t_{NMIW}$ | 200 | - | - | ns | NMI digital filter disabled | $t_{Pcyc} \times 2 \leq 200$ ns |
| | | $t_{Pcyc} \times 2$*1 | - | - | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | - | - | | NMI digital filter enabled | $t_{NMICK} \times 3 \leq 200$ ns |
| | | $t_{NMICK} \times 3.5$*2 | - | - | | | $t_{NMICK} \times 3 > 200$ ns |
| IRQ pulse width | $t_{IRQW}$ | 200 | - | - | ns | IRQ digital filter disabled | $t_{Pcyc} \times 2 \leq 200$ ns |
| | | $t_{Pcyc} \times 2$*1 | - | - | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | - | - | | IRQ digital filter enabled | $t_{IRQCK} \times 3 \leq 200$ ns |
| | | $t_{IRQCK} \times 3.5$*3 | - | - | | | $t_{IRQCK} \times 3 > 200$ ns |

Note: 200 ns minimum in Software Standby mode.
Note 1. $t_{Pcyc}$ indicates the PCLKB cycle.
Note 2. $t_{NMICK}$ indicates the cycle of the NMI digital filter sampling clock.
Note 3. $t_{IRQCK}$ indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

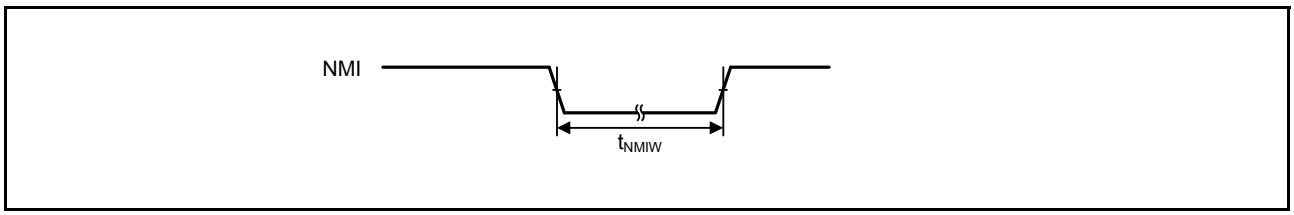



**Figure 2.33 NMI interrupt input timing**

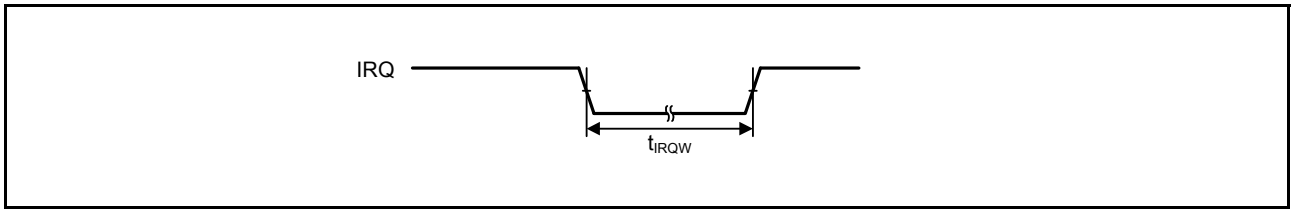



**Figure 2.34 IRQ interrupt input timing**

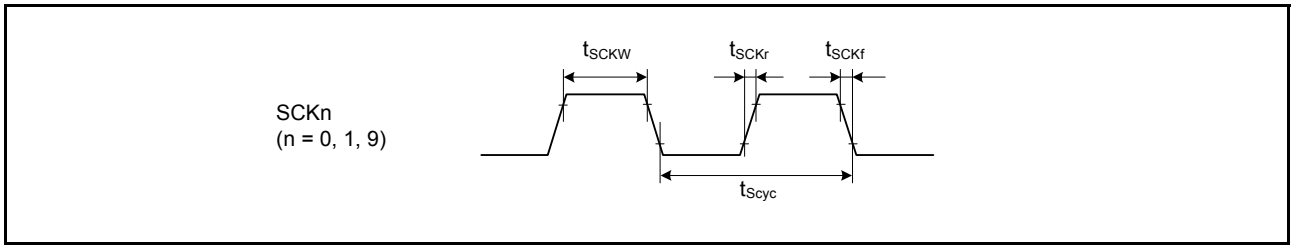



**Figure 2.41 SCK clock input timing**

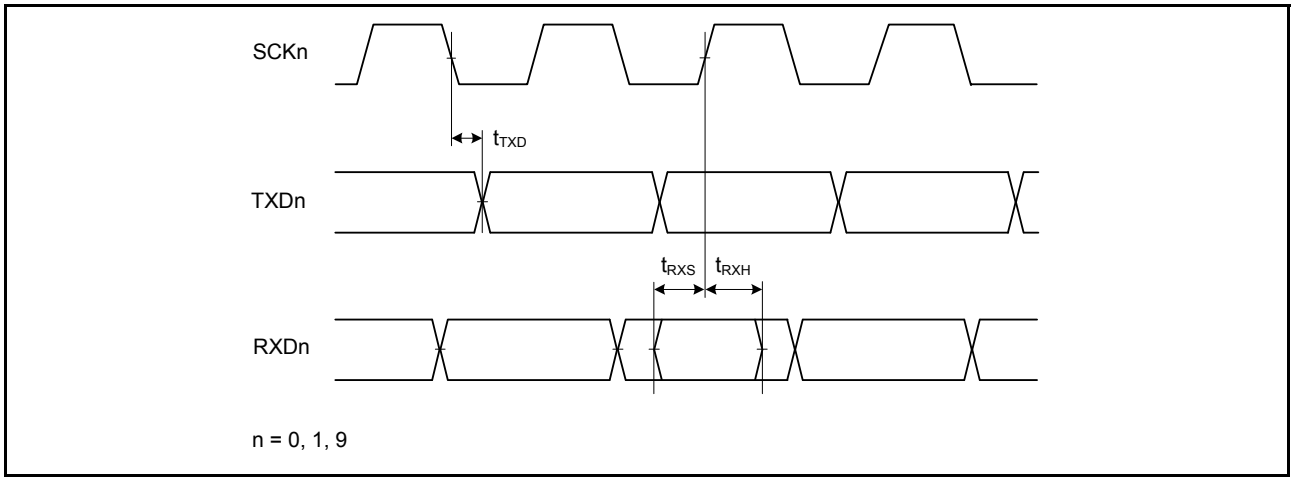



**Figure 2.42 SCI input/output timing in clock synchronous mode**

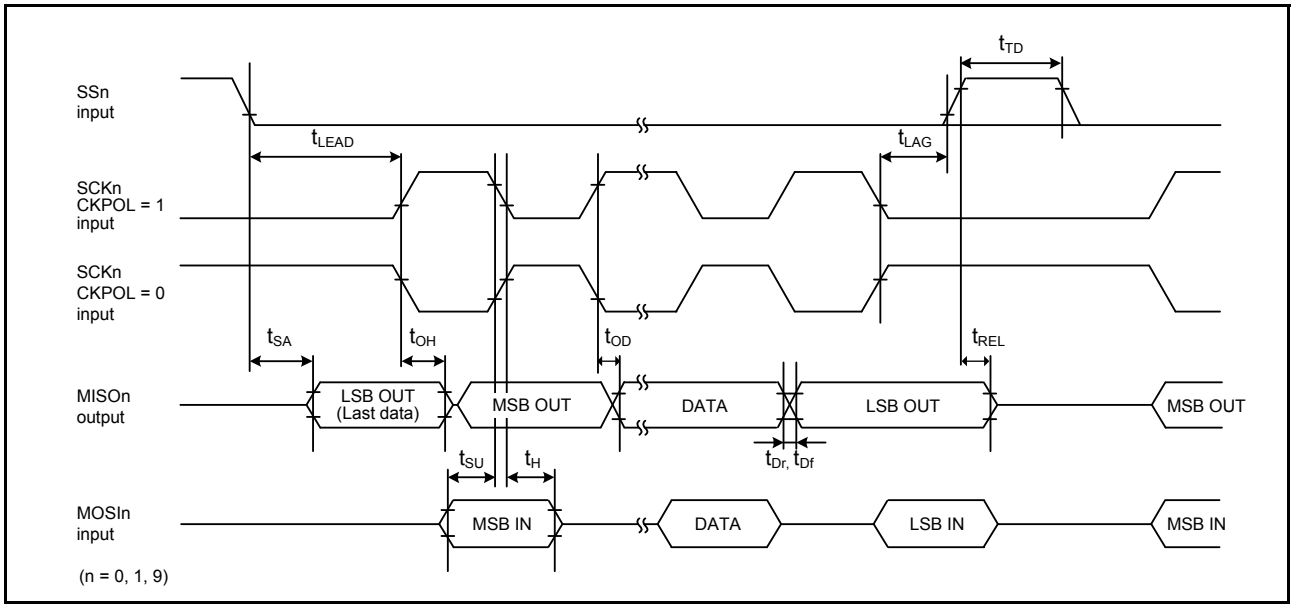



**Figure 2.47 SCI simple SPI mode timing (slave, CKPH = 0)**

**Table 2.34 SCI timing (3)**

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Simple IIC (Standard mode) | SDA input rise time | $t_{Sr}$ | - | 1000 | ns | Figure 2.48 |
| | SDA input fall time | $t_{Sf}$ | - | 300 | ns | |
| | SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{IICcyc}$ | ns | |
| | Data input setup time | $t_{SDAS}$ | 250 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$*1 | - | 400 | pF | |
| Simple IIC*2 (Fast mode) | SDA input rise time | $t_{Sr}$ | - | 300 | ns | Figure 2.48 |
| | SDA input fall time | $t_{Sf}$ | - | 300 | ns | |
| | SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{IICcyc}$ | ns | |
| | Data input setup time | $t_{SDAS}$ | 100 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$*1 | - | 400 | pF | |

Note: $t_{IICcyc}$: Clock cycle selected by the SMR.CKS[1:0] bits.

Note 1. Cb indicates the total capacity of the bus line.

Note 2. Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

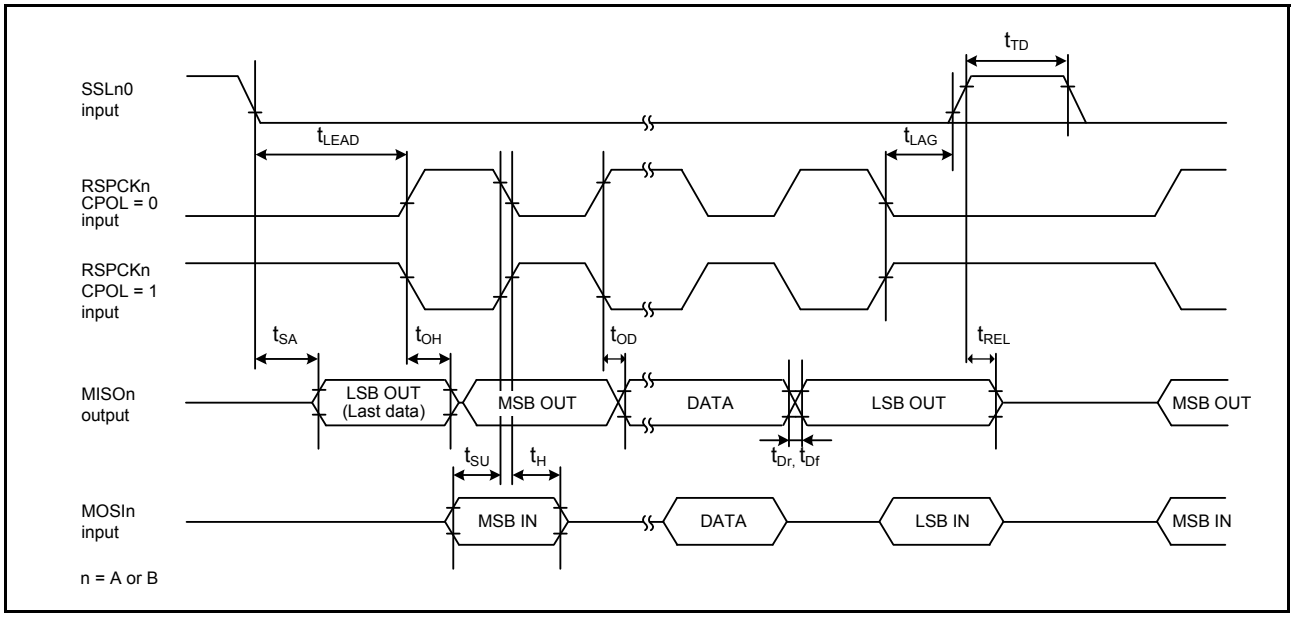



**Figure 2.55 SPI timing (slave, CPHA = 1)**

## 2.3.10 IIC Timing

**Table 2.36 IIC timing**
Conditions: VCC = AVCC0 = 2.7 to 5.5 V

| Parameter | | Symbol | Min*1 | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| IIC (standard mode, SMBus) | SCL input cycle time | $t_{SCL}$ | 6 (12) × $t_{IICcyc}$ + 1300 | - | ns | Figure 2.56 |
| | SCL input high pulse width | $t_{SCLH}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | - | 1000 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | - | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1 (4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time (When wakeup function is disabled) | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SDA input bus free time (When wakeup function is enabled) | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 4 × $t_{Pcyc}$ + 300 | - | ns | |
| | START condition input hold time (When wakeup function is disabled) | $t_{STAH}$ | $t_{IICcyc}$ + 300 | - | ns | |
| | START condition input hold time (When wakeup function is enabled) | $t_{STAH}$ | 1 (5) × $t_{IICcyc}$ + $t_{Pcyc}$ + 300 | - | ns | |
| | Repeated START condition input setup time | $t_{STAS}$ | 1000 | - | ns | |
| | STOP condition input setup time | $t_{STOS}$ | 1000 | - | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$ | - | 400 | pF | |
| IIC*2 (Fast mode) | SCL input cycle time | $t_{SCL}$ | 6 (12) × $t_{IICcyc}$ + 600 | - | ns | Figure 2.56 |
| | SCL input high pulse width | $t_{SCLH}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | - | 300 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | - | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1 (4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time (When wakeup function is disabled) | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SDA input bus free time (When wakeup function is enabled) | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 4 × $t_{Pcyc}$ + 300 | - | ns | |
| | START condition input hold time (When wakeup function is disabled) | $t_{STAH}$ | $t_{IICcyc}$ + 300 | - | ns | |
| | START condition input hold time (When wakeup function is enabled) | $t_{STAH}$ | 1(5) × $t_{IICcyc}$ + $t_{Pcyc}$ + 300 | - | ns | |
| | Repeated START condition input setup time | $t_{STAS}$ | 300 | - | ns | |
| | STOP condition input setup time | $t_{STOS}$ | 300 | - | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$ | - | 400 | pF | |

Note: $t_{IICcyc}$: IIC internal reference clock (IICφ) cycle, $t_{Pcyc}$: PCLKB cycle

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note 2. Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

## 2.3.11 CLKOUT Timing

**Table 2.37 CLKOUT timing**

| Parameter | | | Symbol | Min | Max | Unit*1 | Test conditions |
|---|---|---|---|---|---|---|---|
| CLKOUT | CLKOUT pin output cycle*1 | VCC = 2.7 V or above | $t_{Ccyc}$ | 62.5 | - | ns | Figure 2.57 |
| | | VCC = 1.8 V or above | | 125 | - | | |
| | | VCC = 1.6 V or above | | 250 | - | | |
| | CLKOUT pin high pulse width*2 | VCC = 2.7 V or above | $t_{CH}$ | 15 | - | ns | |
| | | VCC = 1.8 V or above | | 30 | - | | |
| | | VCC = 1.6 V or above | | 150 | - | | |
| | CLKOUT pin low pulse width*2 | VCC = 2.7 V or above | $t_{CL}$ | 15 | - | ns | |
| | | VCC = 1.8 V or above | | 30 | - | | |
| | | VCC = 1.6 V or above | | 150 | - | | |
| | CLKOUT pin output rise time | VCC = 2.7 V or above | $t_{Cr}$ | - | 12 | ns | |
| | | VCC = 1.8 V or above | | - | 25 | | |
| | | VCC = 1.6 V or above | | - | 50 | | |
| | CLKOUT pin output fall time | VCC = 2.7 V or above | $t_{Cf}$ | - | 12 | ns | |
| | | VCC = 1.8 V or above | | - | 25 | | |
| | | VCC = 1.6 V or above | | - | 50 | | |

Note 1. When the EXTAL external clock input or an oscillator is used with division by 1 (the CKOCR.CKOSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

Note 2. When the MOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 001b), set the clock output division ratio selection to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).

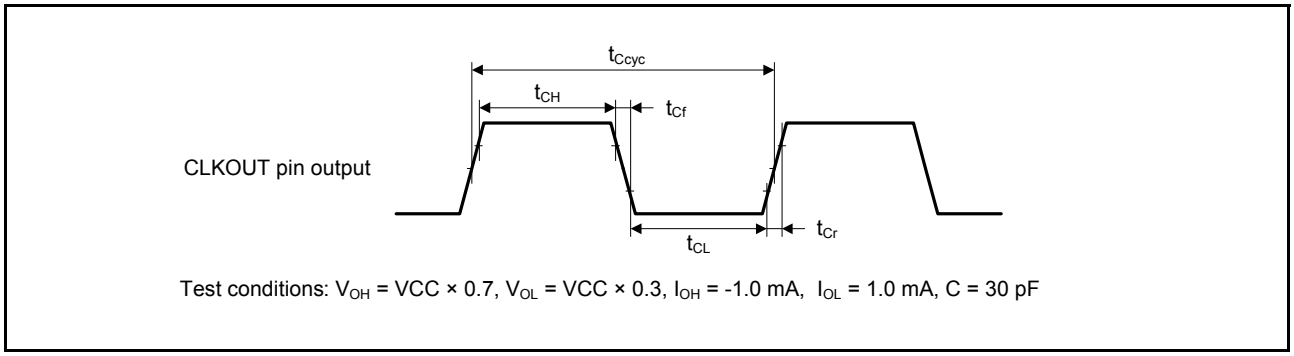



**Figure 2.57 CLKOUT output timing**

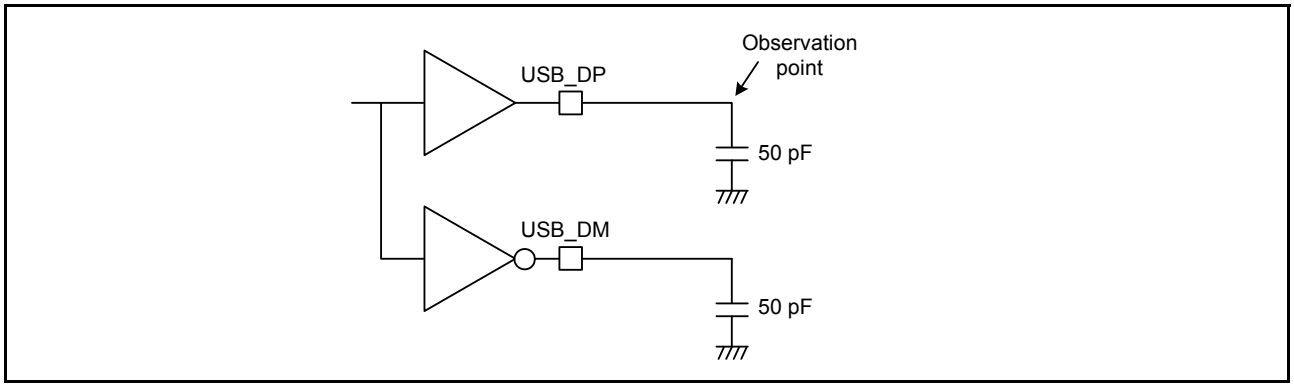



**Figure 2.59 Test circuit for Full-Speed (FS) connection**

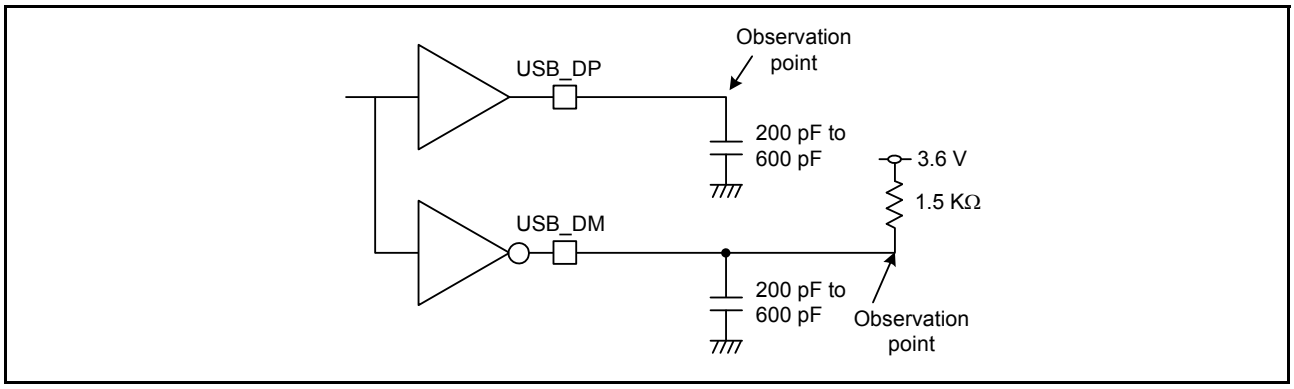



**Figure 2.60 Test circuit for Low-Speed (LS) connection**

### 2.4.2 USB External Supply

**Table 2.39 USB regulator**

| Parameter | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| VCC_USB supply current | VCC_USB_LDO ≥ 3.8V | - | - | 50 | mA | - |
| | VCC_USB_LDO ≥ 4.5V | - | - | 100 | mA | - |
| VCC_USB supply voltage | | 3.0 | - | 3.6 | V | - |

## 2.5 ADC14 Characteristics

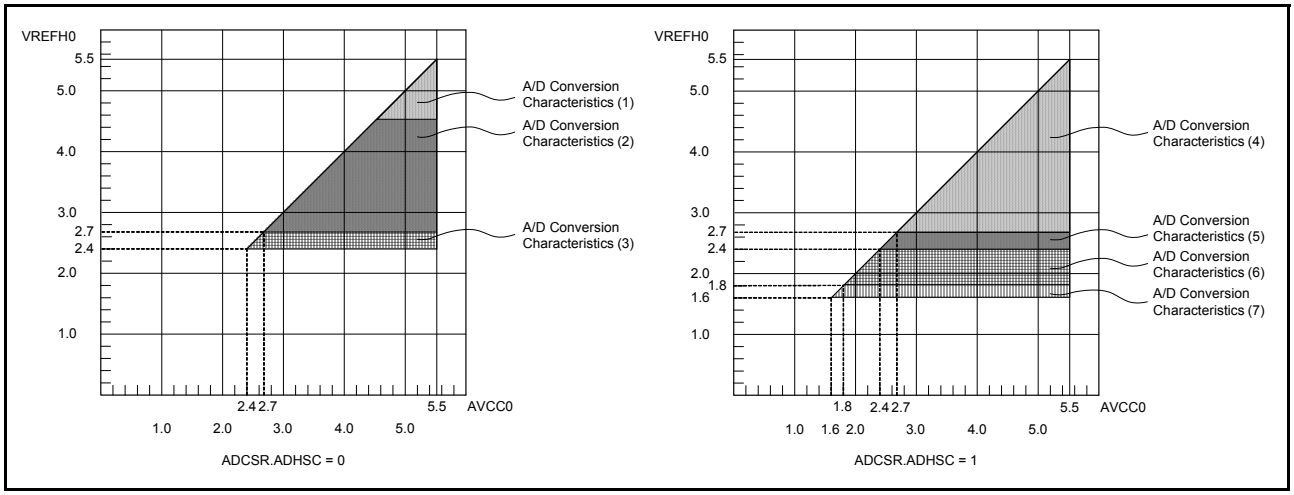



**Figure 2.61 AVCC0 to VREFH0 voltage range**

**Table 2.40 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)**
Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Frequency | | 1 | - | 64 | MHz | - |
| Analog input capacitance*2 | Cs | - | - | 8*3 | pF | High-precision channel |
| | | - | - | 9*3 | pF | Normal-precision channel |
| Analog input resistance | Rs | - | - | 2.5*3 | kΩ | High-precision channel |
| | | - | - | 6.7*3 | kΩ | Normal-precision channel |
| Analog input voltage range | Ain | 0 | - | VREFH0 | V | - |
| 12-bit mode | | | | | | |
| Resolution | | - | - | 12 | Bit | - |
| Conversion time*1 (Operation at PCLKD = 64 MHz) | Permissible signal source impedance Max. = 0.3 kΩ | 0.70 | - | - | µs | High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh |
| | | 1.13 | - | - | µs | Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±0.5 | ±4.5 | LSB | High-precision channel |
| | | | | ±6.0 | LSB | Other than above |
| Full-scale error | | - | ±0.75 | ±4.5 | LSB | High-precision channel |
| | | | | ±6.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±1.25 | ±5.0 | LSB | High-precision channel |
| | | | | ±8.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±1.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±1.0 | ±3.0 | LSB | - |
| 14-bit mode | | | | | | |
| Resolution | | - | - | 14 | Bit | - |

**Table 2.45 A/D conversion characteristics (6) in low-power A/D conversion mode (2 of 2)**
Conditions: VCC = AVCC0 = 1.8 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.8 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

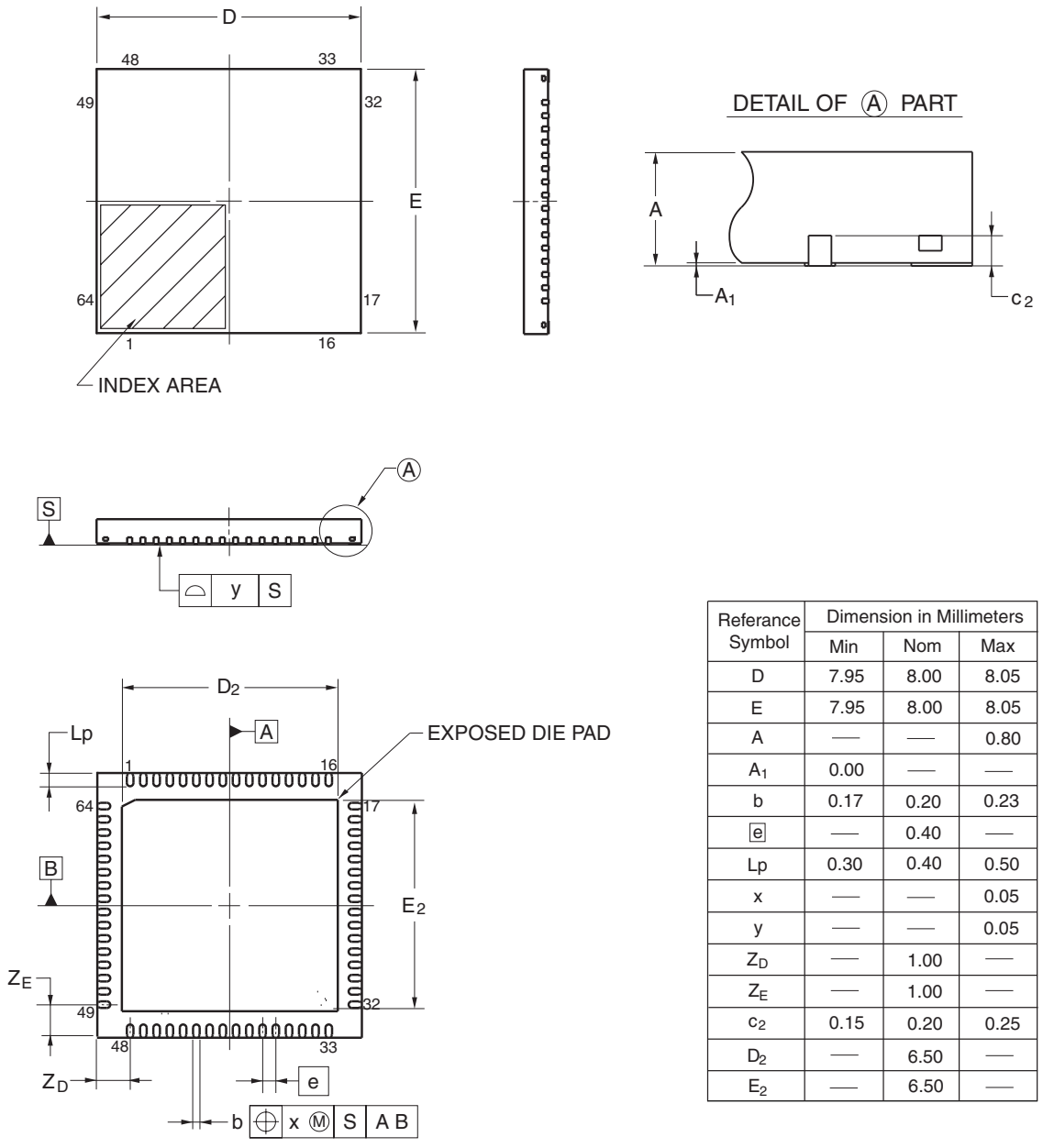
| Parameter | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Conversion time*1 (Operation at PCLKD = 8 MHz) | Permissible signal source impedance Max. = 5 kΩ | 6.75 | - | - | µs | High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh |
| | | 10.13 | - | - | µs | Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±1.0 | ±7.5 | LSB | High-precision channel |
| | | | | ±10.0 | LSB | Other than above |
| Full-scale error | | - | ±1.5 | ±7.5 | LSB | High-precision channel |
| | | | | ±10.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±3.0 | ±8.0 | LSB | High-precision channel |
| | | | | ±12.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±1.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±1.0 | ±3.0 | LSB | - |
| 14-bit mode | | | | | | |
| Resolution | | - | - | 14 | Bit | - |
| Conversion time*1 (Operation at PCLKD = 8 MHz) | Permissible signal source impedance Max. = 5 kΩ | 7.50 | - | - | µs | High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh |
| | | 10.88 | - | - | µs | Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±4.0 | ±30.0 | LSB | High-precision channel |
| | | | | ±40.0 | LSB | Other than above |
| Full-scale error | | - | ±6.0 | ±30.0 | LSB | High-precision channel |
| | | | | ±40.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±12.0 | ±32.0 | LSB | High-precision channel |
| | | | | ±48.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±4.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±4.0 | ±12.0 | LSB | - |

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4, I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.

**Table 2.46 A/D conversion characteristics (7) in low-power A/D conversion mode (1 of 2)**
Conditions: VCC = AVCC0 = 1.6 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.6 to 5.5 V, VSS = AVSS0 = VREFL0 = 0
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Frequency | | 1 | - | 4 | MHz | - |
| Analog input capacitance*2 | Cs | - | - | 8*3 | pF | High-precision channel |
| | | - | - | 9*3 | pF | Normal-precision channel |
| Analog input resistance | Rs | - | - | 13.1*3 | kΩ | High-precision channel |
| | | - | - | 14.3*3 | kΩ | Normal-precision channel |

| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|---|---|---|---|
| P-HWQFN64-8x8-0.40 | PWQN0064LA-A | P64K8-40-9B5-3 | 0.16 |

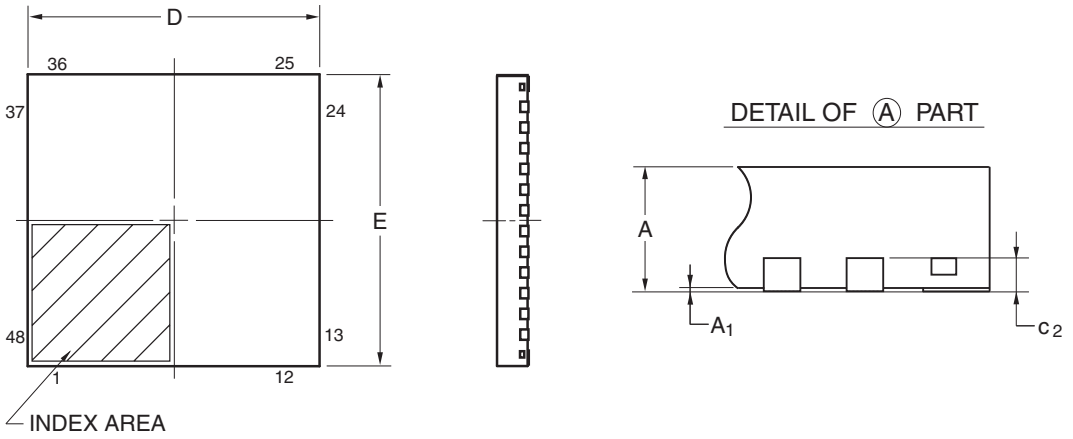


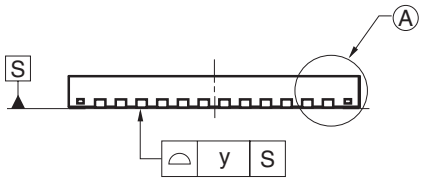

| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 7.95 | 8.00 | 8.05 |
| E | 7.95 | 8.00 | 8.05 |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | — | — |
| b | 0.17 | 0.20 | 0.23 |
| e | — | 0.40 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $Z_D$ | — | 1.00 | — |
| $Z_E$ | — | 1.00 | — |
| $c_2$ | 0.15 | 0.20 | 0.25 |
| $D_2$ | — | 6.50 | — |
| $E_2$ | — | 6.50 | — |

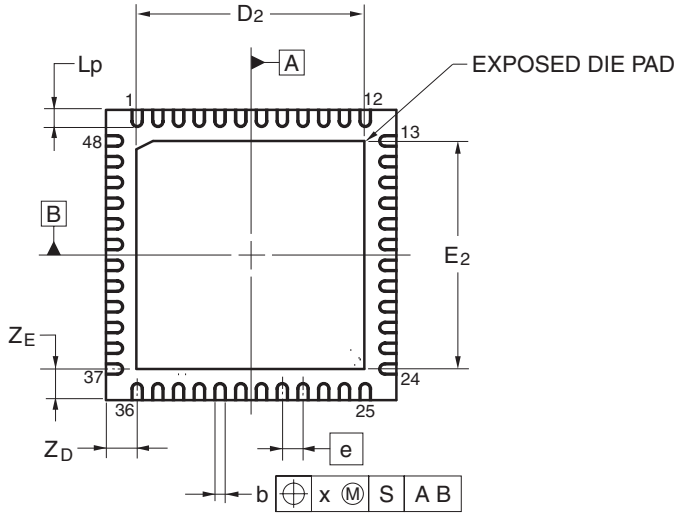


**Figure 1.4 QFN 64-pin**

| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|---|---|---|---|
| P-HWQFN48-7x7-0.50 | PWQN0048KB-A | 48PJN-A<br>P48K8-50-5B4-6 | 0.13 |




| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.95 | 7.00 | 7.05 |
| E | 6.95 | 7.00 | 7.05 |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | — | — |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $Z_D$ | — | 0.75 | — |
| $Z_E$ | — | 0.75 | — |
| $c_2$ | 0.15 | 0.20 | 0.25 |
| $D_2$ | — | 5.50 | — |
| $E_2$ | — | 5.50 | — |



**Figure 1.5 QFN 48-pin**

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