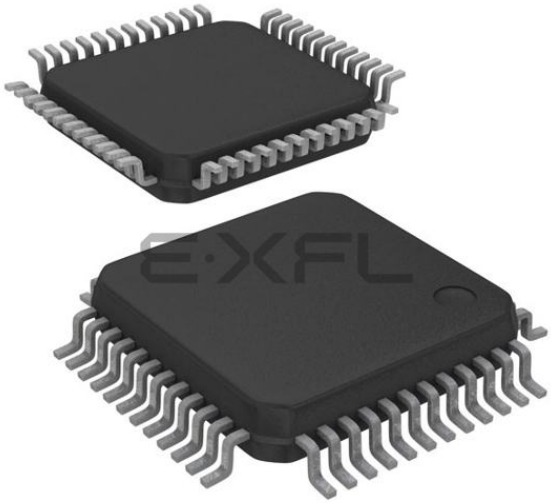
# Renesas Electronics America Inc - R7FS124763A01CFL#AA1 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | CANbus, I²C, SCI, SPI, UART/USART, USB |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 14x14b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LFQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs124763a01cfl-aa1 |

## 1.4 Function Comparison

**Table 1.13 Function comparison**

| Parts number | | R7FS124773A01CFM/ R7FS124763A01CFM/ R7FS124773A01CNB/ | R7FS124773A01CFL/ R7FS124763A01CFL/ R7FS124773A01CNE | R7FS124773A01CNF | R7FS124772A01CLM/ R7FS124762A01CLM |
|---|---|---|---|---|---|
| Pin count | | 64 | 48 | 40 | 36 |
| Package | | LQFP/QFN | LQFP/QFN | QFN | LGA |
| Code flash memory | | 128/64 KB | | | |
| Data flash memory | | 4 KB | | | |
| SRAM | | 16 KB | | | |
| | Parity | 4 KB | | | |
| System | CPU clock | 32 MHz | | | |
| | ICU | Yes | | | |
| | KINT | 8 | 5 | 5 | 4 |
| Event link | ELC | Yes | | | |
| DMA | DTC | Yes | | | |
| Timers | GPT32 | 1 | | | |
| | GPT16 | 6 | 6 | 4 | 4 |
| | AGT | 2 | 2 | 2 | 2 |
| | RTC | Yes | | | |
| | WDT/IWDT | Yes | | | |
| Communication | SCI | 3 | | | |
| | IIC | 2 | | | |
| | SPI | 2 | | | |
| | CAN | Yes | | | |
| | USBFS | Yes | | | |
| Analog | ADC14 | 18 | 14 | 12 | 11 |
| | DAC12 | 1 | | | |
| | ACMPLP | 2 | | | |
| | TSN | Yes | | | |
| HMI | CTSU | 31 | 23 | 17 | 13 |
| | KINT | 8 | 5 | 5 | 4 |
| Data processing | CRC | Yes | | | |
| | DOC | Yes | | | |
| Security | | AES and TRNG | | | |

## 1.6 Pin Assignments

Figure 1.3 to Figure 1.8 show the pin assignments.

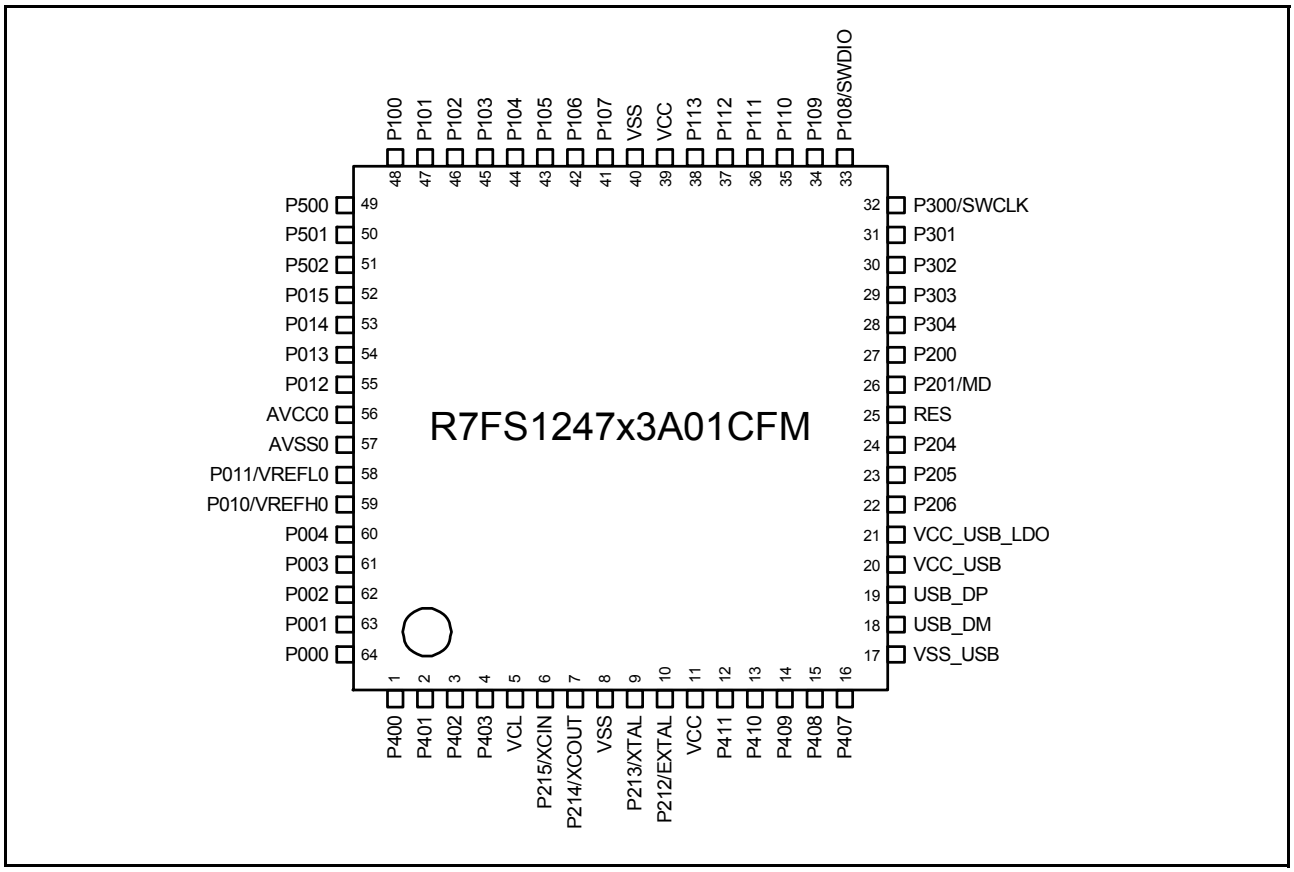



**Figure 1.3 Pin assignment for LQFP 64-pin (top view)**

# 2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC*1 = AVCC0 = VCC_USB*2 = VCC_USB_LDO*2 = 1.6 to 5.5V, VREFH0 = 1.6 to AVCC0,

VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, Ta = $T_{opr}$

Note 1. The typical condition is set to VCC = 3.3V.
Note 2. When USBFS is not used.

Figure 2.1 shows the timing conditions.

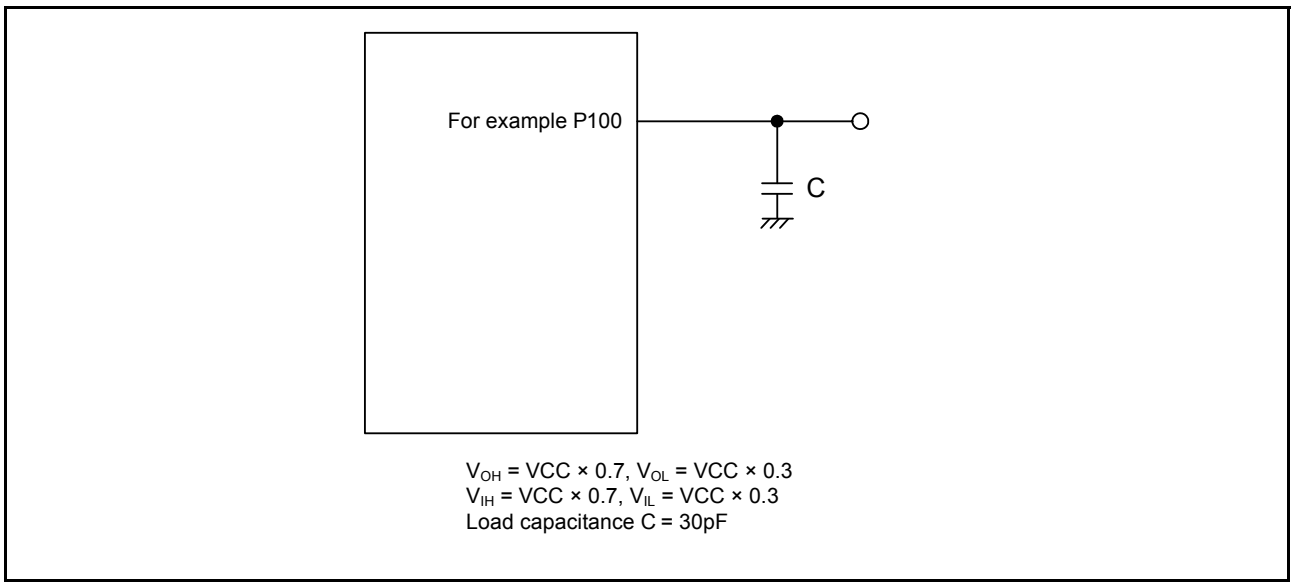



**Figure 2.1 Input or output timing measurement conditions**

The measurement conditions of timing specification in each peripherals are recommended for the best peripheral operation. However, make sure to adjust driving abilities of each pins to meet your conditions.

Each function pin used for the same function must select the same drive ability. If I/O drive ability of each function is mixed, the AC specification of the function is not guaranteed.

**Table 2.5 I/O $V_{IH}$, $V_{IL}$ (2)**
Conditions: VCC = AVCC0 = 1.6 to 2.7 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | RES, NMI<br>Peripheral input pins | $V_{IH}$ | VCC × 0.8 | - | - | V | - |
| | | $V_{IL}$ | - | - | VCC × 0.2 | | |
| | | $\Delta V_T$ | VCC × 0.01 | - | - | | |
| Input voltage (except for Schmitt trigger input pin) | 5V-tolerant ports*1 | $V_{IH}$ | VCC × 0.8 | - | 5.8 | | |
| | | $V_{IL}$ | - | - | VCC × 0.2 | | |
| | P000 to P004<br>P010 to P015 | $V_{IH}$ | AVCC0 × 0.8 | - | - | | |
| | | $V_{IL}$ | - | - | AVCC0 × 0.2 | | |
| | EXTAL<br>Input ports pins except for P000 to P004, P010 to P015 | $V_{IH}$ | VCC × 0.8 | - | - | | |
| | | $V_{IL}$ | - | - | VCC × 0.2 | | |

Note 1. P205, P206, P400, P401, P407 (total 5pins)

## 2.2.3 I/O $I_{OH}$, $I_{OL}$

**Table 2.6 I/O $I_{OH}$, $I_{OL}$**
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

| Parameter | | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Permissible output current (average value per pin) | Ports P000 to P004, P010 to P015, P212, P213 | - | $I_{OH}$ | - | - | –4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | Ports P408, P409 | Low drive*1 | $I_{OH}$ | - | - | –4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | | Middle drive*2 VCC = 2.7 to 3.0 V | $I_{OH}$ | - | - | –8.0 | mA |
| | | | $I_{OL}$ | - | - | 8.0 | mA |
| | | Middle drive*2 VCC = 3.0 to 5.5 V | $I_{OH}$ | - | - | –20.0 | mA |
| | | | $I_{OL}$ | - | - | 20.0 | mA |
| | Other output pins*3 | Low drive*1 | $I_{OH}$ | - | - | –4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | | Middle drive*2 | $I_{OH}$ | - | - | –8.0 | mA |
| | | | $I_{OL}$ | - | - | 8.0 | mA |
| Permissible output current (max value per pin) | Ports P000 to P004, P010 to P015, P212, P213 | - | $I_{OH}$ | - | - | –4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | Ports P408, P409 | Low drive*1 | $I_{OH}$ | - | - | –4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | | Middle drive*2 VCC = 2.7 to 3.0 V | $I_{OH}$ | - | - | –8.0 | mA |
| | | | $I_{OL}$ | - | - | 8.0 | mA |
| | | Middle drive*2 VCC = 3.0 to 5.5 V | $I_{OH}$ | - | - | –20.0 | mA |
| | | | $I_{OL}$ | - | - | 20.0 | mA |
| | Other output pins*3 | Low drive*1 | $I_{OH}$ | - | - | –4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | | Middle drive*2 | $I_{OH}$ | - | - | –8.0 | mA |
| | | | $I_{OL}$ | - | - | 8.0 | mA |
| Permissible output current (max value total pins) | Total of ports P000 to P004, P010 to P015 | | $\Sigma I_{OH\ (max)}$ | - | - | –30 | mA |
| | | | $\Sigma I_{OL\ (max)}$ | - | - | 30 | mA |
| | Total of all output pin | | $\Sigma I_{OH\ (max)}$ | - | - | –60 | mA |
| | | | $\Sigma I_{OL\ (max)}$ | - | - | 60 | mA |

**Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.**

Note 1. This is the value when low driving ability is selected with the Port Drive Capability bit in the PmnPFS register.

Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the register.

Note 3. Except for Ports P200, P214, P215, which are input ports.

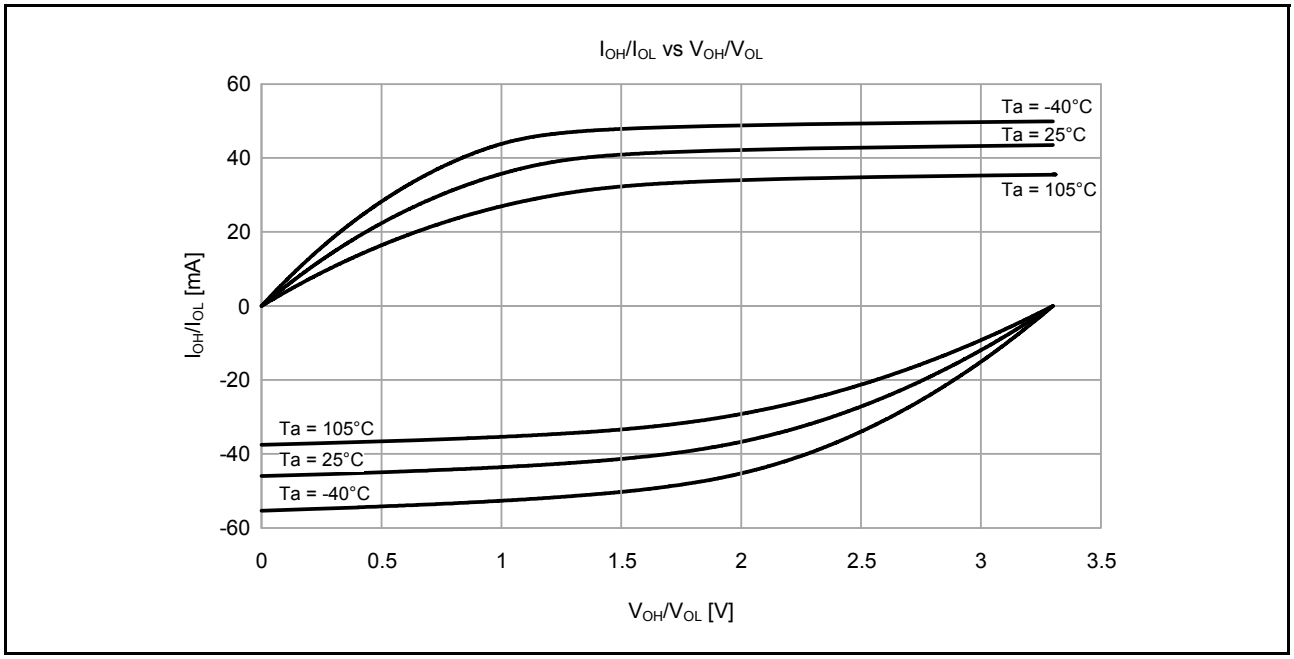



**Figure 2.10** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ temperature characteristics at VCC = 3.3 V when middle drive output is selected (reference data)**

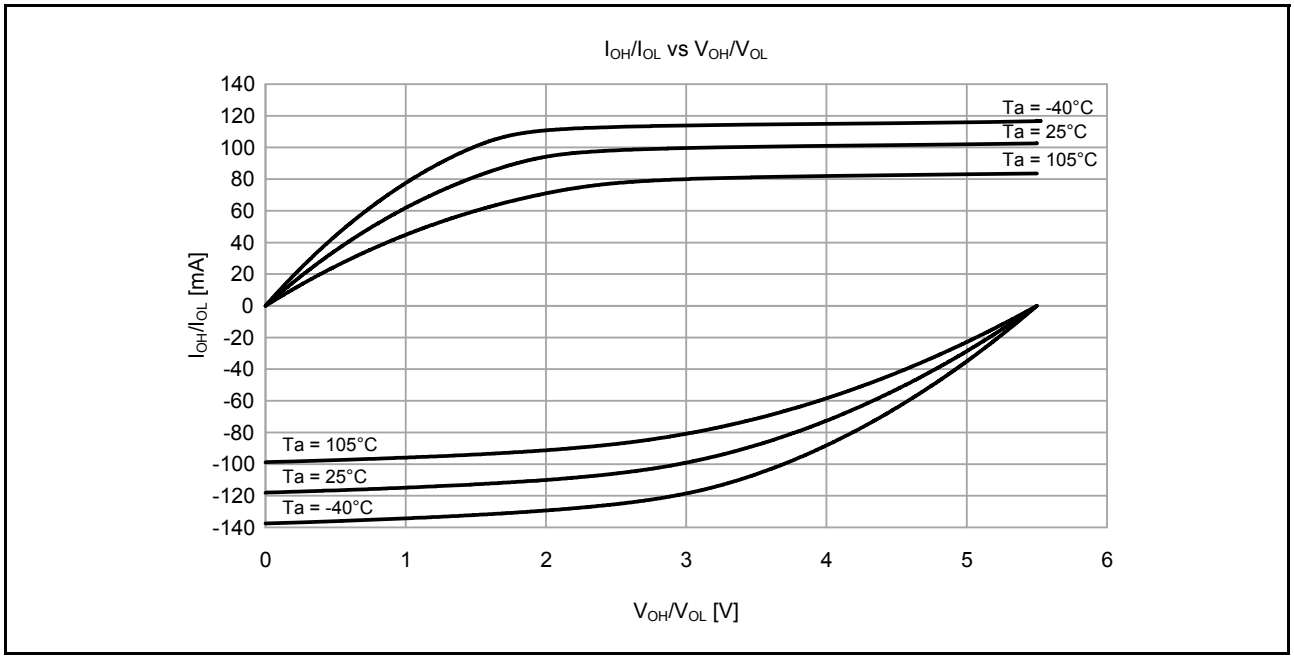



**Figure 2.11** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ temperature characteristics at VCC = 5.5 V when middle drive output is selected (reference data)**

### 2.2.7 P408, P409 I/O Pin Output Characteristics of Middle Drive Capacity

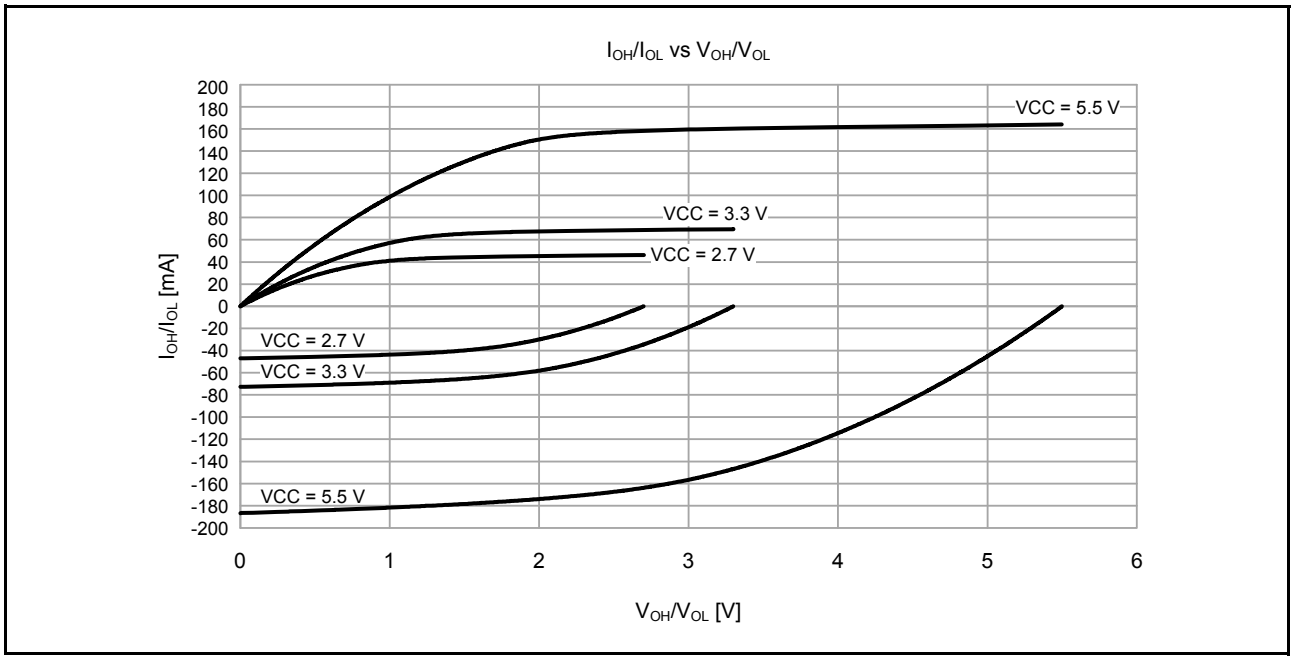



**Figure 2.12** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ voltage characteristics at Ta = 25°C when middle drive output is selected (reference data)**

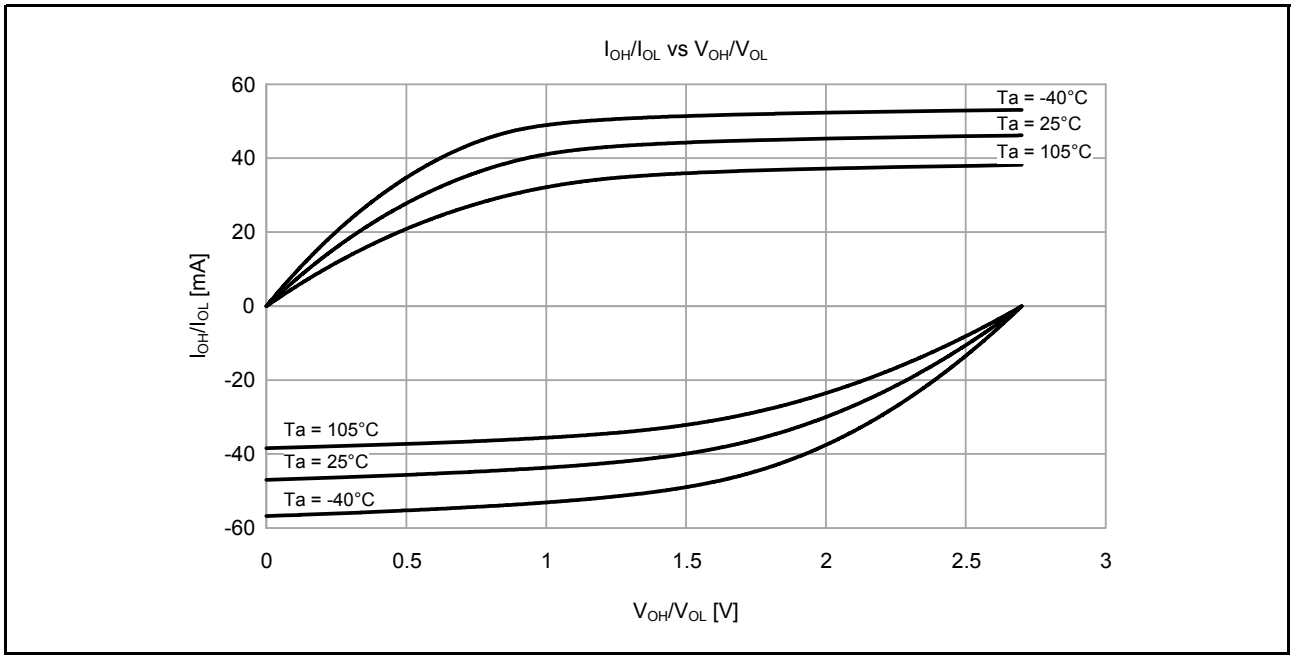



**Figure 2.13** **$V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ temperature characteristics at VCC = 2.7 V when middle drive output is selected (reference data)**

### 2.2.8 IIC I/O Pin Output Characteristics

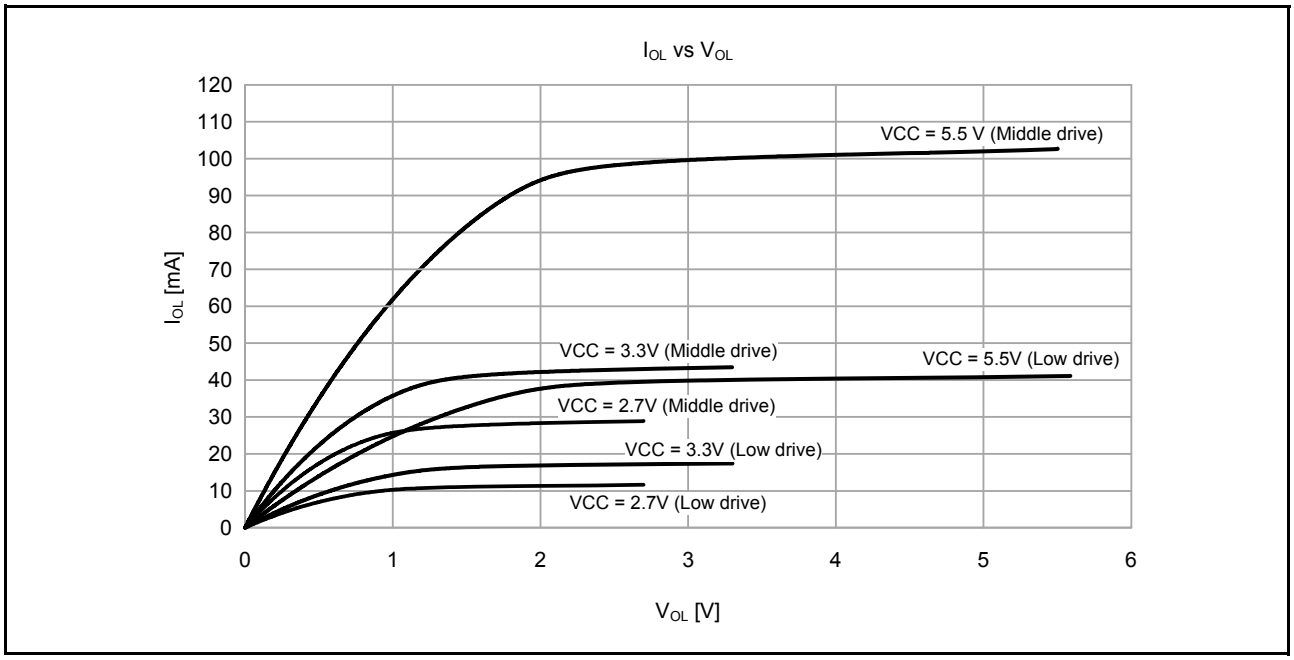
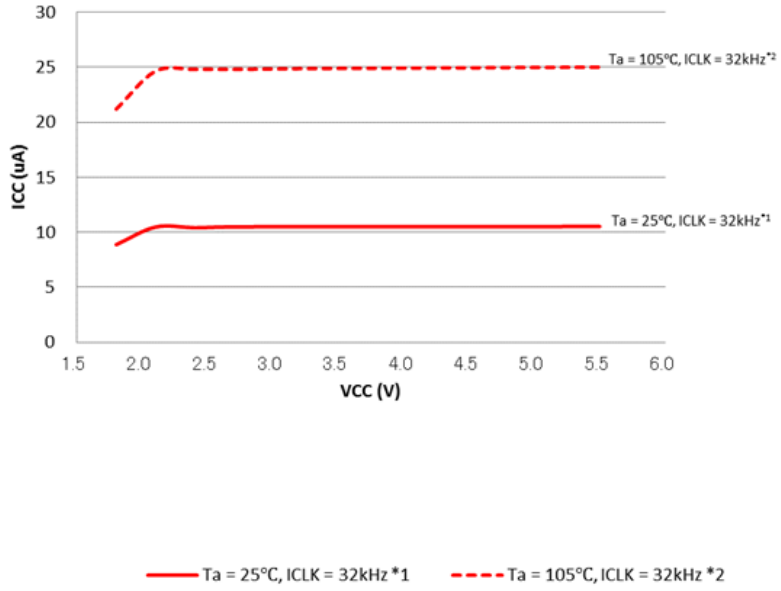



**Figure 2.16 $V_{OH}/V_{OL}$ and $I_{OH}/I_{OL}$ voltage characteristics at Ta = 25°C**




Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.
Note 3. MOCO and DAC are stopped.

**Figure 2.21 Voltage dependency in subosc-speed operating mode (reference data)**

**Table 2.12 Operating and standby current (2)**
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

| Parameter | | | Symbol | Typ*3 | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Supply current*1 | Software Standby mode*2 | $T_a$ = 25°C | $I_{CC}$ | 0.4 | 1.5 | µA | - |
| | | $T_a$ = 55°C | | 0.6 | 5.5 | | |
| | | $T_a$ = 85°C | | 1.2 | 10.0 | | |
| | | $T_a$ = 105°C | | 2.6 | 40.0 | | |
| | Increment for RTC operation with low-speed on-chip oscillator*4 | | | 0.4 | - | | - |
| | Increment for RTC operation with sub-clock oscillator*4 | | | 0.5 | - | | SOMCR.SODRV[1:0] are 11b (Low power mode 3) |
| | | | | 1.3 | - | | SOMCR.SODRV[1:0] are 00b (normal mode) |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOS transistors are in the off state.
Note 2. The IWDT and LVD are not operating.
Note 3. VCC = 3.3 V.
Note 4. Includes the current of low-speed on-chip oscillator or sub-oscillation circuit.

## 2.2.10 VCC Rise and Fall Gradient and Ripple Frequency

**Table 2.14 Rise and fall gradient characteristics**
Conditions: VCC = AVCC0 = 0 to 5.5 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Power-on VCC rising gradient | Voltage monitor 0 reset disabled at startup | SrVCC | 0.02 | - | 2 | ms/V | - |
| | Voltage monitor 0 reset enabled at startup*1, *2 | | 0.02 | - | - | | |
| | SCI Boot mode*2 | | 0.02 | - | 2 | | |

Note 1. When OFS1.LVDAS = 0.
Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

**Table 2.15 Rising and falling gradient and ripple frequency characteristics**
Conditions: VCC = AVCC0 = 1.6 to 5.5 V
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (1.6 V).
When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Allowable ripple frequency | $f_{r\ (VCC)}$ | - | - | 10 | kHz | Figure 2.24<br>$V_{r\ (VCC)} \leq VCC \times 0.2$ |
| | | - | - | 1 | MHz | Figure 2.24<br>$V_{r\ (VCC)} \leq VCC \times 0.08$ |
| | | - | - | 10 | MHz | Figure 2.24<br>$V_{r\ (VCC)} \leq VCC \times 0.06$ |
| Allowable voltage change rising and falling gradient | dt/dVCC | 1.0 | - | - | ms/V | When VCC change exceeds VCC ±10% |

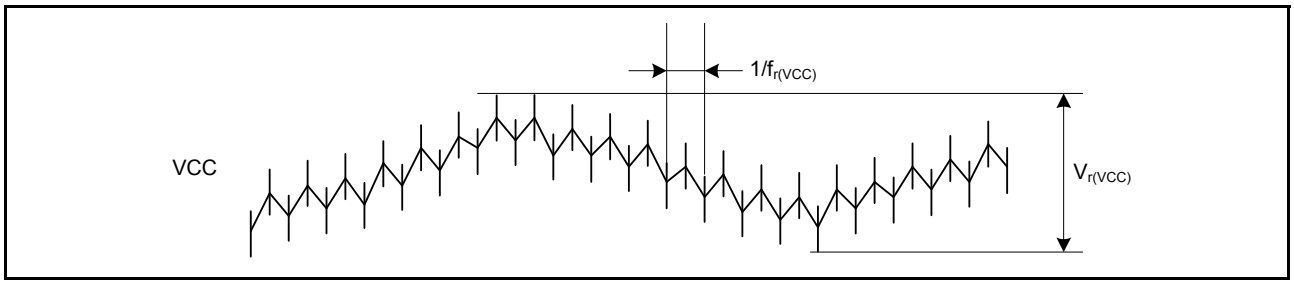



**Figure 2.24 Ripple waveform**

## 2.3.2 Clock Timing

**Table 2.21 Clock timing (1 of 2)**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| EXTAL external clock input cycle time | | $t_{Xcyc}$ | 50 | - | - | ns | Figure 2.25 |
| EXTAL external clock input high pulse width | | $t_{XH}$ | 20 | - | - | ns | |
| EXTAL external clock input low pulse width | | $t_{XL}$ | 20 | - | - | ns | |
| EXTAL external clock rising time | | $t_{Xr}$ | - | - | 5 | ns | |
| EXTAL external clock falling time | | $t_{Xf}$ | - | - | 5 | ns | |
| EXTAL external clock input wait time*1 | | $t_{EXWT}$ | 0.3 | - | - | μs | - |
| EXTAL external clock input frequency | | $f_{EXTAL}$ | - | - | 20 | MHz | 2.4 ≤ VCC ≤ 5.5 |
| | | | - | - | 8 | | 1.8 ≤ VCC < 2.4 |
| | | | - | - | 1 | | 1.6 ≤ VCC < 1.8 |
| Main clock oscillator oscillation frequency | | $f_{MAIN}$ | 1 | - | 20 | MHz | 2.4 ≤ VCC ≤ 5.5 |
| | | | 1 | - | 8 | | 1.8 ≤ VCC < 2.4 |
| | | | 1 | - | 4 | | 1.6 ≤ VCC < 1.8 |
| LOCO clock oscillation frequency | | $f_{LOCO}$ | 27.8528 | 32.768 | 37.6832 | kHz | - |
| LOCO clock oscillation stabilization time | | $t_{LOCO}$ | - | - | 100 | μs | Figure 2.26 |
| IWDT-dedicated clock oscillation frequency | | $f_{ILOCO}$ | 12.75 | 15 | 17.25 | kHz | - |
| MOCO clock oscillation frequency | | $f_{MOCO}$ | 6.8 | 8 | 9.2 | MHz | - |
| MOCO clock oscillation stabilization time | | $t_{MOCO}$ | - | - | 1 | μs | - |
| HOCO clock oscillation frequency | | $f_{HOCO24}$ | 23.64 | 24 | 24.36 | MHz | Ta = –40 to –20°C<br>1.8 ≤ VCC ≤ 5.5 |
| | | | 22.68 | 24 | 25.32 | | Ta = –40 to 85°C<br>1.6 ≤ VCC < 1.8 |
| | | | 23.76 | 24 | 24.24 | | Ta = –20 to 85°C<br>1.8 ≤ VCC ≤ 5.5 |
| | | | 23.52 | 24 | 24.48 | | Ta = 85 to 105°C<br>2.4 ≤ VCC ≤ 5.5 |
| | | $f_{HOCO32}$ | 31.52 | 32 | 32.48 | | Ta = –40 to –20°C<br>1.8 ≤ VCC ≤ 5.5 |
| | | | 30.24 | 32 | 33.76 | | Ta = –40 to 85°C<br>1.6 ≤ VCC < 1.8 |
| | | | 31.68 | 32 | 32.32 | | Ta = –20 to 85°C<br>1.8 ≤ VCC ≤ 5.5 |
| | | | 31.36 | 32 | 32.64 | | Ta = 85 to 105°C<br>2.4 ≤ VCC ≤ 5.5 |
| | | $f_{HOCO48}$*3 | 47.28 | 48 | 48.72 | | Ta = –40 to –20°C<br>1.8 ≤ VCC ≤ 5.5 |
| | | | 47.52 | 48 | 48.48 | | Ta = –20 to 85°C<br>1.8 ≤ VCC ≤ 5.5 |
| | | | 47.04 | 48 | 48.96 | | Ta = 85 to 105°C<br>2.4 ≤ VCC ≤ 5.5 |
| | | $f_{HOCO64}$*4 | 63.04 | 64 | 64.96 | | Ta = –40 to –20°C<br>2.4 ≤ VCC ≤ 5.5 |
| | | | 63.36 | 64 | 64.64 | | Ta = –20 to 85°C<br>2.4 ≤ VCC ≤ 5.5 |
| | | | 62.72 | 64 | 65.28 | | Ta = 85 to 105°C<br>2.4 ≤ VCC ≤ 5.5 |
| HOCO clock oscillation stabilization time*5, *6 | Except low-voltage mode | $t_{HOCO24}$<br>$t_{HOCO32}$ | - | - | 37.1 | μs | Figure 2.27 |
| | | $t_{HOCO48}$ | - | - | 43.3 | | |
| | | $t_{HOCO64}$ | - | - | 80.6 | | |
| | Low-voltage mode | $t_{HOCO24}$<br>$t_{HOCO32}$<br>$t_{HOCO48}$<br>$t_{HOCO64}$ | - | - | 100.9 | | |
| Sub-clock oscillator oscillation frequency | | $f_{SUB}$ | - | 32.768 | - | kHz | - |

## 2.3.4 Wakeup Time

**Table 2.23 Timing of recovery from low power modes (1)**

| Parameter | | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|
| Recovery time from Software Standby mode*1 | High-speed mode | Crystal resonator connected to main clock oscillator | System clock source is main clock oscillator (20 MHz)*2 | $t_{SBYMC}$ | - | 2 | 3 | ms | Figure 2.31 |
| | | External clock input to main clock oscillator | System clock source is main clock oscillator (20 MHz)*3 | $t_{SBYEX}$ | - | 14 | 25 | µs | |
| | | System clock source is HOCO*4 (HOCO clock is 32 MHz) | | $t_{SBYHO}$ | - | 43 | 52 | µs | |
| | | System clock source is HOCO*4 (HOCO clock is 48 MHz) | | $t_{SBYHO}$ | - | 44 | 52 | µs | |
| | | System clock source is HOCO*5 (HOCO clock is 64 MHz) | | $t_{SBYHO}$ | - | 82 | 110 | µs | |
| | | System clock source is MOCO | | $t_{SBYMO}$ | - | 16 | 25 | µs | |

Note 1. The division ratio of ICK and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.
Note 4. The HOCO clock wait control register (HOCOWTCR) is set to 05h.
Note 5. The HOCO clock wait control register (HOCOWTCR) is set to 06h.

**Table 2.24 Timing of recovery from low power modes (2)**

| Parameter | | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|
| Recovery time from Software Standby mode*1 | Middle-speed mode | Crystal resonator connected to main clock oscillator | System clock source is main clock oscillator (12 MHz)*2 | $t_{SBYMC}$ | - | 2 | 3 | ms | Figure 2.31 |
| | | External clock input to main clock oscillator | System clock source is main clock oscillator (12 MHz)*3 | $t_{SBYEX}$ | - | 2.9 | 10 | µs | |
| | | System clock source is HOCO*4 | | $t_{SBYHO}$ | - | 38 | 50 | µs | |
| | | System clock source is MOCO | | $t_{SBYMO}$ | - | 3.5 | 5.5 | µs | |

Note 1. The division ratio of ICK and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.
Note 4. The system clock is 12 MHz.

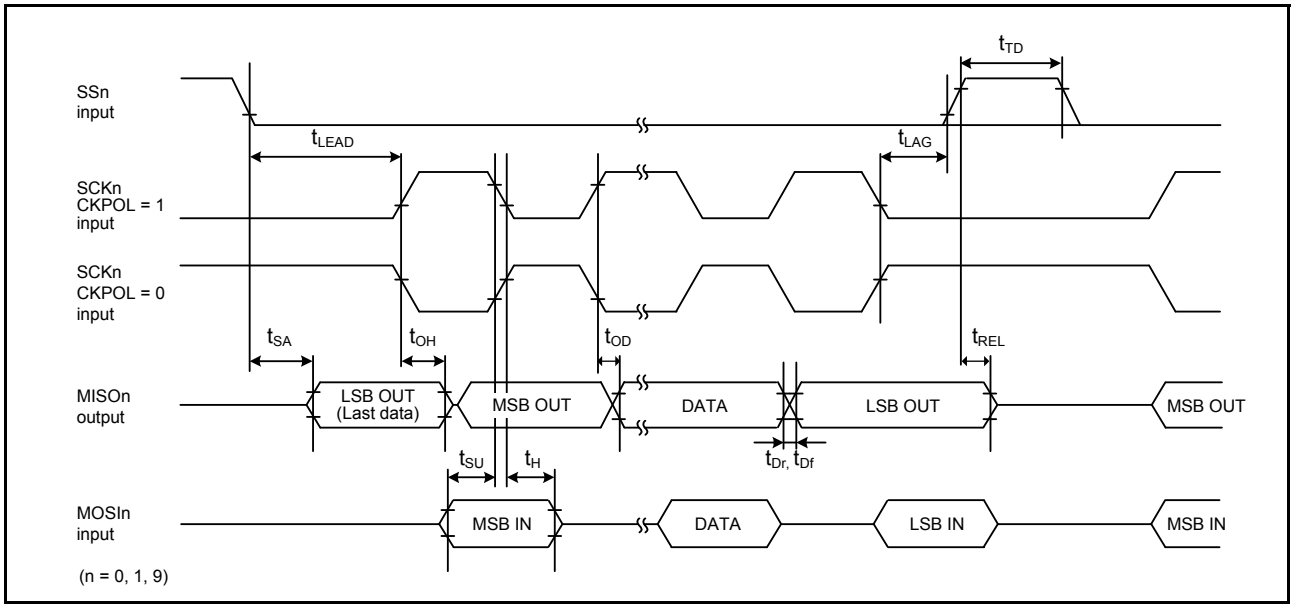



**Figure 2.47 SCI simple SPI mode timing (slave, CKPH = 0)**

**Table 2.34 SCI timing (3)**

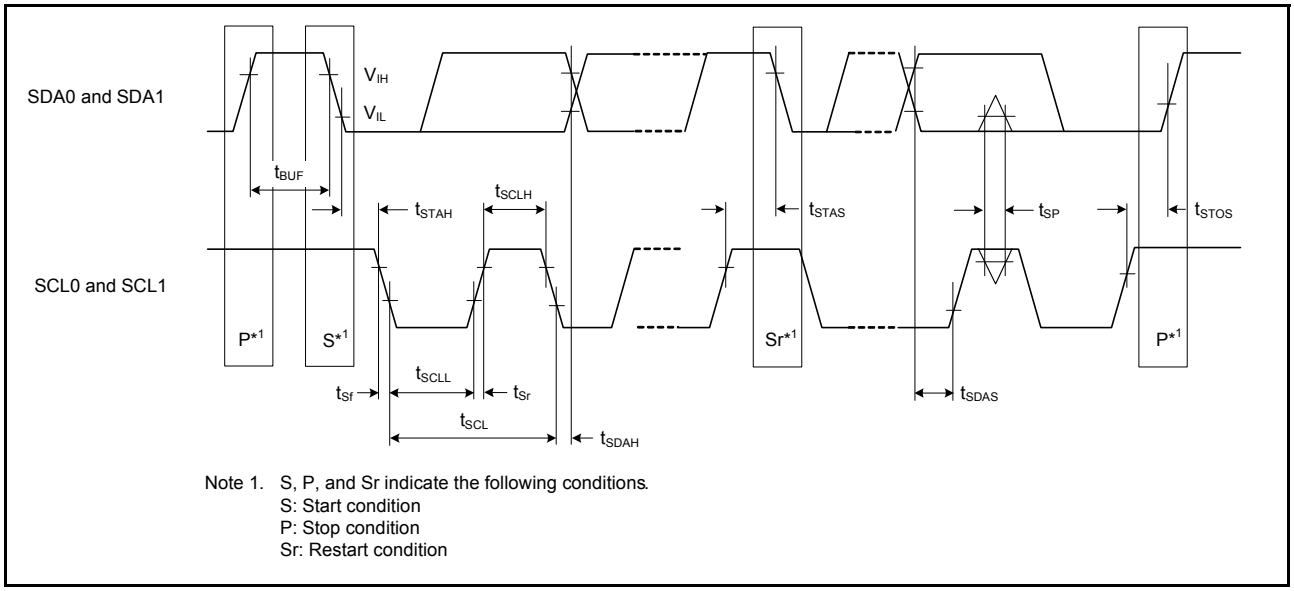
Conditions: VCC = AVCC0 = 2.7 to 5.5 V

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Simple IIC (Standard mode) | SDA input rise time | $t_{Sr}$ | - | 1000 | ns | Figure 2.48 |
| | SDA input fall time | $t_{Sf}$ | - | 300 | ns | |
| | SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{IICcyc}$ | ns | |
| | Data input setup time | $t_{SDAS}$ | 250 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$*1 | - | 400 | pF | |
| Simple IIC*2 (Fast mode) | SDA input rise time | $t_{Sr}$ | - | 300 | ns | Figure 2.48 |
| | SDA input fall time | $t_{Sf}$ | - | 300 | ns | |
| | SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{IICcyc}$ | ns | |
| | Data input setup time | $t_{SDAS}$ | 100 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$*1 | - | 400 | pF | |

Note: $t_{IICcyc}$: Clock cycle selected by the SMR.CKS[1:0] bits.

Note 1. Cb indicates the total capacity of the bus line.

Note 2. Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.




Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

**Figure 2.56 I²C bus interface input/output timing**

## 2.3.11 CLKOUT Timing

**Table 2.37 CLKOUT timing**

| Parameter | | | Symbol | Min | Max | Unit*1 | Test conditions |
|---|---|---|---|---|---|---|---|
| CLKOUT | CLKOUT pin output cycle*1 | VCC = 2.7 V or above | $t_{Ccyc}$ | 62.5 | - | ns | Figure 2.57 |
| | | VCC = 1.8 V or above | | 125 | - | | |
| | | VCC = 1.6 V or above | | 250 | - | | |
| | CLKOUT pin high pulse width*2 | VCC = 2.7 V or above | $t_{CH}$ | 15 | - | ns | |
| | | VCC = 1.8 V or above | | 30 | - | | |
| | | VCC = 1.6 V or above | | 150 | - | | |
| | CLKOUT pin low pulse width*2 | VCC = 2.7 V or above | $t_{CL}$ | 15 | - | ns | |
| | | VCC = 1.8 V or above | | 30 | - | | |
| | | VCC = 1.6 V or above | | 150 | - | | |
| | CLKOUT pin output rise time | VCC = 2.7 V or above | $t_{Cr}$ | - | 12 | ns | |
| | | VCC = 1.8 V or above | | - | 25 | | |
| | | VCC = 1.6 V or above | | - | 50 | | |
| | CLKOUT pin output fall time | VCC = 2.7 V or above | $t_{Cf}$ | - | 12 | ns | |
| | | VCC = 1.8 V or above | | - | 25 | | |
| | | VCC = 1.6 V or above | | - | 50 | | |

Note 1. When the EXTAL external clock input or an oscillator is used with division by 1 (the CKOCR.CKOSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

Note 2. When the MOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 001b), set the clock output division ratio selection to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).

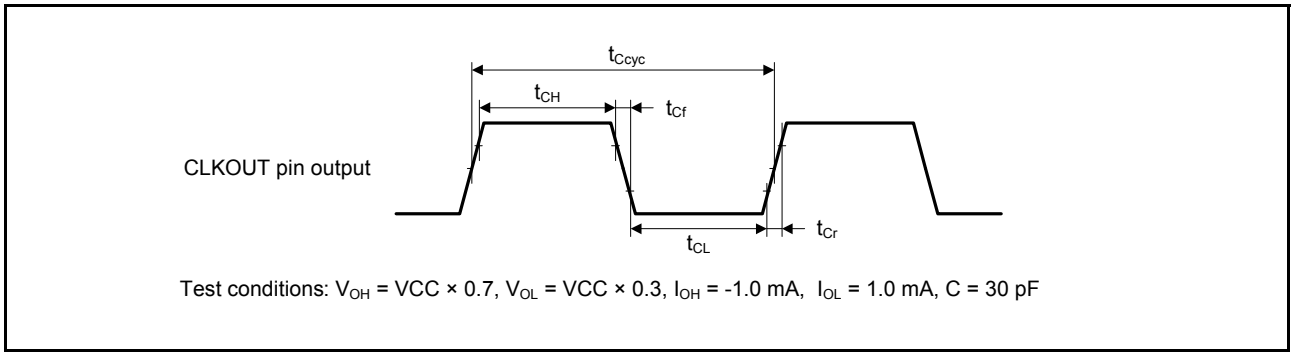



**Figure 2.57 CLKOUT output timing**

**Table 2.42 A/D conversion characteristics (3) in high-speed A/D conversion mode (2 of 2)**
Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| DNL differential nonlinearity error | | - | ±1.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±1.0 | ±3.0 | LSB | - |
| 14-bit mode | | | | | | |
| Resolution | | - | - | 14 | Bit | - |
| Conversion time*1 (Operation at PCLKD = 32 MHz) | Permissible signal source impedance Max. = 1.3 kΩ | 1.59 | - | - | µs | High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh |
| | | 2.44 | - | - | µs | Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±2.0 | ±18 | LSB | High-precision channel |
| | | | | ±24.0 | LSB | Other than above |
| Full-scale error | | - | ±3.0 | ±18 | LSB | High-precision channel |
| | | | | ±24.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |
| Absolute accuracy | | - | ±5.0 | ±20 | LSB | High-precision channel |
| | | | | ±32.0 | LSB | Other than above |
| DNL differential nonlinearity error | | - | ±4.0 | - | LSB | - |
| INL integral nonlinearity error | | - | ±4.0 | ±12.0 | LSB | - |

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4, I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.

**Table 2.43 A/D conversion characteristics (4) in low-power A/D conversion mode (1 of 2)**
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

| Parameter | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Frequency | | 1 | - | 24 | MHz | - |
| Analog input capacitance*2 | Cs | - | - | 8*3 | pF | High-precision channel |
| | | - | - | 9*3 | pF | Normal-precision channel |
| Analog input resistance | Rs | - | - | 2.5*3 | kΩ | High-precision channel |
| | | - | - | 6.7*3 | kΩ | Normal-precision channel |
| Analog input voltage range | Ain | 0 | - | VREFH0 | V | - |
| 12-bit mode | | | | | | |
| Resolution | | - | - | 12 | Bit | - |
| Conversion time*1 (Operation at PCLKD = 24 MHz) | Permissible signal source impedance Max. = 1.1 kΩ | 2.25 | - | - | µs | High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh |
| | | 3.38 | - | - | µs | Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h |
| Offset error | | - | ±0.5 | ±4.5 | LSB | High-precision channel |
| | | | | ±6.0 | LSB | Other than above |
| Full-scale error | | - | ±0.75 | ±4.5 | LSB | High-precision channel |
| | | | | ±6.0 | LSB | Other than above |
| Quantization error | | - | ±0.5 | - | LSB | - |

## 2.11 Comparator Characteristics

**Table 2.55 ACMPLP characteristics**
Conditions: VCC = AVCC0 = 1.8 to 5.5 V, VSS = AVSS0 = 0 V

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Reference voltage range | | $V_{REF}$ | 0 | - | VCC –1.4 | V | - |
| Input voltage range | | $V_I$ | 0 | - | VCC | V | - |
| Internal reference voltage | | - | 1.36 | 1.44 | 1.50 | V | - |
| Output delay | High-speed mode | $T_d$ | - | - | 1.2 | µs | VCC = 3.0<br>Slew rate of input signal > 50 mV/µs |
| | Low-speed mode | | - | - | 5 | µs | |
| | Window mode | | - | - | 2 | µs | |
| Offset voltage | High-speed mode | - | - | - | 50 | mV | - |
| | Low-speed mode | - | - | - | 40 | mV | - |
| | Window mode | - | - | - | 60 | mV | - |
| Internal reference voltage for window mode | | $V_{RFH}$ | - | 0.76 × VCC | - | V | - |
| | | $V_{RFL}$ | - | 0.24 × VCC | - | V | - |
| Operation stabilization wait time | | $T_{cmp}$ | 100 | - | - | µs | - |

**Table 2.58 Code flash characteristics (3)**

Middle-speed operating mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V, Ta = -40 to +85°C

| Parameter | | Symbol | ICLK = 1 MHz | | | ICLK = 8 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Programming time | 4-byte | $t_{P4}$ | - | 157 | 1411 | - | 101 | 966 | µs |
| Erasure time | 1-KB | $t_{E1K}$ | - | 9.10 | 289 | - | 6.10 | 228 | ms |
| Blank check time | 2-byte | $t_{BC4}$ | - | - | 87.7 | - | - | 52.5 | µs |
| | 1-KB | $t_{BC1K}$ | - | - | 1930 | - | - | 414 | µs |
| Erase suspended time | | $t_{SED}$ | - | - | 32.7 | - | - | 21.6 | µs |
| Startup area switching setting time | | $t_{SAS}$ | - | 22.8 | 592 | - | 14.2 | 465 | ms |
| Access window time | | $t_{AWS}$ | - | 22.8 | 592 | - | 14.2 | 465 | ms |
| OCD/serial programmer ID setting time | | $t_{OSIS}$ | - | 22.8 | 592 | - | 14.2 | 465 | ms |
| Flash memory mode transition wait time 1 | | $t_{DIS}$ | 2 | - | - | 2 | - | - | µs |
| Flash memory mode transition wait time 2 | | $t_{MS}$ | 720 | - | - | 720 | - | - | ns |

Note 1. Does not include the time until each operation of the flash memory is started after instructions are executed by the software.

Note 2. The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 3. The frequency accuracy of ICLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

## 2.12.2 Data Flash Memory Characteristics

**Table 2.59 Data flash characteristics (1)**

| Parameter | | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| Reprogramming/erasure cycle*1 | | $N_{DPEC}$ | 100000 | 1000000 | - | Times | - |
| Data hold time | After 10000 times of $N_{DPEC}$ | $t_{DDRP}$ | 20*2, *3 | - | - | Year | Ta = +85°C |
| | After 100000 times of $N_{DPEC}$ | | 5*2, *3 | - | - | Year | |
| | After 1000000 times of $N_{DPEC}$ | | - | 1*2, *3 | - | Year | Ta = +25°C |

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,000 times for different addresses in 1-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as 1. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited.)

Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. These results are obtained from reliability testing.

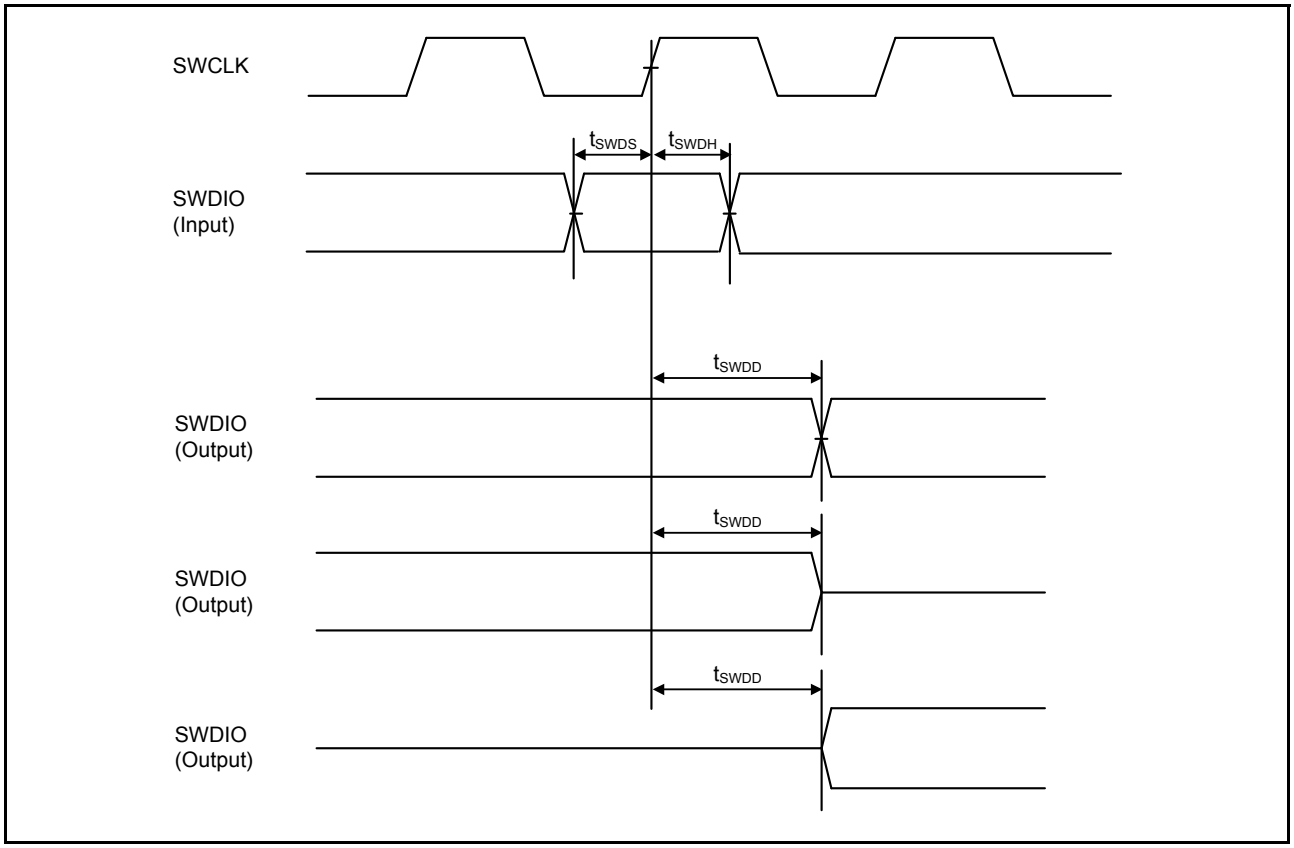
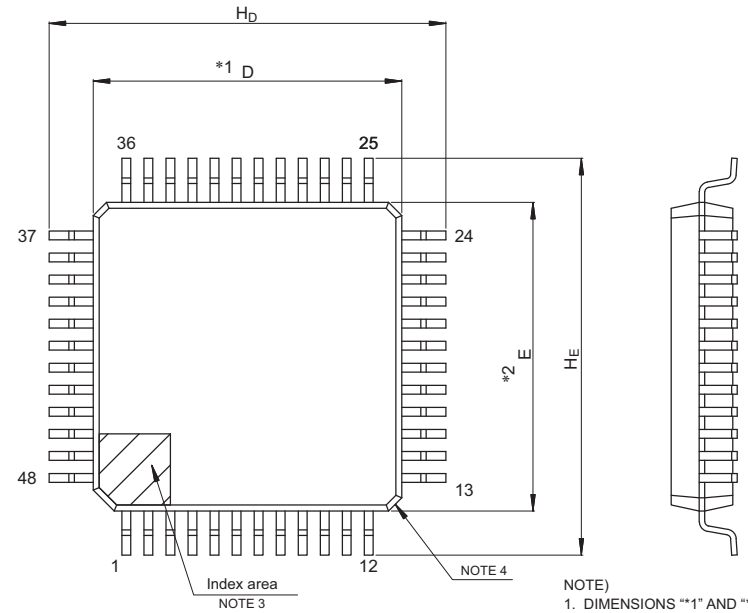


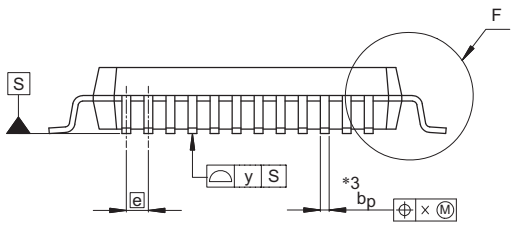

**Figure 2.72 SWD input output timing**

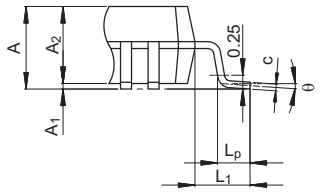
| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP48-7x7-0.50 | PLQP0048KB-B | — | 0.2 |

Unit: mm




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.




Detail F

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.9 | 7.0 | 7.1 |
| E | 6.9 | 7.0 | 7.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 8.8 | 9.0 | 9.2 |
| $H_E$ | 8.8 | 9.0 | 9.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.17 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |



**Figure 1.2 LQFP 48-pin**