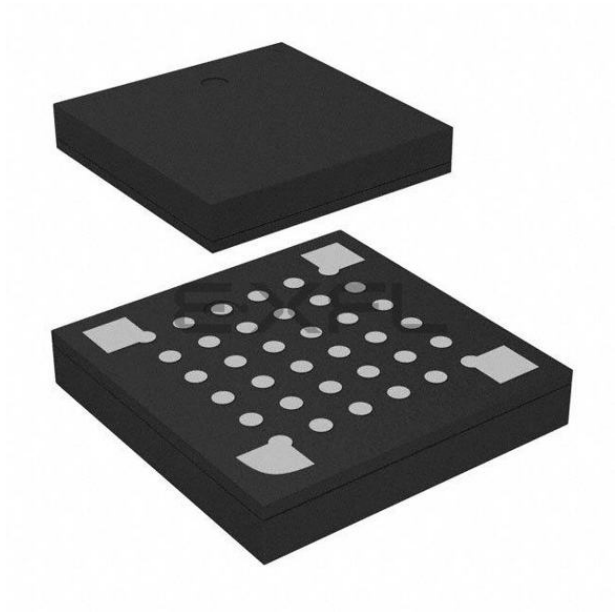
Renesas Electronics America Inc - R7FS124772A01CLM#AC0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 11x14b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-WFLGA
Supplier Device Package	36-WFLGA (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs124772a01clm-ac0

Ultra-low power 32-MHz Arm® Cortex®-M0+ microcontroller, 128-KB code flash memory, 16-KB SRAM, Capacitive Touch Sensing Unit, 14-bit A/D Converter, 12-bit D/A Converter, security and safety features.

Features

■ Arm Cortex-M0+ Core
- Armv6-M architecture
- Maximum operating frequency: 32 MHz
- Debug and Trace: DWT, BPU, CoreSight™ MTB-M0+
- CoreSight Debug Port: SW-DP

■ Memory
- 128-KB code flash memory
- 4-KB data flash memory (100,000 erase/write cycles)
- Up to 16-KB SRAM
- 128-bit unique ID

■ Connectivity
- USB 2.0 Full-Speed Module (USBFS)
  - On-chip transceiver with voltage regulator
  - Compliant with USB Battery Charging Specification 1.2
- Serial Communications Interface (SCI) × 3
  - UART
  - Simple IIC
  - Simple SPI
- Serial Peripheral Interface (SPI) × 2
- I^2C bus interface (IIC) × 2
- CAN module (CAN)

■ Analog
- 14-Bit A/D Converter (ADC14)
- 12-Bit D/A Converter (DAC12)
- Low-Power Analog Comparator (ACMPLP) × 2
- Temperature Sensor (TSN)

■ Timers
- General PWM Timer 32-Bit (GPT32)
- General PWM Timer 16-Bit (GPT16) × 6
- Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

■ Safety
- SRAM Parity Error Check
- Flash Area Protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) Calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO Readback Level Detection
- Register Write Protection
- Main Oscillator Stop Detection

■ System and Power Management
- Low-power modes
- Realtime Clock (RTC)
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection with voltage settings

■ Security and Encryption
- AES128/256
- True Random Number Generator (TRNG)

■ Human Machine Interface (HMI)
- Capacitive Touch Sensing Unit (CTSU)

■ Multiple Clock Sources
- Main clock oscillator (MOSC)
  (1 to 20 MHz when VCC = 2.4 to 5.5 V)
  (1 to 8 MHz when VCC = 1.8 to 5.5 V)
  (1 to 4 MHz when VCC = 1.6 to 5.5 V)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO)
  (24, 32, 48, 64 MHz when VCC = 2.4 to 5.5 V)
  (24, 32, 48 MHz when VCC = 1.8 to 5.5 V)
  (24, 32 MHz when VCC = 1.6 to 5.5 V)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Independent watchdog timer OCO (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

■ General Purpose I/O Ports
- Up to 51 input/output pins
  - Up to 3 CMOS input
  - Up to 48 CMOS input/output
    - Up to 6 input/output 5 V tolerant
    - Up to 16 pins high current (20 mA)

■ Operating Voltage
- VCC: 1.6 to 5.5 V

■ Operating Temperature and Packages
- Ta = –40°C to +85°C
  - 36-pin LGA (4 mm × 4 mm, 0.5 mm pitch)
- Ta = –40°C to +105°C
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
  - 64-pin QFN (8 mm × 8 mm, 0.4 mm pitch)
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)
  - 40-pin QFN (6 mm × 6 mm, 0.5 mm pitch)

1.5 Pin Functions

Table 1.14 Pin functions (1 of 3)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation mode transition at the time of release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin.
On-chip debug	SWDIO	I/O	Serial Wire debug Data Input/Output pin.
	SWCLK	Input	Serial Wire Clock pin.
Interrupt	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Maskable interrupt request pins.
GPT	GTETRGA, GTETRGB	Input	External trigger input pin.
	GTIOC0A to GTIOC6A, GTIOC0B to GTIOC6B	I/O	Input capture, Output Compare, or PWM output pin.
	GTIU	Input	Hall sensor input pin U.
	GTIV	Input	Hall sensor input pin V.
	GTIW	Input	Hall sensor input pin W.
	GTOUUP	Output	Three-phase PWM output for BLDC motor control (positive U phase).
	GTOULO	Output	Three-phase PWM output for BLDC motor control (negative U phase).
	GTOVUP	Output	Three-phase PWM output for BLDC motor control (positive V phase).
	GTOVLO	Output	Three-phase PWM output for BLDC motor control (negative V phase).
	GTOWUP	Output	Three-phase PWM output for BLDC motor control (positive W phase).
	GTOWLO	Output	Three-phase PWM output for BLDC motor control (negative W phase).
AGT	AGTEE0, AGTEE1	Input	External event input enable.
	AGTIO0, AGTIO1	I/O	External event input and pulse output.
	AGTO0, AGTO1	Output	Pulse output.
	AGTOA0, AGTOA1	Output	Output compare match A output.
	AGTOB0, AGTOB1	Output	Output compare match B output.
RTC	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock.

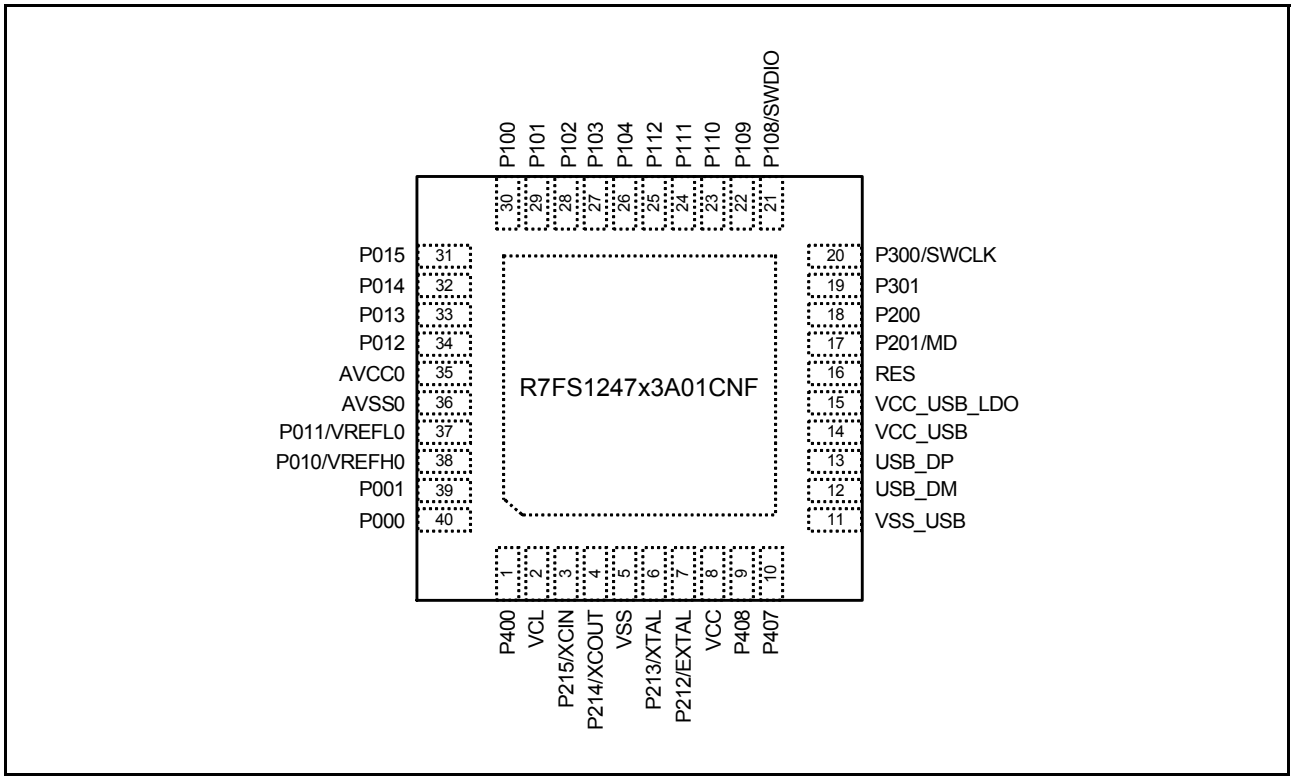


Figure 1.7 Pin assignment for QFN 40-pin (top view)

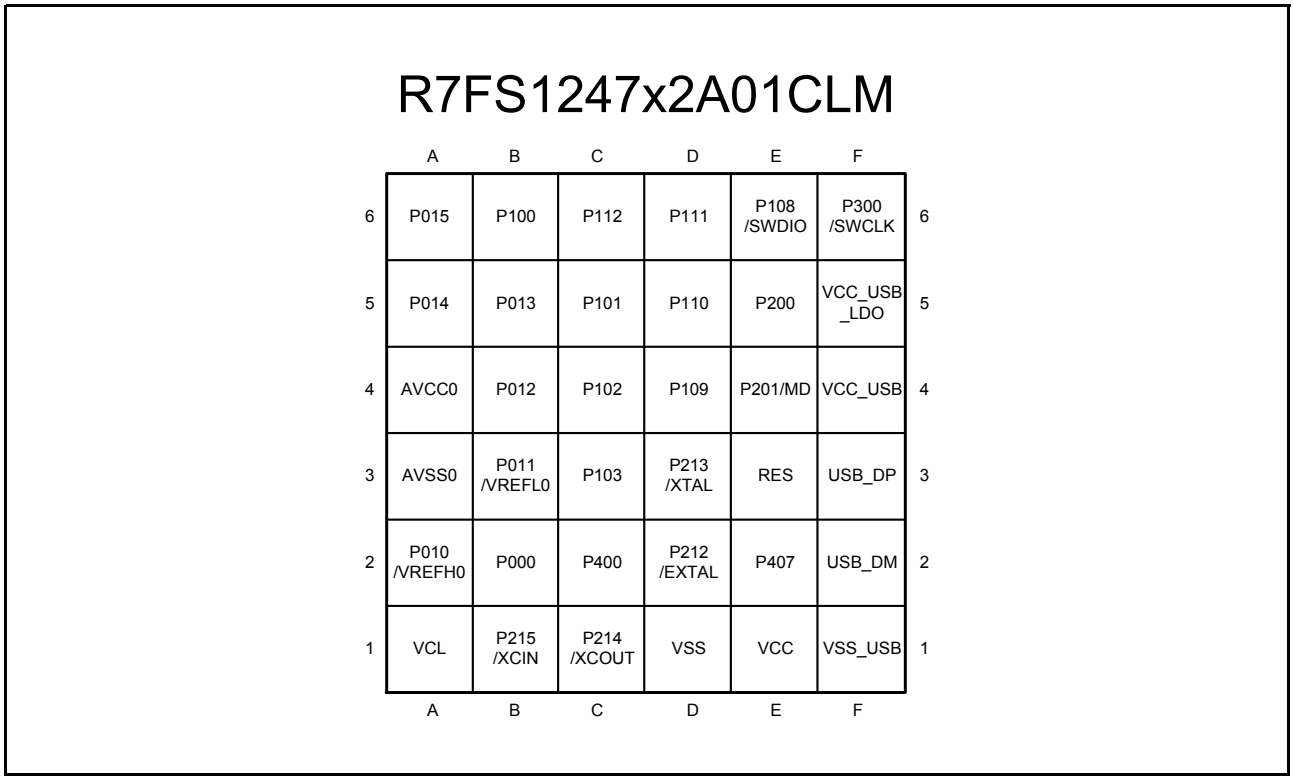


Figure 1.8 Pin assignment for LGA 36-pin (top view, pad side down)

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	–0.5 to +6.5	V
Input voltage	5V-tolerant ports*1	V_{in}	–0.3 to +6.5	V
	P000 to P004 P010 to P015	V_{in}	–0.3 to AVCC0 + 0.3	V
	Others	V_{in}	–0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	–0.3 to +6.5	V
Analog power supply voltage		AVCC0	–0.5 to +6.5	V
USB power supply voltage		VCC_USB	–0.5 to +6.5	V
		VCC_USB_LDO	–0.5 to +6.5	V
Analog input voltage	When AN000 to AN010 are used	V_{AN}	–0.3 to AVCC0 + 0.3	V
	When AN016 to AN022 are used		–0.3 to VCC + 0.3	V
Operating temperature*2 *3		T_{opr}	–40 to +85 –40 to +105	°C
Storage temperature		T_{stg}	–55 to +125	°C

Note: See the Total Operating Time (TOT) Utility located at http://www.renesas.com. This utility is provided for educational and evaluation purposes only and is subject to the accompanying disclaimer.

Note 1. Ports P205, P206, P400, P401, and P407 are 5V-tolerant.
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.

Note 2. See section 2.2.1, Tj/Ta Definition.

Note 3. The upper limit of the operating temperature is 85°C or 105°C, depending on the product. For details, see section 1, Part Numbering

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, and between the VREFH0 and VREFL0 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces. Also, connect capacitors as stabilization capacitance.
Connect the VCL pin to a VSS pin by a 4.7-µF capacitor. The capacitor must be placed close to the pin.

Table 2.9 I/O V_{OH}, V_{OL} (3)
Conditions: VCC = AVCC0 = 1.6 to 2.7 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P004 P010 to P015	Low drive	V_{OH}	AVCC0 – 0.3	-	-		I_{OH} = –0.5 mA
			V_{OL}	-	-	0.3		I_{OL} = 0.5 mA
		Middle drive	V_{OH}	AVCC0 – 0.3	-	-		I_{OH} = –1.0 mA
			V_{OL}	-	-	0.3		I_{OL} = 1.0 mA
	Other output pins*1	Low drive	V_{OH}	VCC – 0.3	-	-	V	I_{OH} = –0.5 mA
			V_{OL}	-	-	0.3		I_{OL} = 0.5 mA
		Middle drive*2	V_{OH}	VCC – 0.3	-	-		I_{OH} = –1.0 mA
			V_{OL}	-	-	0.3		I_{OL} = 1.0 mA

Note 1. Except for Ports P200, P214, P215, which are input ports.
Note 2. Except for P212, P213.

Table 2.10 I/O other characteristics
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES, Ports P200, P214, P215	$\lvert I_{in} \rvert$	-	-	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5V-tolerant ports	$\lvert I_{TSI} \rvert$	-	-	1.0	µA	V_{in} = 0 V V_{in} = 5.8 V
	Other ports		-	-	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up resistor	All ports (except for P200, P214, P215)	R_U	10	20	50	kΩ	V_{in} = 0 V
Input capacitance	USB_DP, USB_DM, P200	C_{in}	-	-	30	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	Other input pins		-	-	15		

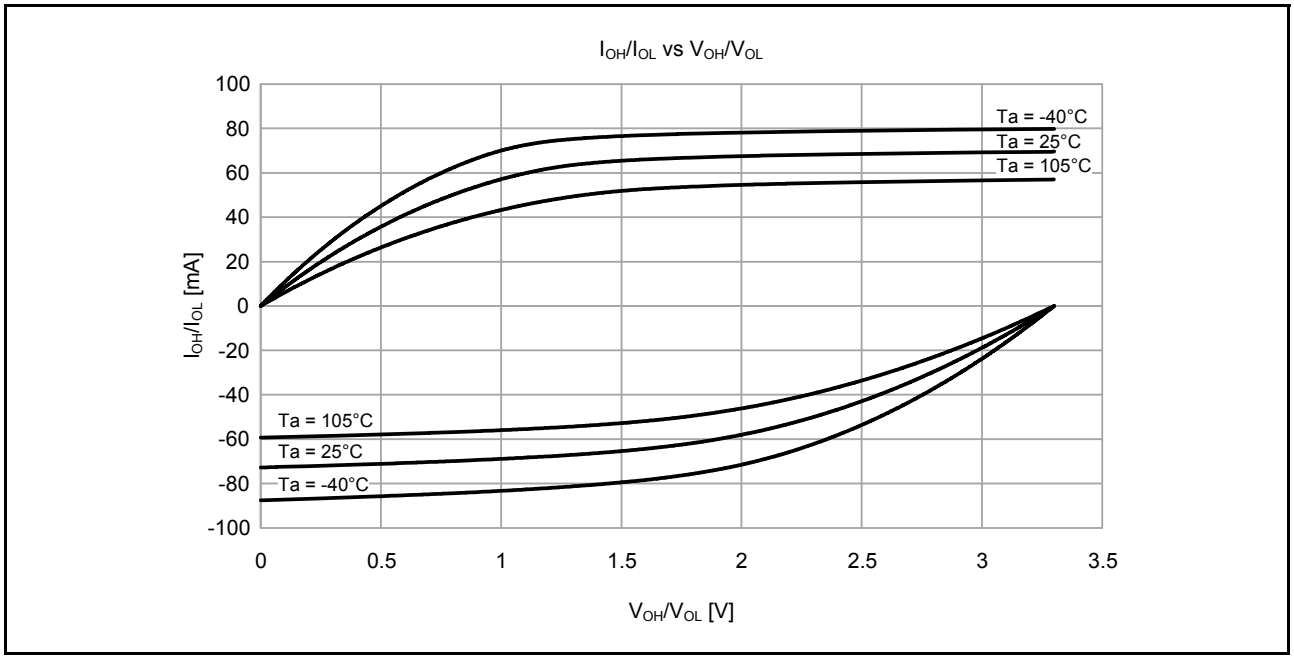


Figure 2.14 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 3.3 V when middle drive output is selected (reference data)**

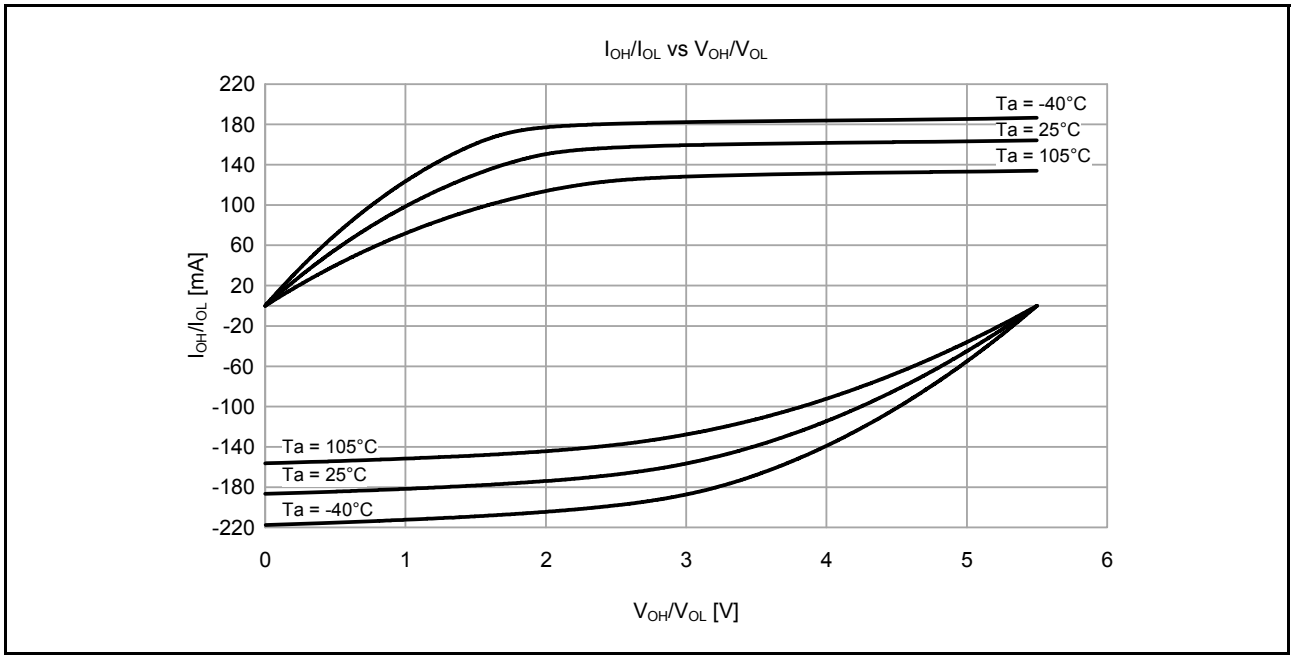


Figure 2.15 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 5.5 V when middle drive output is selected (reference data)**

2.2.9 Operating and Standby Current

Table 2.11 Operating and standby current (1) (1 of 2)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*9	Max	Unit	Test Conditions
Supply current*1	High-speed mode*2	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 32 MHz	I_{CC}	3.6	-	mA	*7
				ICLK = 16 MHz		2.4	-		
				ICLK = 8 MHz		1.7	-		
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 32 MHz		5.6	-		
				ICLK = 16 MHz		3.5	-		
				ICLK = 8 MHz		2.4	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 32 MHz		9.5	-		*8
				ICLK = 16 MHz		5.4	-		
				ICLK = 8 MHz		3.3	-		
			All peripheral clock enabled, code executing from flash*5	ICLK = 32 MHz		-	21.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 32 MHz		1.5	-		*7
				ICLK = 16 MHz		1.1	-		
				ICLK = 8 MHz		0.9	-		
			All peripheral clock enabled*5	ICLK = 32 MHz		7.2	-		*8
				ICLK = 16 MHz		4.0	-		
				ICLK = 8 MHz		2.4	-		
		Increase during BGO operation*6				2.5	-		-
	Middle-speed mode*2	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 12 MHz	I_{CC}	1.7	-	mA	*7
				ICLK = 8 MHz		1.5	-		
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 12 MHz		2.7	-		
				ICLK = 8 MHz		1.9	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 12 MHz		3.9	-		*8
				ICLK = 8 MHz		3.0	-		
			All peripheral clock enabled, code executing from flash*5	ICLK = 12 MHz		-	8.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 12 MHz		0.8	-		*7
				ICLK = 8 MHz		0.8	-		
			All peripheral clock enabled*5	ICLK = 12 MHz		2.9	-		*8
				ICLK = 8 MHz		2.2	-		
		Increase during BGO operation*6				2.5	-		-
	Low-speed mode*3	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 1 MHz	I_{CC}	0.2	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 1 MHz		0.3	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 1 MHz		0.4	-		*8
			All peripheral clock enabled, code executing from flash*5	ICLK = 1 MHz		-	2.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 1 MHz		0.2	-		*7
			All peripheral clock enabled*5	ICLK = 1 MHz		0.3	-		*8

Table 2.21 Clock timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock oscillation stabilization time*2	t_{SUBOSC}	-	0.5	-	s	Figure 2.28

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.
Note 2. After changing the setting of the SOSCCR.SOSTP bit to start sub-clock oscillator operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization wait time elapsed. Use the oscillator wait time value recommended by the oscillator manufacturer.
Note 3. The 48-MHz HOCO can be used within a VCC range of 1.8 V to 5.5 V.
Note 4. The 64-MHz HOCO can be used within a VCC range of 2.4 V to 5.5 V.
Note 5. This is a characteristic when the HOCOCR.HCSTP bit is cleared to 0 (oscillation) in the MOCO stop state. When the HOCOCR.HCSTP bit is cleared to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1 µs.
Note 6. Check OSCSF.HOCOSF to confirm whether stabilization time has elapsed.

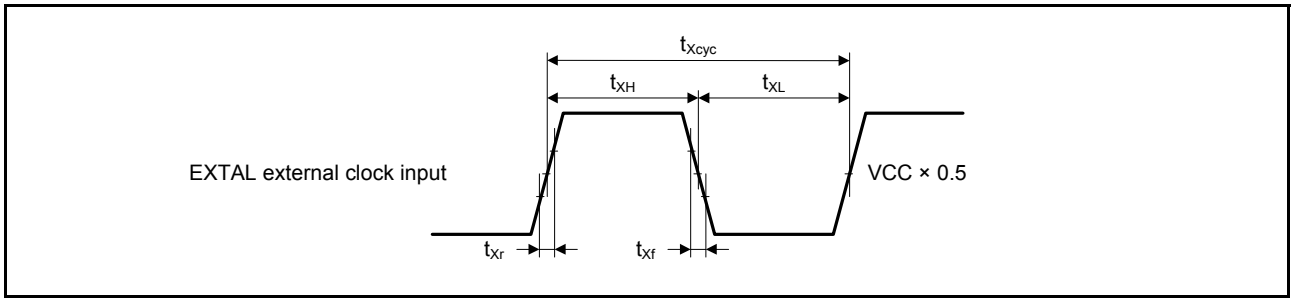


Figure 2.25 EXTAL external clock input timing

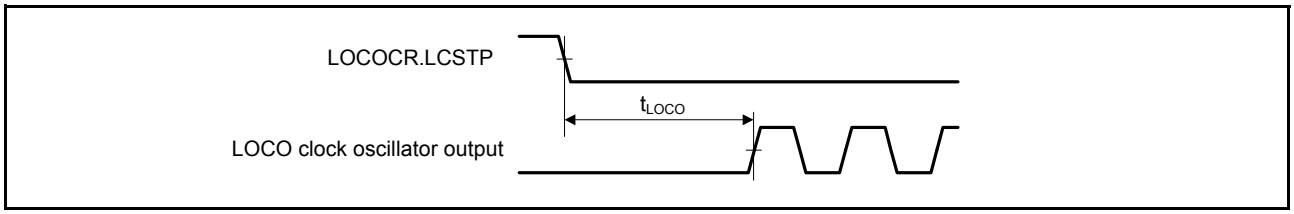


Figure 2.26 LOCO clock oscillation start timing

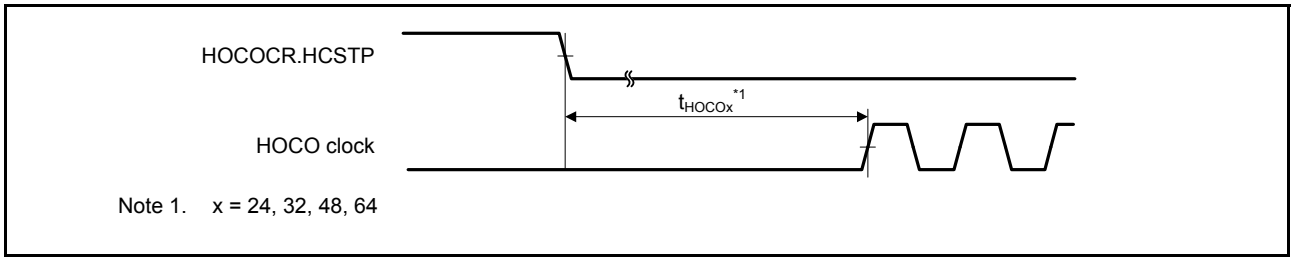


Figure 2.27 HOCO clock oscillation start timing (started by setting the HOCOCR.HCSTP bit)

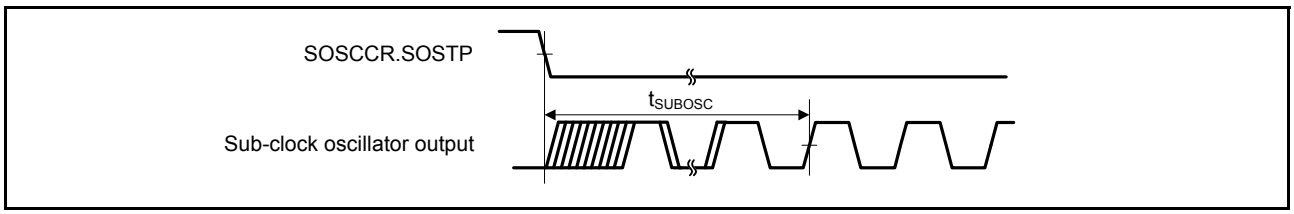


Figure 2.28 Sub-clock oscillation start timing

Table 2.33 SCI timing (2)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	Test conditions
Simple SPI	SCK clock cycle output (master)			t_{SPcyc}	4	65536	t_{Pcyc}	Figure 2.43
	SCK clock cycle input (slave)				6	65536		
	SCK clock high pulse width			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		1.8V or above	t_{SPCKr}, t_{SPCKf}	-	20	ns	
			1.6V or above		-	30		
	Data input setup time	Master	2.7V or above	t_{SU}	45	-	ns	Figure 2.44 to Figure 2.47
			2.4V or above		55	-		
			1.8V or above		80	-		
			1.6V or above		110	-		
		Slave	2.7V or above		40	-		
			1.6V or above		45	-		
	Data input hold time	Master		t_H	33.3	-	ns	
		Slave			40	-		
	SS input setup time			t_{LEAD}	1	-	t_{SPcyc}	
	SS input hold time			t_{LAG}	1	-	t_{SPcyc}	
	Data output delay	Master	1.8V or above	t_{OD}	-	40	ns	
			1.6V or above		-	50		
		Slave	2.4V or above		-	65		
			1.8V or above		-	100		
			1.6V or above		-	125		
	Data output hold time	Master	2.7V or above	t_{OH}	–10	-	ns	
			2.4V or above		–20	-		
			1.8V or above		–30	-		
			1.6V or above		–40	-		
		Slave			–10	-		
	Data rise and fall time	Master	1.8V or above	t_{Dr}, t_{Df}	-	20	ns	
			1.6V or above		-	30		
		Slave	1.8V or above		-	20		
			1.6V or above		-	30		
Simple SPI	Slave access time			t_{SA}	-	6	t_{Pcyc}	Figure 2.47
	Slave output release time			t_{REL}	-	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLKB cycle

Table 2.35 SPI timing (2 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	Data output delay	Master	2.7V or above	t_{OD}	-	14	ns	Figure 2.50 to Figure 2.55 C = 30pF
			2.4V or above		-	20		
			1.8V or above		-	25		
			1.6V or above		-	30		
		Slave	2.7V or above		-	50		
			2.4V or above		-	60		
			1.8V or above		-	85		
			1.6V or above		-	110		
	Data output hold time	Master		t_{OH}	0	-	ns	
		Slave			0	-		
	Successive transmission delay	Master		t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave			6 × t_{Pcyc}	-		
	MOSI and MISO rise and fall time	Output	2.7V or above	t_{Dr}, t_{Df}	-	10	ns	
			2.4V or above		-	15		
			1.8V or above		-	20		
			1.6V or above		-	30		
		Input			-	1	µs	
	SSL rise and fall time	Output	2.7V or above	t_{SSLr}, t_{SSLf}	-	10	ns	
			2.4V or above		-	15		
			1.8V or above		-	20		
			1.6V or above		-	30		
		Input			-	1	µs	
	Slave access time		2.4V or above	t_{SA}	-	2 × t_{Pcyc} +100	ns	Figure 2.54 and Figure 2.55 C = 30pF
			1.8V or above		-	2 × t_{Pcyc} +140		
			1.6V or above		-	2 × t_{Pcyc} +180		
	Slave output release time		2.4V or above	t_{REL}	-	2 × t_{Pcyc} +100	ns	
			1.8V or above		-	2 × t_{Pcyc} +140		
			1.6V or above		-	2 × t_{Pcyc} +180		

Note 1. t_{Pcyc}: PCLKB cycle.

Note 2. N is set as an integer from 1 to 8 by the SPCKD register.

Note 3. N is set as an integer from 1 to 8 by the SSLND register.

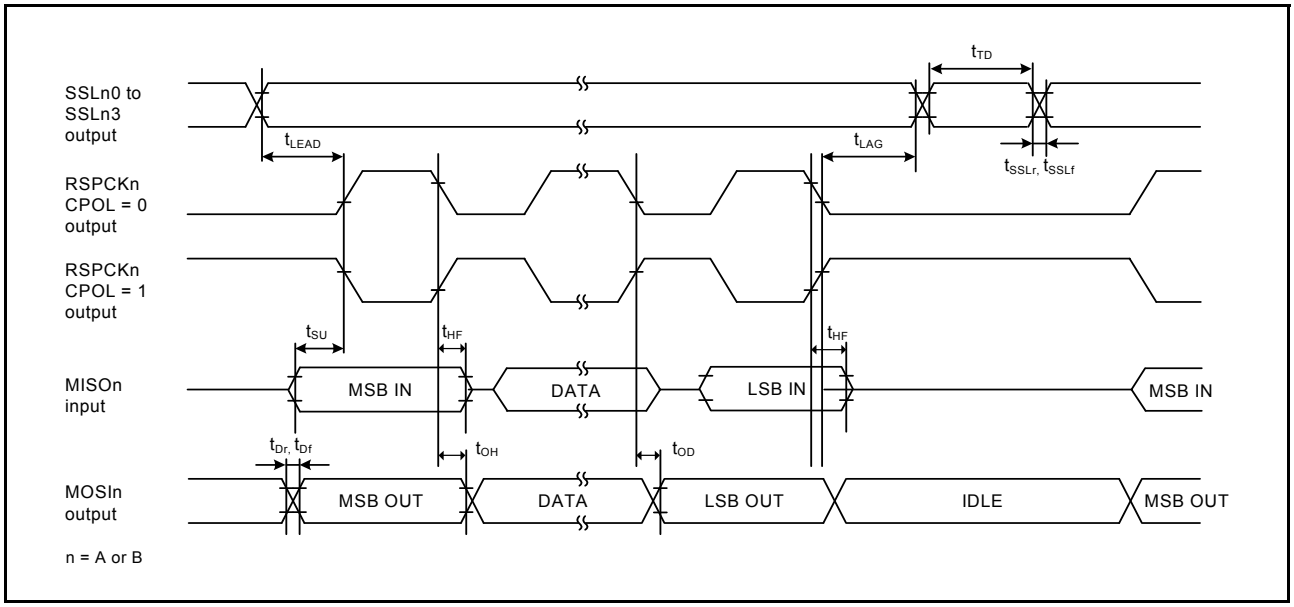


Figure 2.51 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to 1/2)

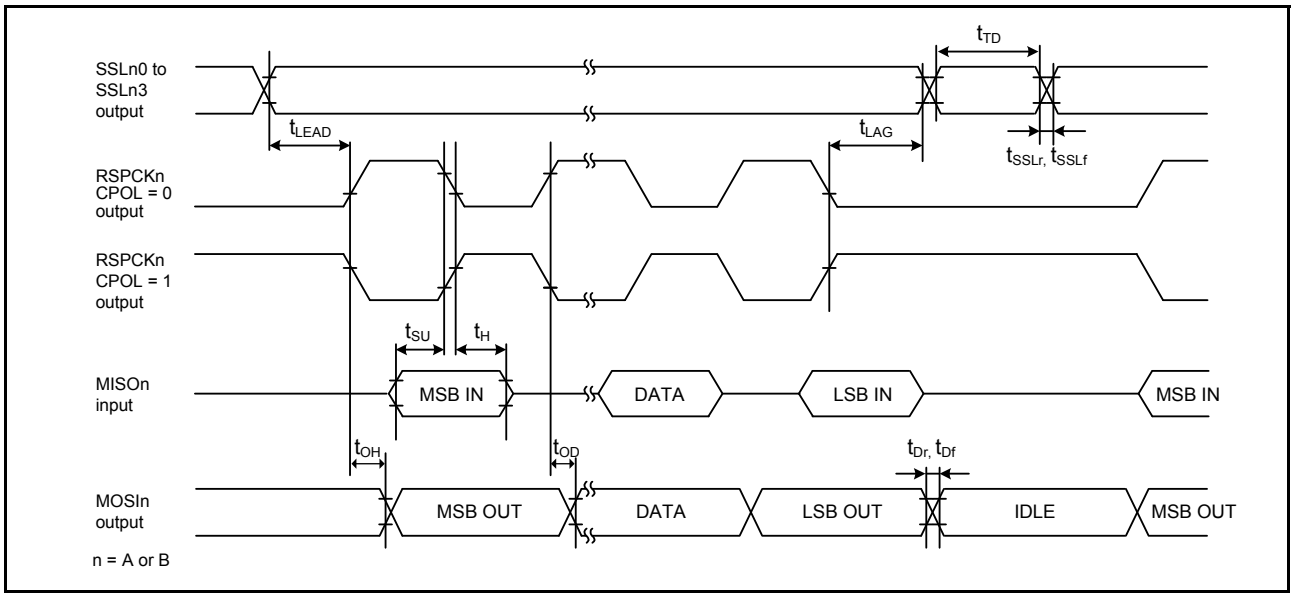


Figure 2.52 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to any value other than 1/2)

2.3.10 IIC Timing

Table 2.36 IIC timing
Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	Test conditions
IIC (standard mode, SMBus)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 2.56
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	1000	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	1000	-	ns	
	STOP condition input setup time	t_{STOS}	1000	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	
IIC*2 (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 2.56
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	300	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1(5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note 2. Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Table 2.43 A/D conversion characteristics (4) in low-power A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	2.50	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.63	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4, I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.

Table 2.44 A/D conversion characteristics (5) in low-power A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	16	MHz	-
Analog input capacitance*2	Cs	-	-	8*3	pF	High-precision channel
		-	-	9*3	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5*3	kΩ	High-precision channel
		-	-	6.7*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	3.38	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		5.06	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above

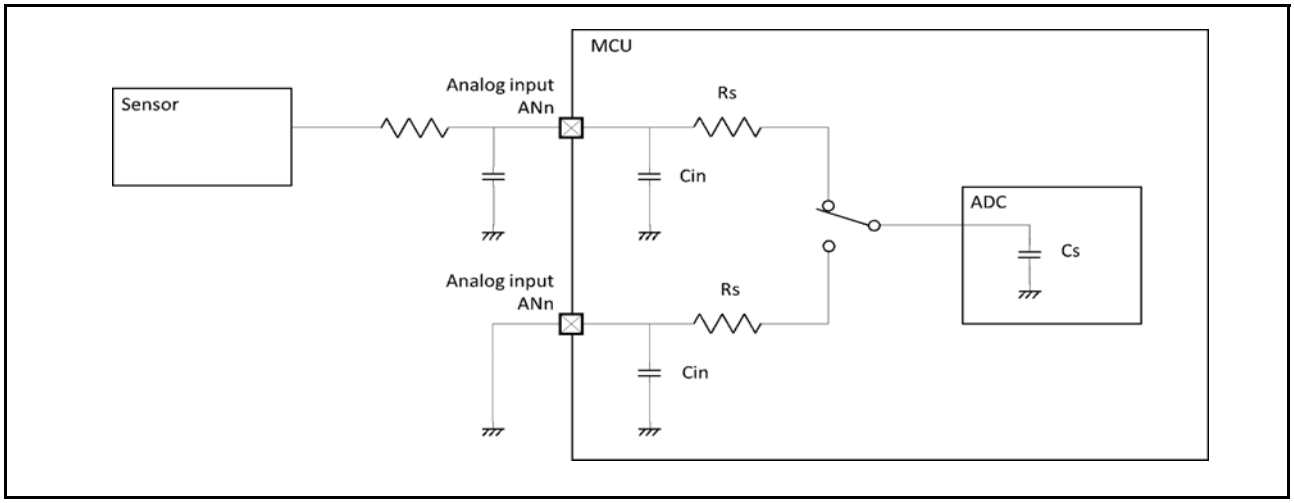


Figure 2.62 Equivalent circuit for analog input

Table 2.47 14-bit A/D converter channel classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN010	AVCC0 = 1.6 to 5.5 V	Pins AN000 to AN010 cannot be used as general I/O, TS transmission, when the A/D converter is in use.
Normal-precision channel	AN016 to AN022		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 5.5 V	-
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 5.5 V	-

Table 2.48 A/D internal reference voltage characteristics

Conditions: VCC = AVCC0 = VREFH0 = 2.0 to 5.5 V*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.36	1.43	1.50	V	-
Frequency	1	-	2	MHz	-
Sampling time	5.0	-	-	µs	-

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 < 2.0 V.

Note 2. The 14-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 14-bit A/D converter.

Table 2.53 Power-on reset circuit and voltage detection circuit characteristics (2) (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Power-on reset enable time	$t_{W\ (POR)}$	1	-	-	ms	Figure 2.67, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)	$T_{d\ (E-A)}$	-	-	300	µs	Figure 2.69, Figure 2.70
Hysteresis width (POR)	V_{PORH}	-	110	-	mV	-
Hysteresis width (LVD0, LVD1, and LVD2)	V_{LVH}	-	60	-	mV	LVD0 selected
		-	100	-		V_{det1_0} to V_{det1_2} selected.
		-	60	-		V_{det1_3} to V_{det1_9} selected.
		-	50	-		V_{det1_A} to V_{det1_B} selected.
		-	40	-		V_{det1_C} to V_{det1_F} selected.
		-	60	-		LVD2 selected

Note 1. When OFS1.LVDAS = 0
Note 2. When OFS1.LVDAS = 1
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

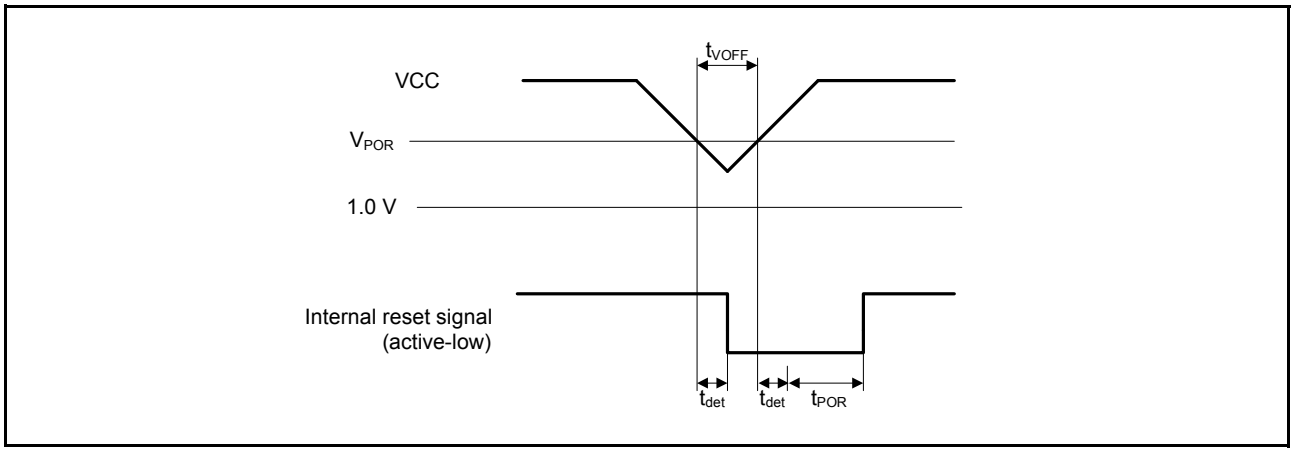
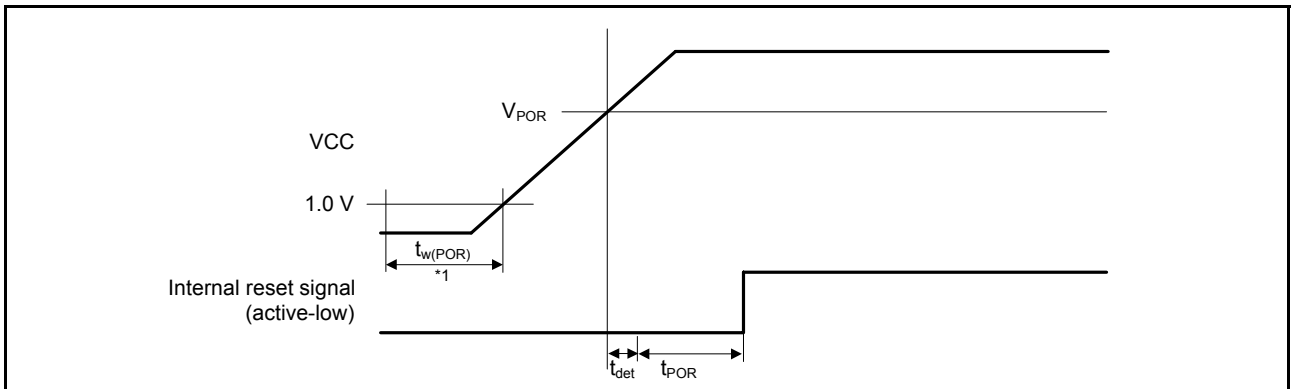


Figure 2.66 Voltage detection reset timing



Note: $t_{W(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{W(POR)}$ for 1.0 ms or more.

Figure 2.67 Power-on reset timing

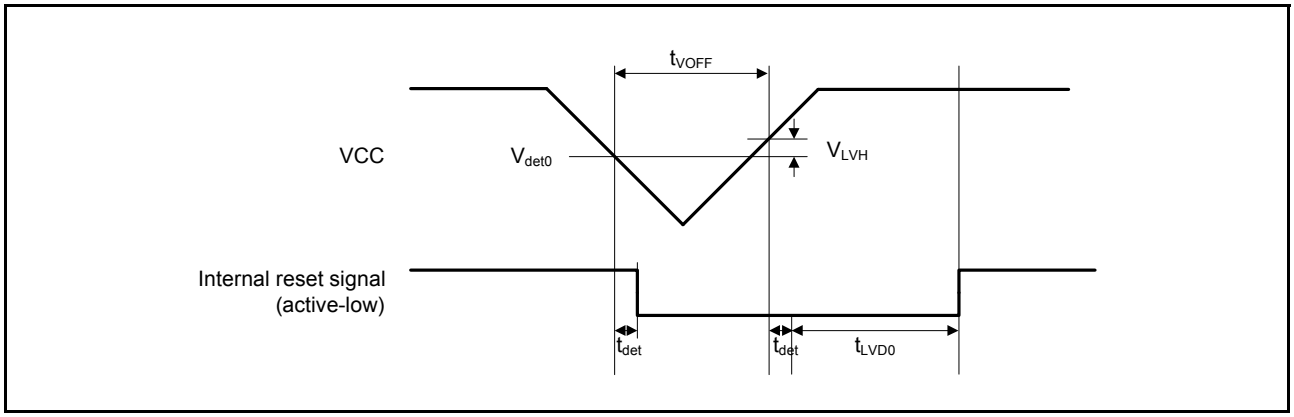


Figure 2.68 Voltage detection circuit timing (V_{det0})

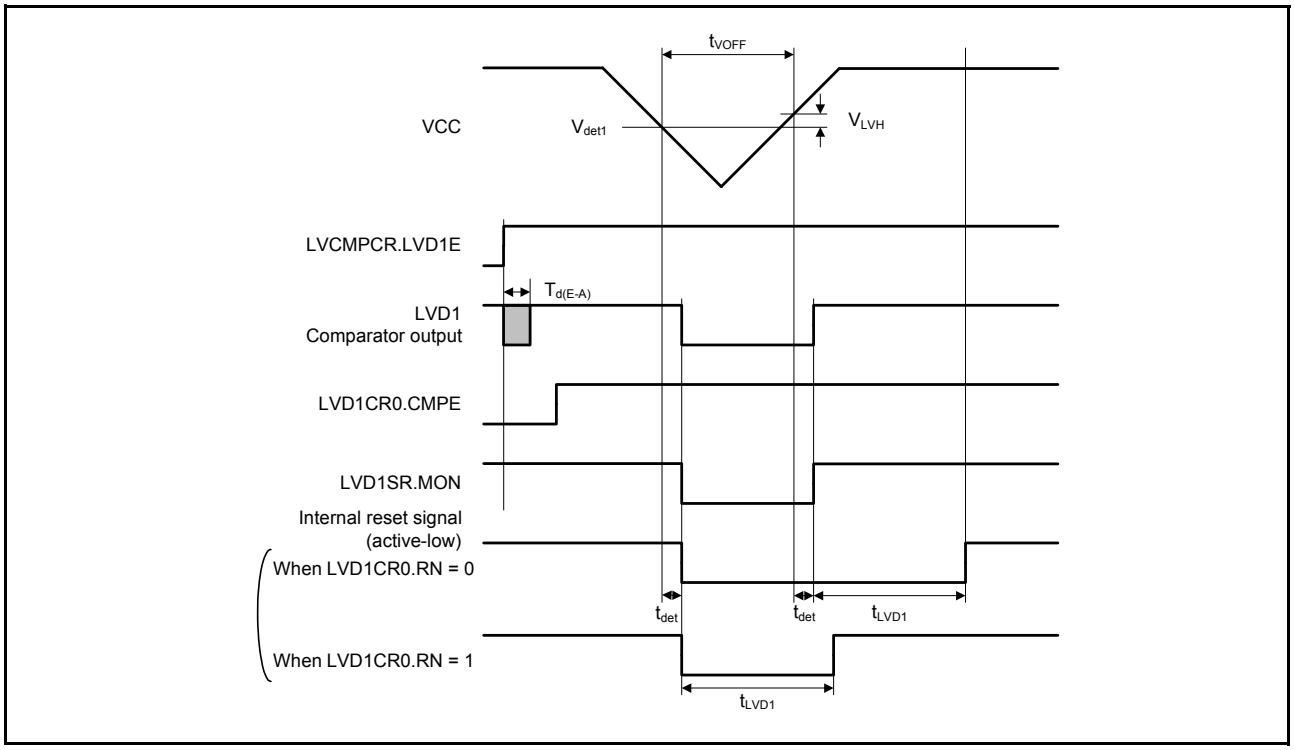


Figure 2.69 Voltage detection circuit timing (V_{det1})

2.11 Comparator Characteristics

Table 2.55 ACMPLP characteristics
Conditions: VCC = AVCC0 = 1.8 to 5.5 V, VSS = AVSS0 = 0 V

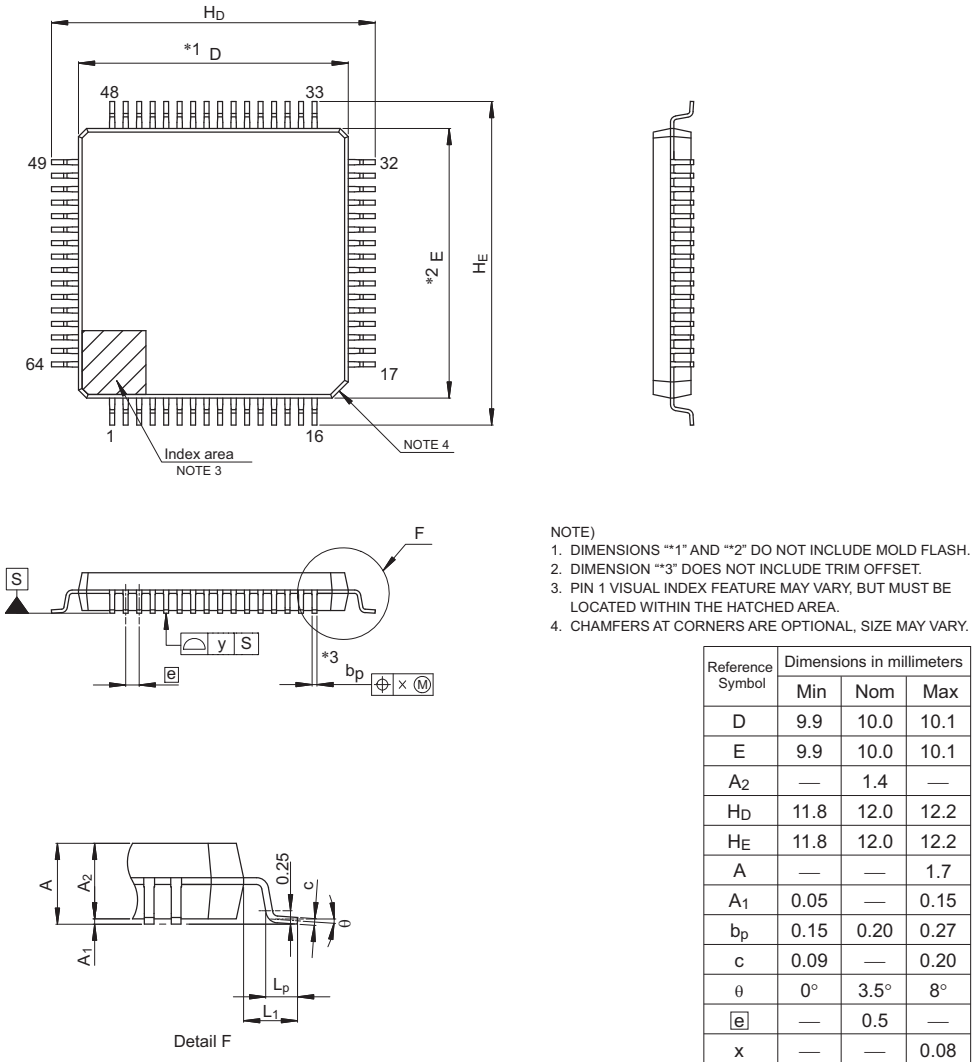
Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range		V_{REF}	0	-	VCC –1.4	V	-
Input voltage range		V_I	0	-	VCC	V	-
Internal reference voltage		-	1.36	1.44	1.50	V	-
Output delay	High-speed mode	T_d	-	-	1.2	µs	VCC = 3.0 Slew rate of input signal > 50 mV/µs
	Low-speed mode		-	-	5	µs	
	Window mode		-	-	2	µs	
Offset voltage	High-speed mode	-	-	-	50	mV	-
	Low-speed mode	-	-	-	40	mV	-
	Window mode	-	-	-	60	mV	-
Internal reference voltage for window mode		V_{RFH}	-	0.76 × VCC	-	V	-
		V_{RFL}	-	0.24 × VCC	-	V	-
Operation stabilization wait time		T_{cmp}	100	-	-	µs	-

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm



NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 1.1 LQFP 64-pin

Revision History	S124 Microcontroller Group Datasheet

Rev.	Date	Summary
1.00	May 19, 2016	1st release
1.01	Oct 3, 2016	2nd release
1.30	Feb 5, 2018	3rd release

General Precautions

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.