E. Kenesas Electronics America Inc - <u>R7FS124772A01CLM#AC1 Datasheet</u>



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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CANbus, I ² C, SCI, SPI, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 11x14b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-WFLGA
Supplier Device Package	36-WFLGA (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs124772a01clm-ac1

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Feature	Functional description
AES	See section 38, AES Engine in User's Manual
True Random Number Generator (TRNG)	See section 39, True Random Number Generator (TRNG) in User's Manual

1.2 Block Diagram

Figure 1.1 shows the block diagram of the MCU superset. Individual devices within the group may have a subset of the features.



Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows how to read the product part number, memory capacity, and package types. Table 1.12 shows a list of products.





Table 1.12 Product list

Product part number	Orderable part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FS124773A01CFM	R7FS124773A01CFM#AA1	PLQP0064KB-C	128 KB	4 KB	16 KB	–40 to +105°C
R7FS124773A01CNB	R7FS124773A01CNB#AC1	PWQN0064LA-A				–40 to +105°C
R7FS124773A01CFL	R7FS124773A01CFL#AA1	PLQP0048KB-B				–40 to +105°C
R7FS124773A01CNE	R7FS124773A01CNE#AC1	PWQN0048KB-A				-40 to +105°C
R7FS124773A01CNF	R7FS124773A01CNF#AC1	PWQN0040KC-A				–40 to +105°C
R7FS124772A01CLM	R7FS124772A01CLM#AC1	PWLG0036KA-A				–40 to +85°C
R7FS124763A01CFM	R7FS124763A01CFM#AA1	PLQP0064KB-C	64 KB			–40 to +105°C
R7FS124763A01CFL	R7FS124763A01CFL#AA1	PLQP0048KB-B				-40 to +105°C
R7FS124762A01CLM	R7FS124762A01CLM#AC1	PWLG0036KA-A				-40 to +85°C

Note: Earlier products with orderable part number suffix AA0 and AC0 have a restriction in AES functions. If AES functions are required for your application, refer to the products with orderable part number suffix AA1 or AC1. For details on the differences of AES functions between AA0/AC0 and AA1/AC1 products, see *Technical Update* (*TN-SY*-A024A/E*). Contact your Renesas sales representative for additional information.

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1.5 Pin Functions

Table 1.14	Pin function	ıs (1	of 3)
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Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1 - μ F capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through
	EXTAL	Input	the EXTAL pin.
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator
	XCOUT	Output	between XCOUT and XCIN.
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation mode transition at the time of release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin.
On-chip debug	SWDIO	I/O	Serial Wire debug Data Input/Output pin.
	SWCLK	Input	Serial Wire Clock pin.
Interrupt	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Maskable interrupt request pins.
GPT	GTETRGA, GTETRGB	Input	External trigger input pin.
	GTIOC0A to GTIOC6A, GTIOC0B to GTIOC6B	I/O	Input capture, Output Compare, or PWM output pin.
	GTIU	Input	Hall sensor input pin U.
	GTIV	Input	Hall sensor input pin V.
	GTIW	Input	Hall sensor input pin W.
	GTOUUP	Output	Three-phase PWM output for BLDC motor control (positive U phase).
	GTOULO	Output	Three-phase PWM output for BLDC motor control (negative U phase).
	GTOVUP	Output	Three-phase PWM output for BLDC motor control (positive V phase).
	GTOVLO	Output	Three-phase PWM output for BLDC motor control (negative V phase).
	GTOWUP	Output	Three-phase PWM output for BLDC motor control (positive W phase).
	GTOWLO	Output	Three-phase PWM output for BLDC motor control (negative W phase).
AGT	AGTEE0, AGTEE1	Input	External event input enable.
	AGTIO0, AGTIO1	I/O	External event input and pulse output.
	AGTO0, AGTO1	Output	Pulse output.
	AGTOA0, AGTOA1	Output	Output compare match A output.
	AGTOB0, AGTOB1	Output	Output compare match B output.
RTC	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock.



1. Overview

1.7 Pin Lists

		Pin numbe	r					Tin	ners		Co	ommunicat	ion Interfac	ces	Ana	logs	H	мі
LQFP64, QFN64	LQFP48	QFN48	QFN40	LGA36	Power, System, Clock, Debug, CAC	I/O ports	AGT	GPT_OPS, POEG	вт	RTC	USBFS,CAN	sci	S	IdS	ADC14	DAC12, ACMPLP	cTSU	Interrupt
1	1	1	1	C2	CACREF_ C	P400	AGTIO1_ D		GTIOC6A A			SCK0_B/ SCK1 B	SCL0_A				TS20	IRQ0
2	2	2	-	-		P401		GTETRG A_B	_ GTIOC6B _A		CTX0_B	CTS0_RT S0_B/ SS0_B/ TXD1_B/ MOSI1_B/ SDA1_B	SDA0_A				TS19	IRQ5
3	-	-	-	-		P402					CRX0_B	RXD1_B/ MISO1_B/ SCL1 B					TS18	IRQ4
4	-	-	-	-		P403			GTIOC3A _B			CTS1_RT S1_B/					TS17	
5	3	3	2	A1	VCL							331_B						
6	4	4	3	B1	XCIN	P215												
7	5	5	4	C1	XCOUT	P214												
8	6	6	5	D1	VSS													
9	7	7	6	D3	XTAL	P213		GTETRG A_D				TXD1_A/ MOSI1_A/						IRQ2
10	8	8	7	D2	EXTAL	P212	AGTEE1	GTETRG B_D				RXD1_A/ MISO1_A/						IRQ3
11	9	9	8	E1	VCC							SCL1_A						
12	-	-	-	-		P411	AGTOA1	GTOVUP _B	GTIOC6A _B			TXD0_B/ MOSI0_B/ SDA0_B		MOSIA_B			TS07	IRQ4
13	-	-	-	-		P410	AGTOB1	GTOVLO _B	GTIOC6B _B			RXD0_B/ MISO0_B/ SCL0_B		MISOA_B			TS06	IRQ5
14	10	10	-	-		P409		GTOWUP _B	GTIOC5A _B			TXD9_A/ MOSI9_A/					TS05	IRQ6
15	11	11	9	-		P408		GTOWLO	GTIOC5B _B			RXD9_A/ MISO9_A/					TS04	IRQ7
16	12	12	10	E2		P407				RTCOUT	USB_VBU S	CTS0_RT S0_D/	SDA0_B	SSLB3_A	ADTRG0_ B		TS03	
17	13	13	11	F1	VSS_USB							330_D						
18	14	14	12	F2							USB_DM							
19	15	15	13	F3							USB_DP							
20	16	16	14	F4	VCC_US B													
21	17	17	15	F5	VCC_US B LDO													
22	18	18	-	-	_	P206		GTIU_A				RXD0_D/ MISO0_D/ SCL0_D	SDA1_A	SSLB1_A			TS01	IRQ0
23	-	-	-	-	CLKOUT_ A	P205	AGTO1	GTIV_A	GTIOC4A _B			TXD0_D/ MOSI0_D/ SDA0_D/ CTS9_RT S9_A/ SS9_A	SCL1_A	SSLB0_A			TSCAP_A	IRQ1
24	-	-	-	-	CACREF_ A	P204	AGTIO1_ A	GTIW_A	GTIOC4B _B			SCK0_D/ SCK9_A	SCL0_B	RSPCKB_ A			TS00	
25	19	19	16	E3	RES													
26	20	20	17	E4	MD	P201												
27	21	21	18	E5		P200												NMI
28	-	-	-	-		P304			GTIOC1A _B									
29	-	-	-	-		P303			GTIOC1B _B								TS02	
30	22	22	-	-		P302		GTOUUP _A	GTIOC4A _A					SSLB3_B			TS08	IRQ5
31	23	23	19	-		P301		GTOULO _A	GTIOC4B _A					SSLB2_B			TS09	IRQ6
32	24	24	20	F6	SWCLK	P300		GTOUUP _C	GTIOC0A _A					SSLB1_B				
33	25	25	21	E6	SWDIO	P108		GTOULO _C	GTIOC0B _A			CTS9_RT S9_B/ SS9_B		SSLB0_B				
34	26	26	22	D4	CLKOUT_ B	P109		GTOVUP _A	GTIOC1A _A		CTX0_A	TXD9_B/ MOSI9_B/ SDA9_B		MOSIB_B			TS10	



2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

 $VCC^{*1} = AVCC0 = VCC_USB^{*2} = VCC_USB_LDO^{*2} = 1.6$ to 5.5V, VREFH0 = 1.6 to AVCC0,

 $VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, Ta = T_{opr}$

Note 1. The typical condition is set to VCC = 3.3V.

Note 2. When USBFS is not used.

Figure 2.1 shows the timing conditions.



Figure 2.1 Input or output timing measurement conditions

The measurement conditions of timing specification in each peripherals are recommended for the best peripheral operation. However, make sure to adjust driving abilities of each pins to meet your conditions.

Each function pin used for the same function must select the same drive ability. If I/O drive ability of each function is mixed, the AC specification of the function is not guaranteed.



Table 2.9 I/O V_{OH}, V_{OL} (3)

	UII/	
Conditions: VO	CC = AVCC0 =	1.6 to 2.7 V

Parameter		Symbol	Min	Тур	Max	Unit	Test conditions	
Output voltage	put voltage Ports P000 to P004 P010 to P015		V _{OH}	AVCC0 – 0.3	-	-		I _{OH} = -0.5 mA
			V _{OL}	-	-	0.3		I _{OL} = 0.5 mA
		Middle drive	V _{OH}	AVCC0 – 0.3	-	-		I _{OH} = -1.0 mA
			V _{OL}	-	-	0.3		I _{OL} = 1.0 mA
	Other output pins*1	Low drive	V _{OH}	VCC - 0.3	-	-	V	I _{OH} = -0.5 mA
			V _{OL}	-	-	0.3		I _{OL} = 0.5 mA
		Middle drive*2	V _{OH}	VCC - 0.3	-	-		I _{OH} = -1.0 mA
			V _{OL}	-	-	0.3		I _{OL} = 1.0 mA

Note 1. Except for Ports P200, P214, P215, which are input ports.

Note 2. Except for P212, P213.

Table 2.10I/O other characteristics

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Тур	Max	Unit	Test conditions
Input leakage current	RES, Ports P200, P214, P215	I _{in}	-	-	1.0	μA	V _{in} = 0 V V _{in} = VCC
Three-state leakage current (off state)	I _{TSI}	-	-	1.0	μA	V _{in} = 0 V V _{in} = 5.8 V	
	Other ports		-	-	1.0		V _{in} = 0 V V _{in} = VCC
Input pull-up resistor	All ports (except for P200, P214, P215)	R _U	10	20	50	kΩ	V _{in} = 0 V
Input capacitance	USB_DP, USB_DM, P200	C _{in}	-	-	30	pF	V _{in} = 0 V
	Other input pins		-	-	15		f = 1 MHz T _a = 25°C





Figure 2.22 Temperature dependency in Software Standby mode (reference data)



Figure 2.23 Temperature dependency of RTC operation (reference data)

Tab	le 2.1	3	Operatin	g and	standby	current	(3) (1 of 2)	
~								

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Тур	Max	Unit	Test conditions
Analog power	During A/D conversion (at high-speed conversion)	I _{AVCC}	-	-	3.0	mA	-
supply current	During A/D conversion (at low-power conversion)		-	-	1.0	mA	-
	During D/A conversion*1	-	-	0.4	0.8	mA	-
	Waiting for A/D and D/A conversion (all units)*5		-	-	1.0	μA	-
Reference	During A/D conversion	I _{REFH0}	-	-	150	μA	-
power supply current	Waiting for A/D conversion (all units)		-	-	60	nA	-
Temperature sensor			-	75	-	μA	-



2.3.3 Reset Timing

Table 2.22 Reset timing

Parameter	Symbol	Min	Тур	Max	Unit	Test conditions	
RES pulse width	At power-on	t _{RESWP}	3	-	-	ms	Figure 2.29
	Not at power-on	t _{RESW}	30	-	-	μs	Figure 2.30
Wait time after RES cancellation	LVD0 enabled*1	t _{RESWT}	-	0.7	-	ms	Figure 2.29
(at power-on)	LVD0 disabled*2		-	0.3	-		
Wait time after RES cancellation	LVD0 enabled*1	t _{RESWT2}	-	0.5	-	ms	Figure 2.30
(during powered-on state)	LVD0 disabled*2		-	0.05	-		
Internal reset cancellation time (Watchdog	LVD0 enabled*1	t _{RESWT3}	-	0.6	-	ms	
Software reset)	LVD0 disabled*2		-	0.15	-		

Note 1. When OFS1.LVDAS = 0.

Note 2. When OFS1.LVDAS = 1.



Figure 2.29 Reset input timing at power-on



Figure 2.30 Reset input timing (1)



2.3.4 Wakeup Time

Table 2.23	Timing of recovery from low power modes (1)
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Parameter	Symbol	Min	Тур	Max	Unit	Test conditions			
Recovery time from Software Standby mode ^{*1}	Recovery time High-speed Crystal from Software Standby mode ^{*1} High-speed crystal resonator resonator (main clock oscillator		System clock source is main clock oscillator (20 MHz) ^{*2}	t _{SBYMC}	-	2	3	ms	Figure 2.31
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz) ^{*3}	t _{SBYEX}	-	14	25	μs	
		System clock source is HOCO ^{*4} (HOCO clock is 32 MHz)		t _{SBYHO}	-	43	52	μs	
		System clock sou (HOCO clock is 4	t _{SBYHO}	-	44	52	μs		
		System clock source is HOCO ^{*5} (HOCO clock is 64 MHz)		t _{SBYHO}	-	82	110	μs	
		System clock sou	urce is MOCO	t _{SBYMO}	-	16	25	μs	

Note 1. The division ratio of ICK and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.

Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Note 4. The HOCO clock wait control register (HOCOWTCR) is set to 05h.

Note 5. The HOCO clock wait control register (HOCOWTCR) is set to 06h.

Table 2.24Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Тур	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (12 MHz)* ²	t _{SBYMC}	-	2	3	ms	Figure 2.31
		External clock input to main clock oscillator	System clock source is main clock oscillator (12 MHz)* ³	t _{SBYEX}	-	2.9	10	μs	
		System clock source is HOCO*4 System clock source is MOCO		t _{SBYHO}	-	38	50	μs	
				t _{SBYMO}	-	3.5	5.5	μs	

Note 1. The division ratio of ICK and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.

Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Note 4. The system clock is 12 MHz.





Figure 2.45 SCI simple SPI mode timing (master, CKPH = 0)









Figure 2.53 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to 1/2)



Figure 2.54 SPI timing (slave, CPHA = 0)



2.3.11 CLKOUT Timing

Table 2.37 CLKOUT timing

Parameter			Symbol	Min	Max	Unit*1	Test conditions
CLKOUT	CLKOUT pin output cycle*1	VCC = 2.7 V or above	t _{Ccyc}	62.5	-	ns	Figure 2.57
		VCC = 1.8 V or above		125	-		
		VCC = 1.6 V or above		250	-		
	CLKOUT pin high pulse width*2	VCC = 2.7 V or above	t _{CH}	15	-	ns	
		VCC = 1.8 V or above		30	-		
		VCC = 1.6 V or above		150	-		
	CLKOUT pin low pulse width*2	VCC = 2.7 V or above	t _{CL}	15	-	ns	
		VCC = 1.8 V or above		30	-		
		VCC = 1.6 V or above		150	-		
	CLKOUT pin output rise time	VCC = 2.7 V or above	t _{Cr}	-	12	ns	
		VCC = 1.8 V or above		-	25		
		VCC = 1.6 V or above		-	50		
	CLKOUT pin output fall time	VCC = 2.7 V or above	t _{Cf}	-	12	ns	
		VCC = 1.8 V or above		-	25		
		VCC = 1.6 V or above		-	50		

Note 1. When the EXTAL external clock input or an oscillator is used with division by 1 (the CKOCR.CKOSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

Note 2. When the MOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 001b), set the clock output division ratio selection to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).



Figure 2.57 CLKOUT output timing



2.5 ADC14 Characteristics



Figure 2.61 AVCC0 to VREFH0 voltage range

Table 2.40	A/D conversion	characteristics (1) in high-speed	A/D conversion	mode (1 of 2)
Conditions: VCC	= AVCC0 = 4.5 to 5.	5 V, VREFH0 = 4.5	to 5.5 V, VSS = AV	SS0 = VREFL0 = 0\	/
Reference voltage	e range applied to th	e VREFH0 and VRE	EFLO.		

Parameter			Min	Тур	Мах	Unit	Test Conditions
Frequency			1	-	64	MHz	-
Analog input capacitance	*2	Cs	-	-	8* ³	pF	High-precision channel
			-	-	9* ³	pF	Normal-precision channel
Analog input resistance		Rs	-	-	2.5* ³	kΩ	High-precision channel
			-	-	6.7* ³	kΩ	Normal-precision channel
Analog input voltage rang	e	Ain	0	-	VREFH0	V	-
12-bit mode							
Resolution			-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 64 MHz)	Conversion time*1Permissible signal source impedance(Operation at PCLKD = 64 MHz)Max. = 0.3 kΩ		0.70	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
			1.13	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error			-	±0.5	±4.5	LSB	High-precision channel
					±6.0	LSB	Other than above
Full-scale error			-	±0.75	±4.5	LSB	High-precision channel
					±6.0	LSB	Other than above
Quantization error			-	±0.5	-	LSB	-
Absolute accuracy			-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above	
DNL differential nonlinearity error			-	±1.0	-	LSB	-
INL integral nonlinearity e	error		-	±1.0	±3.0	LSB	-
14-bit mode							
Resolution			-	-	14	Bit	-



Table 2.41A/D conversion characteristics (2) in high-speed A/D conversion mode (2 of 2)Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V

Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Тур	Мах	Unit	Test Conditions
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1Permissible sign(Operation atsource impedanPCLKD = 48 MHz)Max. = 0.3 kΩ		1.06	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.63	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity	error	-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see section 2.2.4, I/O VOH, VOL, and Other Characteristics.

Note 3. Reference data.

Table 2.42 A/D conversion characteristics (3) in high-speed A/D conversion mode (1 of 2) Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V Reference voltage range applied to the VREFH0 and VREFL0.

Parameter			Min	Тур	Max	Unit	Test Conditions
Frequency			1	-	32	MHz	-
Analog input capacitance	e* ²	Cs		-	8* ³	pF	High-precision channel
			-	-	9* ³	pF	Normal-precision channel
Analog input resistance		Rs	-	-	2.5* ³	kΩ	High-precision channel
			-	-	6.7* ³	kΩ	Normal-precision channel
Analog input voltage range Ain		Ain	0	-	VREFH0	V	-
12-bit mode						1	
Resolution			-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 32 MHz)Permissible source imp Max. = 1.3		Permissible signal source impedance Max. = 1.3 kΩ		-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
			2.25	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error	•		-	±0.5	±4.5	LSB	High-precision channel
					±6.0	LSB	Other than above
Full-scale error			-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above	
Quantization error			-	±0.5	-	LSB	-
Absolute accuracy			-	±1.25	±5.0	LSB	High-precision channel
					±8.0	LSB	Other than above



Table 2.42 A/D conversion characteristics (3) in high-speed A/D conversion mode (2 of 2) Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V

Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Тур	Max	Unit	Test Conditions
DNL differential nonlinea	arity error	-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode					·	
Resolution		-	-	14	Bit	-
Conversion time ^{*1} (Operation at PCLKD = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.59	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		2.44	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinea	arity error	-	±4.0	-	LSB	-
INL integral nonlinearity	error	-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see section 2.2.4, I/O VOH, VOL, and Other Characteristics.

Note 3. Reference data.

Table 2.43 A/D conversion characteristics (4) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V Reference voltage range applied to the VREFH0 and VREFL0.

Parameter			Min	Тур	Max	Unit	Test Conditions		
Frequency			1	-	24	MHz	-		
Analog input capacitance	e*2	Cs	-	-	8* ³	pF	High-precision channel		
			-	-	9* ³	pF	Normal-precision channel		
Analog input resistance		Rs	-	-	2.5* ³	kΩ	High-precision channel		
			-	-	6.7* ³	kΩ	Normal-precision channel		
Analog input voltage range Ain		0	-	VREFH0	V	-			
12-bit mode									
Resolution			-	-	12	Bit	-		
Conversion time ^{*1} (Operation at PCLKD = 24 MHz)	Conversion time*1Permissible(Operation atsource impPCLKD = 24 MHz)Max. = 1.1		2.25	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh		
			3.38	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h		
Offset error			-	±0.5	±4.5	LSB	High-precision channel		
					±6.0	LSB	Other than above		
Full-scale error			-	±0.75	±4.5	LSB	High-precision channel		
					±6.0	LSB	Other than above		
Quantization error			-	±0.5	-	LSB	-		



Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions
Power-on reset enable time	t _{W (POR)}	1	-	-	ms	Figure 2.67, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)	T _{d (E-A)}	-	-	300	μs	Figure 2.69, Figure 2.70
Hysteresis width (POR)	V _{PORH}	-	110	-	mV	-
Hysteresis width (LVD0, LVD1, and LVD2)	V _{LVH}	-	60	-	mV	LVD0 selected
		-	100	-		V_{det1_0} to V_{det1_2} selected.
		-	60	-		V_{det1_3} to V_{det1_9} selected.
		-	50	-		V_{det1_A} to V_{det1_B} selected.
		-	40	-		V _{det1_C} to V _{det1_F} selected.
		-	60	-		LVD2 selected

Table 2.53	Power-on reset circuit and voltage detection circuit characteristics (2) (2 of	2)
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Note 1. When OFS1.LVDAS = 0

Note 2. When OFS1.LVDAS = 1

Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det0} , V_{det1} , and V_{det2} for the POR/LVD.



Figure 2.66 Voltage detection reset timing



Figure 2.67 Power-on reset timing

Serial Wire Debug (SWD) 2.12.3

Table 2.62SWD characteristics (1)Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter	Symbol	Min	Тур	Max	Unit	Test conditions
SWCLK clock cycle time	t _{SWCKcyc}	80	-	-	ns	Figure 2.71
SWCLK clock high pulse width	t _{swcкн}	35	-	-	ns	
SWCLK clock low pulse width	t _{SWCKL}	35	-	-	ns	
SWCLK clock rise time	t _{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t _{SWCKf}	-	-	5	ns	
SWDIO setup time	t _{SWDS}	16	-	-	ns	Figure 2.72
SWDIO hold time	t _{SWDH}	16	-	-	ns	
SWDIO data delay time	t _{SWDD}	2	-	70	ns	

Table 2.63 SWD characteristics (2)

Conditions: VCC = AVCC0 = 1.6 to 2.4 V

Parameter	Symbol	Min	Тур	Max	Unit	Test conditions
SWCLK clock cycle time	t _{SWCKcyc}	250	-	-	ns	Figure 2.71
SWCLK clock high pulse width	t _{SWCKH}	120	-	-	ns	-
SWCLK clock low pulse width	t _{SWCKL}	120	-	-	ns	-
SWCLK clock rise time	t _{SWCKr}	-	-	5	ns	-
SWCLK clock fall time	t _{SWCKf}	-	-	5	ns	-
SWDIO setup time	t _{SWDS}	50	-	-	ns	Figure 2.72
SWDIO hold time	t _{SWDH}	50	-	-	ns	
SWDIO data delay time	t _{SWDD}	2	-	150	ns	











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Figure 1.3 LGA 36-pin



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