Renesas Electronics America Inc - R7FS124773A01CFM#AA1 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 18x14b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs124773a01cfm-aa1

Table 1.6 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with 1 channel and a 16-bit timer with 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms for controlling brushless DC motors can be generated. The GPT can also be used as a general-purpose timer. See section 19, General PWM Timer (GPT) in User's Manual.
Port Output Enable for GPT (POEG)	Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 18, Port Output Enable for GPT (POEG) in User's Manual.
Asynchronous General Purpose Timer (AGT)	The Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and they can be accessed with the AGT register. See section 20, Asynchronous General Purpose Timer (AGT) in User's Manual.
Realtime Clock (RTC)	The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 21, Realtime Clock (RTC) in User's Manual.

Table 1.7 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communication Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: • Asynchronous interfaces (UART and asynchronous communications interface adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCI0 has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 25, Serial Communications Interface (SCI) in User's Manual.
I^2C Bus interface (IIC)	The MCU has a two-channel I^2C bus interface (IIC). The IIC module conforms with and provides a subset of the NXP I^2C bus (Inter-Integrated Circuit bus) interface functions. See section 26, I2C Bus Interface (IIC) in User's Manual.
Serial Peripheral Interface (SPI)	The MCU includes two independent channels of the Serial Peripheral Interface (SPI). The SPI channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 28, Serial Peripheral Interface (SPI) in User's Manual.
Controller Area Network (CAN) Module	The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 27, Controller Area Network (CAN) Module in User's Manual.

1.4 Function Comparison

Table 1.13 Function comparison

Parts number		R7FS124773A01CFM/ R7FS124763A01CFM/ R7FS124773A01CNB/	R7FS124773A01CFL/ R7FS124763A01CFL/ R7FS124773A01CNE	R7FS124773A01CNF	R7FS124772A01CLM/ R7FS124762A01CLM
Pin count		64	48	40	36
Package		LQFP/QFN	LQFP/QFN	QFN	LGA
Code flash memory		128/64 KB			
Data flash memory		4 KB			
SRAM		16 KB			
	Parity	4 KB			
System	CPU clock	32 MHz			
	ICU	Yes			
	KINT	8	5	5	4
Event link	ELC	Yes			
DMA	DTC	Yes			
Timers	GPT32	1			
	GPT16	6	6	4	4
	AGT	2	2	2	2
	RTC	Yes			
	WDT/IWDT	Yes			
Communication	SCI	3			
	IIC	2			
	SPI	2			
	CAN	Yes			
	USBFS	Yes			
Analog	ADC14	18	14	12	11
	DAC12	1			
	ACMPLP	2			
	TSN	Yes			
HMI	CTSU	31	23	17	13
	KINT	8	5	5	4
Data processing	CRC	Yes			
	DOC	Yes			
Security		AES and TRNG			

Table 1.14 Pin functions (3 of 3)

Function	Signal	I/O	Description
ACMPLP	VCOUT	Output	Comparator output pin.
	CMPREF0, CMPREF1	Input	Reference voltage input pins.
	CMPIN0, CMPIN1	Input	Analog voltage input pins.
CTSU	TS00 to TS28, TS30, TS31	Input	Capacitive touch detection pins (touch pins).
	TSCAP	-	Secondary power supply pin for the touch driver.
KINT	KR00 to KR07	Input	Key interrupt input pins.
I/O ports	P000 to P004, P010 to P015	I/O	General-purpose input/output pins.
	P100 to P113	I/O	General-purpose input/output pins.
	P200	Input	General-purpose input pin.
	P201, P204 to P206, P212, P213	I/O	General-purpose input/output pins.
	P214, P215	Input	General-purpose input pins.
	P300 to P304	I/O	General-purpose input/output pins.
	P400 to P403, P407 to P411	I/O	General-purpose input/output pins.
	P500 to P502	I/O	General-purpose input/output pins.

1.6 Pin Assignments

Figure 1.3 to Figure 1.8 show the pin assignments.

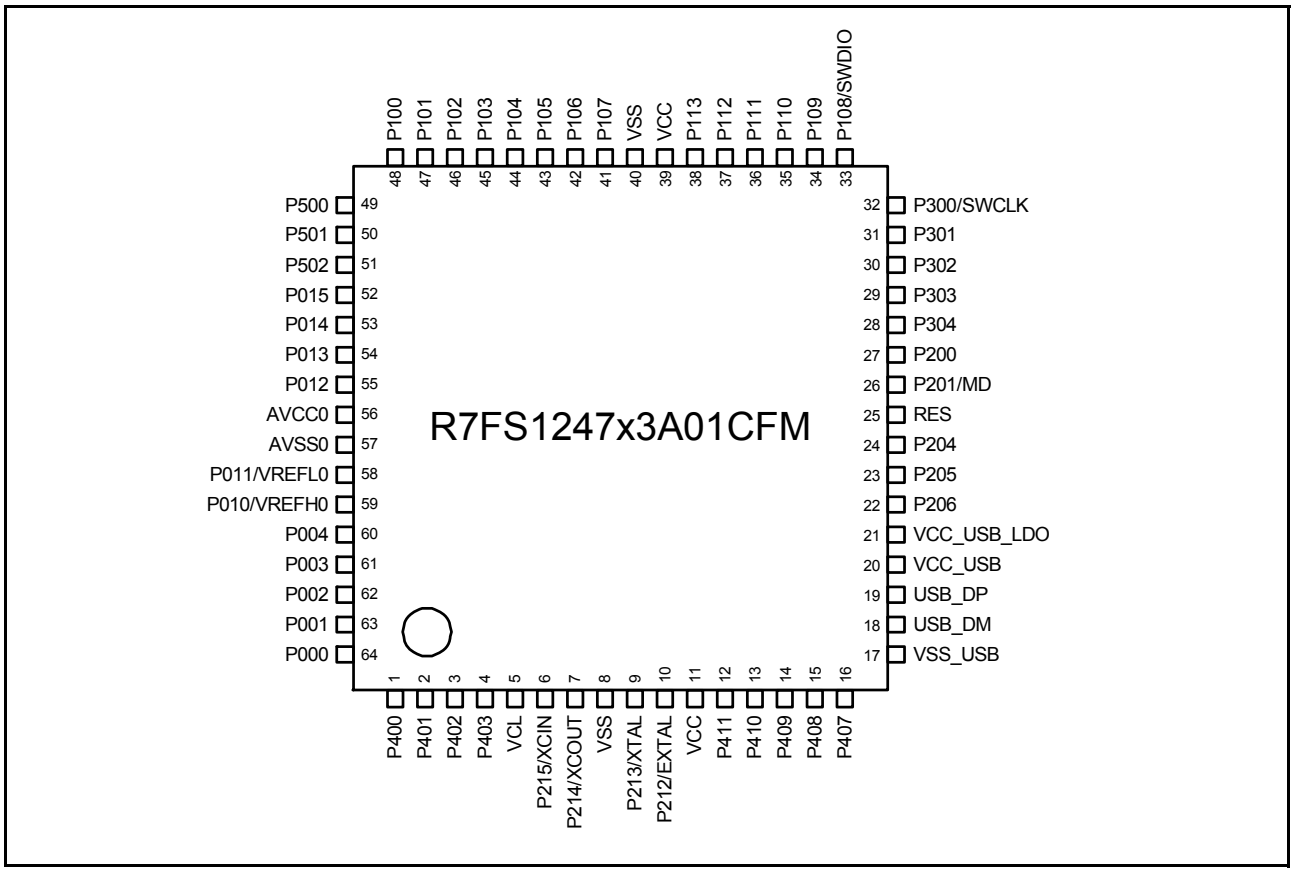


Figure 1.3 Pin assignment for LQFP 64-pin (top view)

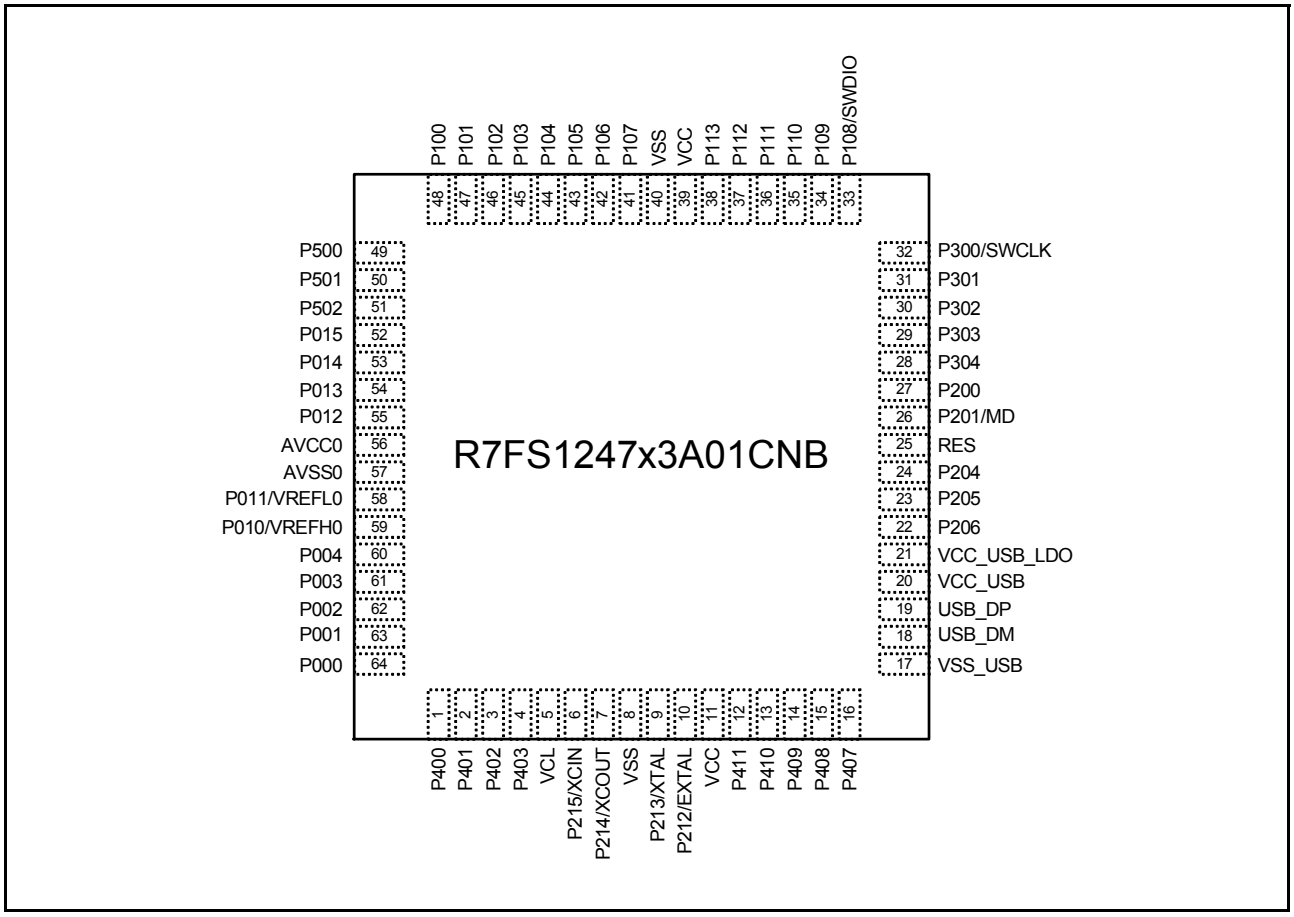


Figure 1.4 Pin assignment for QFN 64-pin (top view)

Pin number					Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication Interfaces				Analogs		HMI	
LQFP64, QFN64	LQFP48	QFN48	QFN40	LGA36			AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN	SCI	IIC	SPI	ADC14	DAC12, ACMPLP	CTSU	Interrupt
35	27	27	23	D5		P110		GTOVLO_A	GTIOC1B_A		CRX0_A	CTS0_RTS0_C/SS0_C/RXD9_B/MISO9_B/SCL9_B		MISOB_B		VCOUT	TS11	IRQ3
36	28	28	24	D6		P111			GTIOC3A_A			SCK0_C/SCK9_B		RSPCKB_B			TS12	IRQ4
37	29	29	25	C6		P112			GTIOC3B_A			TXD0_C/MOSI0_C/SDA0_C					TSCAP_C	
38	-	-	-	-		P113												
39	30	30	-	-	VCC													
40	31	31	-	-	VSS													
41	-	-	-	-		P107			GTIOC0A_B									KR07
42	-	-	-	-		P106			GTIOC0B_B					SSLA3_A				KR06
43	-	-	-	-		P105		GTETRGA_C						SSLA2_A				KR05/IRQ0
44	32	32	26	-		P104		GTETRGB_B				RXD0_C/MISO0_C/SCL0_C		SSLA1_A			TS13	KR04/IRQ1
45	33	33	27	C3		P103		GTOWUP_A	GTIOC2A_A		CTX0_C	CTS0_RTS0_A/SS0_A		SSLA0_A	AN019	CMPREF1	TS14	KR03
46	34	34	28	C4		P102	AGTO0	GTOWLO_A	GTIOC2B_A		CRX0_C	SCK0_A		RSPCKA_A	AN020/ADTRG0_A	CMPIN1	TS15	KR02
47	35	35	29	C5		P101	AGTEE0	GTETRGB_A	GTIOC5A_A			TXD0_A/MOSI0_A/SDA0_A/CTS1_RTS1_A/SS1_A	SDA1_B	MOSIA_A	AN021	CMPREF0	TS16	KR01/IRQ1
48	36	36	30	B6		P100	AGTIO0_A	GTETRGA_A	GTIOC5B_A			RXD0_A/MISO0_A/SCL0_A/SCK1_A	SCL1_B	MISOA_A	AN022	CMPIN0	TS26	KR00/IRQ2
49	37	37	-	-		P500	AGTOA0	GTIU_B	GTIOC2A_B						AN016		TS27	
50	-	-	-	-		P501	AGTOB0	GTIV_B	GTIOC2B_B						AN017			
51	-	-	-	-		P502		GTIW_B	GTIOC3B_B						AN018			
52	38	38	31	A6		P015									AN010		TS28	IRQ7
53	39	39	32	A5		P014									AN009	DA0		
54	40	40	33	B5		P013									AN008			
55	41	41	34	B4		P012									AN007			
56	42	42	35	A4	AVCC0													
57	43	43	36	A3	AVSS0													
58	44	44	37	B3	VREFL0	P011									AN006		TS31	
59	45	45	38	A2	VREFH0	P010									AN005		TS30	
60	-	-	-	-		P004									AN004		TS25	IRQ3
61	-	-	-	-		P003									AN003		TS24	
62	46	46	-	-		P002									AN002		TS23	IRQ2
63	47	47	39	-		P001									AN001		TS22	IRQ7
64	48	48	40	B2		P000									AN000		TS21	IRQ6

Note: Several pin names have the added suffix of _A, _B, _C, and _D. The suffix can be ignored when assigning functionality.

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC*1 = AVCC0 = VCC_USB*2 = VCC_USB_LDO*2 = 1.6 to 5.5V, VREFH0 = 1.6 to AVCC0,

VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3V.
Note 2. When USBFS is not used.

Figure 2.1 shows the timing conditions.

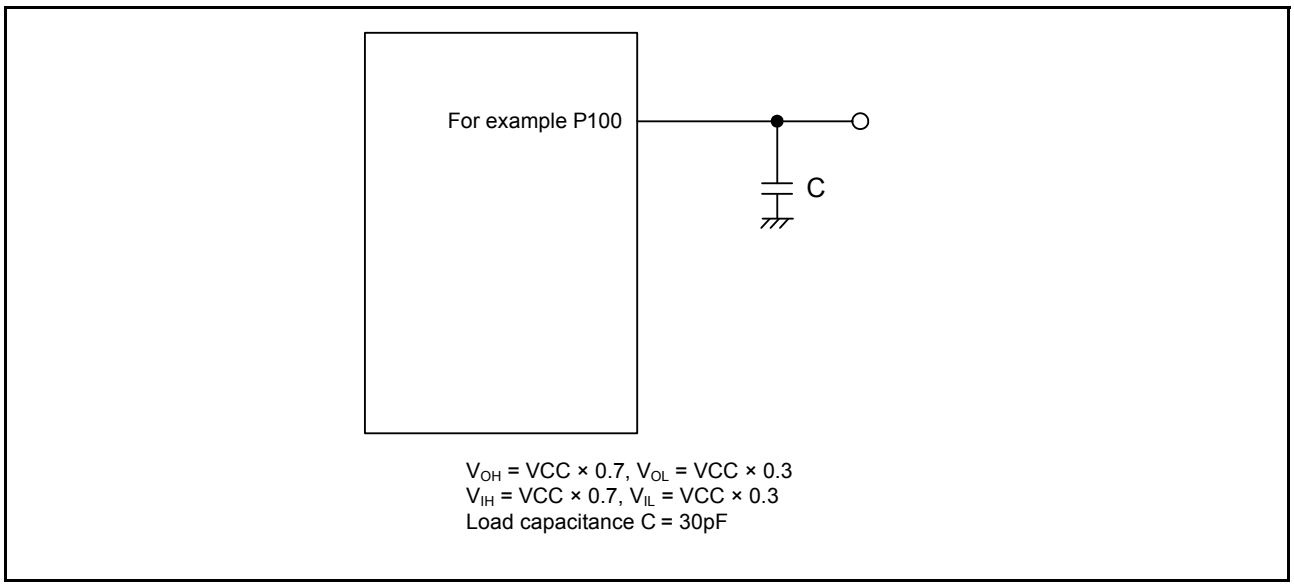


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of timing specification in each peripherals are recommended for the best peripheral operation. However, make sure to adjust driving abilities of each pins to meet your conditions.

Each function pin used for the same function must select the same drive ability. If I/O drive ability of each function is mixed, the AC specification of the function is not guaranteed.

Table 2.2 Recommended operating conditions

Parameter	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC*1, *2	When USBFS is not used	1.6	-	5.5	V
		When USBFS is used USB Regulator Disable	VCC_USB	-	3.6	V
		When USBFS is used USB Regulator Enable	VCC_USB_LDO	-	5.5	V
	VSS		-	0	-	V
USB power supply voltages	VCC_USB	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Disable (Input)	3.0	3.3	3.6	V
	VCC_USB_LDO	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Enable	3.8	-	5.5	V
		When USBFS is used USB Regulator Disable	-	VCC	-	V
	VSS_USB		-	0	-	V
Analog power supply voltages	AVCC0*1, *2		1.6	-	5.5	V
	AVSS0		-	0	-	V
	VREFH0	When used as ADC14 Reference	1.6	-	AVCC0	V
	VREFL0		-	0	-	V

Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.2 V and AVCC0 ≥ 2.2 V
AVCC0 = VCC when VCC < 2.2 V or AVCC0 < 2.2 V.

Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.7 I/O V_{OH}, V_{OL} (1)
Conditions: VCC = AVCC0 = 4.0 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC*1, *2		V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	-	-	0.6		I_{OL} = 6.0 mA
	Ports P408, P409*2, *3		V_{OH}	VCC – 1.0	-	-		I_{OH} = –20 mA
			V_{OL}	-	-	1.0		I_{OL} = 20 mA
	Ports P000 to P004 P010 to P015	Low drive	V_{OH}	AVCC0 – 0.8	-			I_{OH} = –2.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 2.0 mA
		Middle drive	V_{OH}	AVCC0 – 0.8	-			I_{OH} = –4.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 4.0 mA
	Other output pins*4	Low drive	V_{OH}	VCC – 0.8	-	-		I_{OH} = –2.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 2.0 mA
		Middle drive*5	V_{OH}	VCC – 0.8	-	-		I_{OH} = –4.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 4.0 mA

Note 1. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL1_A, SDA1_A, SCL1_B, SDA1_B (total 8 pins).
Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the PmnPFS register.
Note 3. Based on characterization data, not tested in production.
Note 4. Except for Ports P200, P214, and P215, which are input ports.
Note 5. Except for P212, P213.

Table 2.8 I/O V_{OH}, V_{OL} (2)
Conditions: VCC = AVCC0 = 2.7 to 4.0 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC*1, *2		V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	-	-	0.6		I_{OL} = 6.0 mA
	Ports P408, P409*2, *3		V_{OH}	VCC – 1.0	-	-		I_{OH} = –20 mA VCC = 3.3 V
			V_{OL}	-	-	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Ports P000 to P004 P010 to P015	Low drive	V_{OH}	AVCC0 – 0.5	-	-		I_{OH} = –1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
		Middle drive	V_{OH}	AVCC0 – 0.5	-	-		I_{OH} = –2.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 2.0 mA
	Other output pins*4	Low drive	V_{OH}	VCC – 0.5	-	-		I_{OH} = –1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
		Middle drive*5	V_{OH}	VCC – 0.5	-	-		I_{OH} = –2.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 2.0 mA

Note 1. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL1_A, SDA1_A, SCL1_B, SDA1_B (total 8 pins).
Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the PmnPFS register.
Note 3. Based on characterization data, not tested in production.
Note 4. Except for Ports P200, P214, P215, which are input ports.
Note 5. Except for P212, P213.

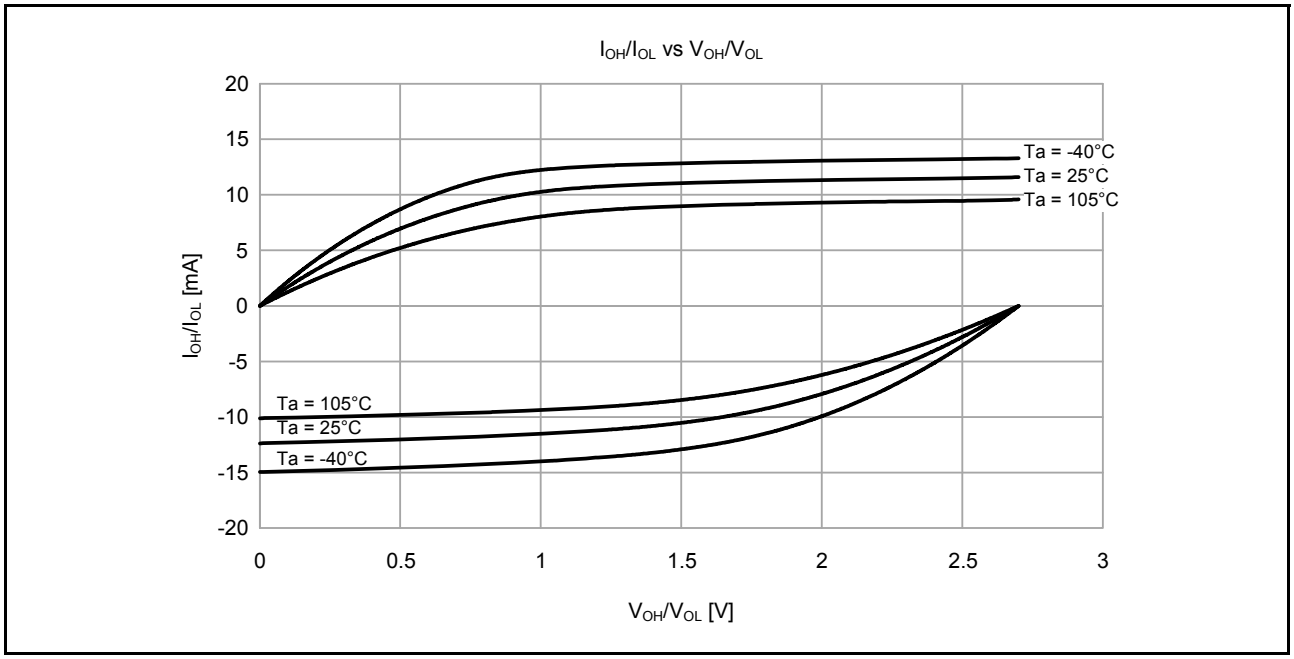


Figure 2.4 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 2.7 V when low drive output is selected (reference data)**

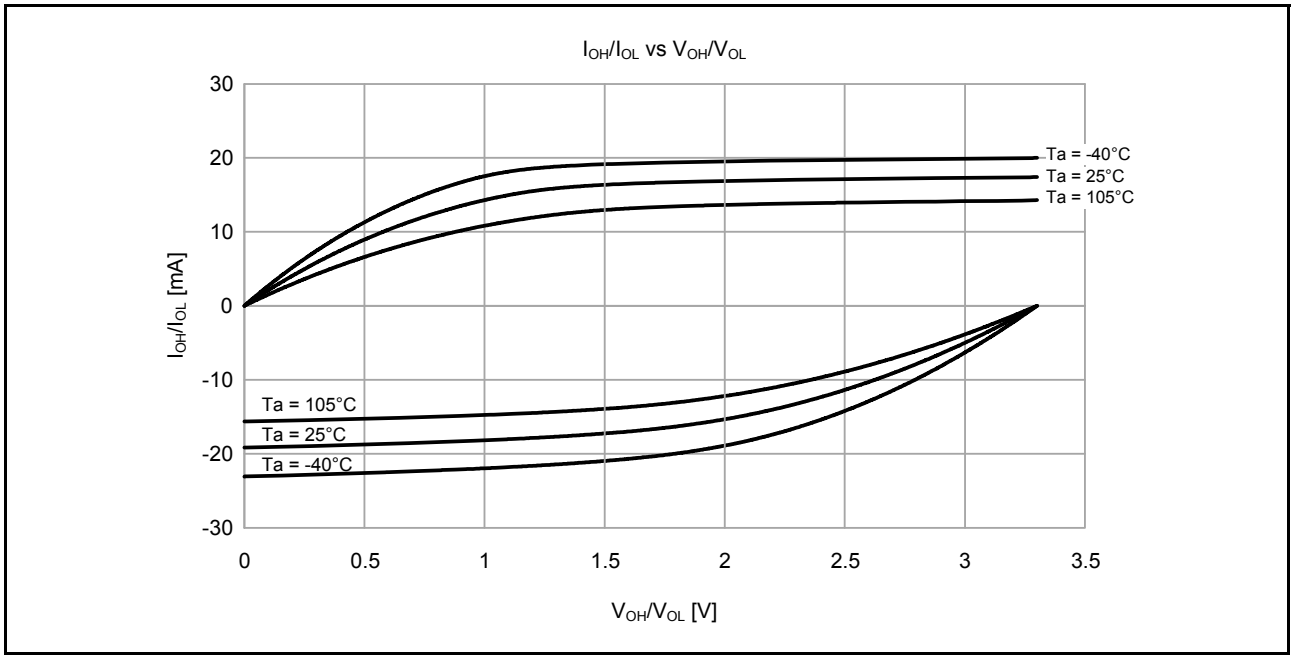


Figure 2.5 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 3.3 V when low drive output is selected (reference data)**

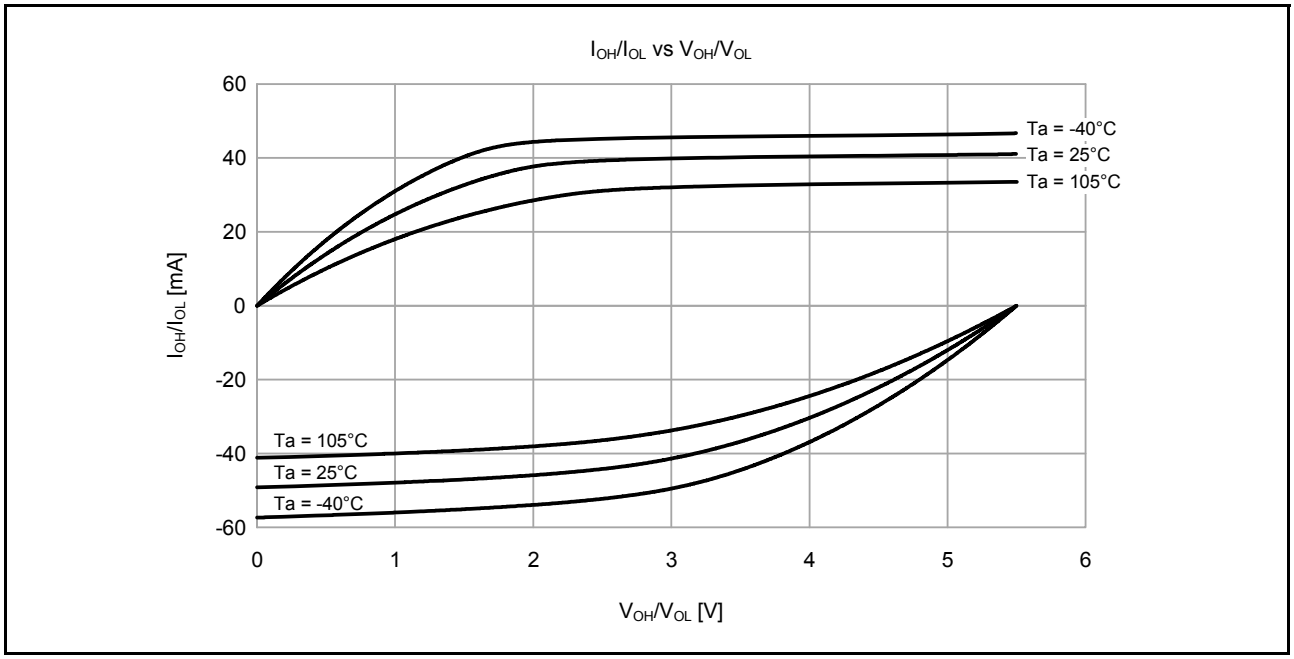


Figure 2.6 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 5.5 V when low drive output is selected (reference data)**

2.2.6 I/O Pin Output Characteristics of Middle Drive Capacity

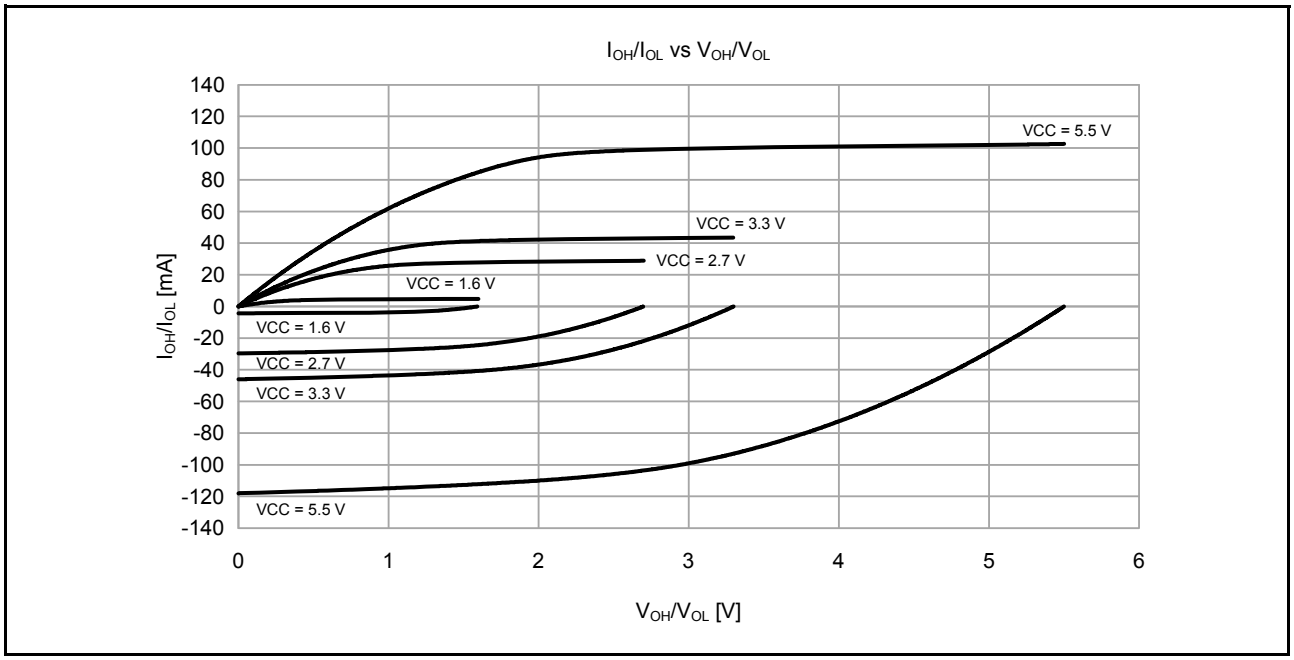
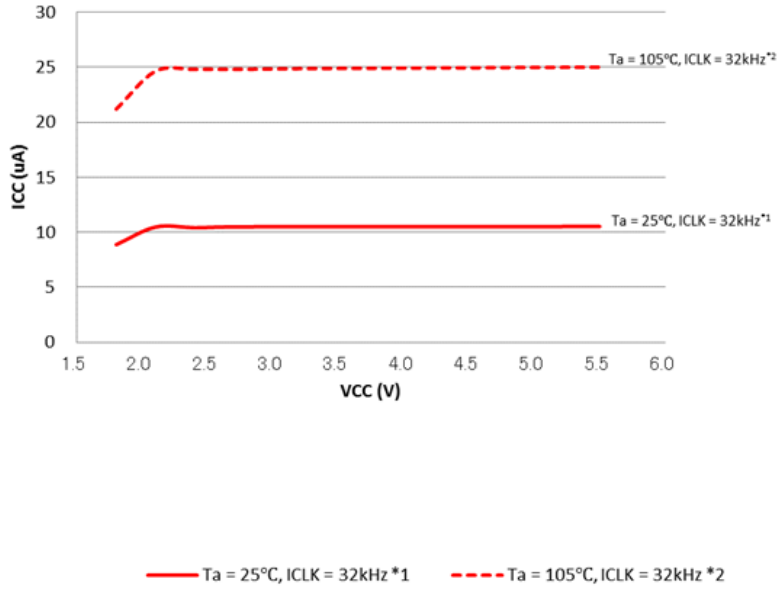


Figure 2.7 **V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C when middle drive output is selected (reference data)**



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.
Note 3. MOCO and DAC are stopped.

Figure 2.21 Voltage dependency in subosc-speed operating mode (reference data)

Table 2.12 Operating and standby current (2)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Typ*3	Max	Unit	Test conditions
Supply current*1	Software Standby mode*2	T_a = 25°C	I_{CC}	0.4	1.5	µA	-
		T_a = 55°C		0.6	5.5		
		T_a = 85°C		1.2	10.0		
		T_a = 105°C		2.6	40.0		
	Increment for RTC operation with low-speed on-chip oscillator*4			0.4	-		-
	Increment for RTC operation with sub-clock oscillator*4			0.5	-		SOMCR.SODRV[1:0] are 11b (Low power mode 3)
				1.3	-		SOMCR.SODRV[1:0] are 00b (normal mode)

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOS transistors are in the off state.
Note 2. The IWDT and LVD are not operating.
Note 3. VCC = 3.3 V.
Note 4. Includes the current of low-speed on-chip oscillator or sub-oscillation circuit.

2.3 AC Characteristics

2.3.1 Frequency

Table 2.16 Operation frequency in high-speed operating mode
Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1, *2, *4	2.7 to 5.5 V	f	0.032768	-	32	MHz
		2.4 to 2.7 V		0.032768	-	16	
	Peripheral module clock (PCLKB)*4	2.7 to 5.5 V		-	-	32	
		2.4 to 2.7 V		-	-	16	
	Peripheral module clock (PCLKD)*3, *4	2.7 to 5.5 V		-	-	64	
		2.4 to 2.7 V		-	-	16	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 2.21, Clock timing.

Table 2.17 Operation frequency in middle-speed mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1, *2, *4	2.7 to 5.5 V	f	0.032768	-	12	MHz
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	Peripheral module clock (PCLKB)*4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	Peripheral module clock (PCLKD)*3, *4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 2.21, Clock timing.

Table 2.25 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (1 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 2.31
		External clock input to main clock oscillator	System clock source is main clock oscillator (1 MHz)*3	t_{SBYEX}	-	28	50	µs	
		System clock source is MOCO		t_{SBYMO}	-	25	35	µs	

Note 1. The division ratio of ICK and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 2.26 Timing of recovery from low power modes (4)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-voltage mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (4 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 2.31
		External clock input to main clock oscillator	System clock source is main clock oscillator (4 MHz)*3	t_{SBYEX}	-	108	130	µs	
		System clock source is HOCO		t_{SBYHO}	-	108	130	µs	

Note 1. The division ratio of ICK and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 2.27 Timing of recovery from low power modes (5)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	SubOSC-speed mode	System clock source is sub-clock oscillator (32.768 kHz)	t_{SBYSC}	-	0.85	1	ms	Figure 2.31
		System clock source is LOCO (32.768 kHz)	t_{SBYLO}	-	0.85	1.2	ms	

Note 1. The sub-clock oscillator or LOCO itself continues oscillating in Software Standby mode during Subosc-speed mode.

2.3.5 NMI and IRQ Noise Filter

Table 2.29 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	-	-	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	-	-	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

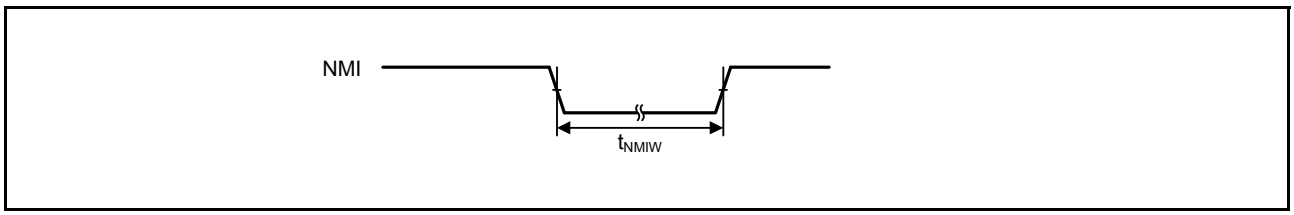


Figure 2.33 NMI interrupt input timing

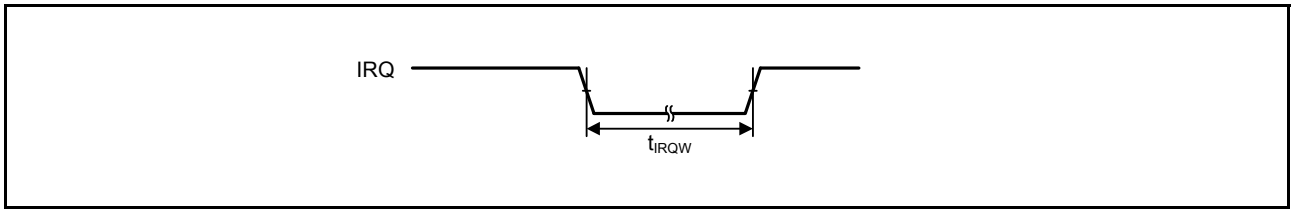


Figure 2.34 IRQ interrupt input timing

2.3.11 CLKOUT Timing

Table 2.37 CLKOUT timing

Parameter			Symbol	Min	Max	Unit*1	Test conditions
CLKOUT	CLKOUT pin output cycle*1	VCC = 2.7 V or above	t_{Ccyc}	62.5	-	ns	Figure 2.57
		VCC = 1.8 V or above		125	-		
		VCC = 1.6 V or above		250	-		
	CLKOUT pin high pulse width*2	VCC = 2.7 V or above	t_{CH}	15	-	ns	
		VCC = 1.8 V or above		30	-		
		VCC = 1.6 V or above		150	-		
	CLKOUT pin low pulse width*2	VCC = 2.7 V or above	t_{CL}	15	-	ns	
		VCC = 1.8 V or above		30	-		
		VCC = 1.6 V or above		150	-		
	CLKOUT pin output rise time	VCC = 2.7 V or above	t_{Cr}	-	12	ns	
		VCC = 1.8 V or above		-	25		
		VCC = 1.6 V or above		-	50		
	CLKOUT pin output fall time	VCC = 2.7 V or above	t_{Cf}	-	12	ns	
		VCC = 1.8 V or above		-	25		
		VCC = 1.6 V or above		-	50		

Note 1. When the EXTAL external clock input or an oscillator is used with division by 1 (the CKOCR.CKOSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

Note 2. When the MOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 001b), set the clock output division ratio selection to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).

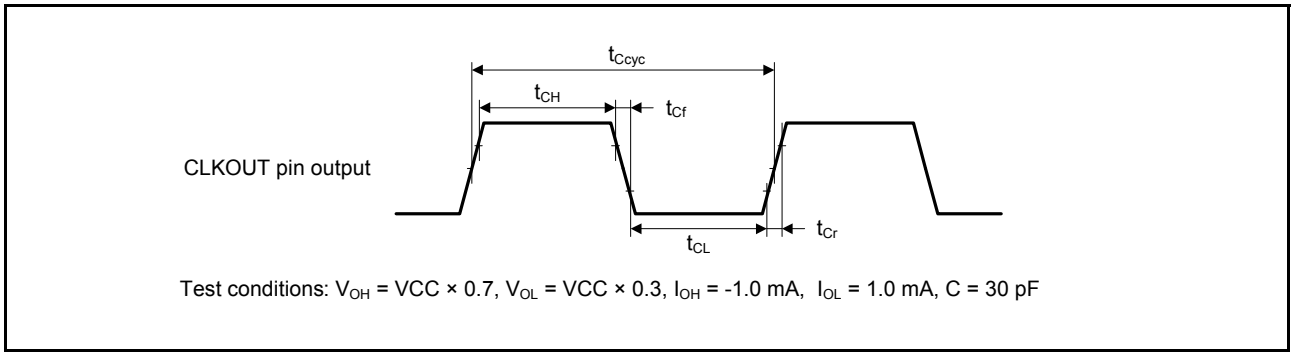


Figure 2.57 CLKOUT output timing

2.4 USB Characteristics

2.4.1 USBFS Timing

Table 2.38 USB characteristics

Conditions: VCC = AVCC0 = VCC_USB = 3.0 to 3.6V, Ta = –20 to +85°C

Parameter			Symbol	Min	Max	Unit	Test conditions
Input characteristics	Input high level voltage		V_{IH}	2.0	-	V	-
	Input low level voltage		V_{IL}	-	0.8	V	-
	Differential input sensitivity		V_{DI}	0.2	-	V	| USB_DP – USB_DM |
	Differential common mode range		V_{CM}	0.8	2.5	V	-
Output characteristics	Output high level voltage		V_{OH}	2.8	VCC_USB	V	I_{OH} = –200 µA
	Output low level voltage		V_{OL}	0.0	0.3	V	I_{OL}= 2 mA
	Cross-over voltage		V_{CRS}	1.3	2.0	V	Figure 2.58, Figure 2.59, Figure 2.60
	Rise time	FS	t_r	4	20	ns	
		LS		75	300		
	Fall time	FS	t_f	4	20	ns	
		LS		75	300		
	Rise/fall time ratio	FS	t_r/t_f	90	111.11	%	
		LS		80	125		
	Output resistance		Z_{DRV}	28	44	Ω	(Adjusting the resistance of external elements is not necessary.)
VBUS characteristics	VBUS input voltage		V_{IH}	VCC × 0.8	-	V	-
			V_{IL}	-	VCC × 0.2	V	-
Pull-up, pull-down	Pull-down resistor		R_{PD}	14.25	24.80	kΩ	-
	Pull-up resistor		R_{PUI}	0.9	1.575	kΩ	During idle state
			R_{PUA}	1.425	3.09	kΩ	During reception
Battery Charging Specification Ver 1.2	D + sink current		I_{DP_SINK}	25	175	µA	-
	D – sink current		I_{DM_SINK}	25	175	µA	-
	DCD source current		I_{DP_SRC}	7	13	µA	-
	Data detection voltage		V_{DAT_REF}	0.25	0.4	V	-
	D + source voltage		V_{DP_SRC}	0.5	0.7	V	Output current = 250 µA
	D – source voltage		V_{DM_SRC}	0.5	0.7	V	Output current = 250 µA

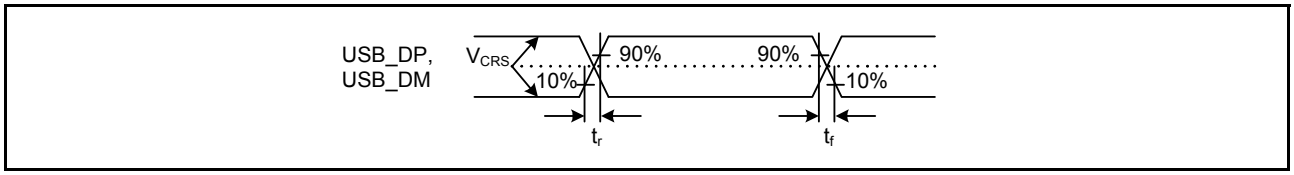


Figure 2.58 USB_DP and USB_DM output timing

Table 2.42 A/D conversion characteristics (3) in high-speed A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.59	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		2.44	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4, I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.

Table 2.43 A/D conversion characteristics (4) in low-power A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	24	MHz	-
Analog input capacitance*2	Cs	-	-	8*3	pF	High-precision channel
		-	-	9*3	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5*3	kΩ	High-precision channel
		-	-	6.7*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	2.25	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.38	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-

2.11 Comparator Characteristics

Table 2.55 ACMPLP characteristics
Conditions: VCC = AVCC0 = 1.8 to 5.5 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range		V_{REF}	0	-	VCC –1.4	V	-
Input voltage range		V_I	0	-	VCC	V	-
Internal reference voltage		-	1.36	1.44	1.50	V	-
Output delay	High-speed mode	T_d	-	-	1.2	µs	VCC = 3.0 Slew rate of input signal > 50 mV/µs
	Low-speed mode		-	-	5	µs	
	Window mode		-	-	2	µs	
Offset voltage	High-speed mode	-	-	-	50	mV	-
	Low-speed mode	-	-	-	40	mV	-
	Window mode	-	-	-	60	mV	-
Internal reference voltage for window mode		V_{RFH}	-	0.76 × VCC	-	V	-
		V_{RFL}	-	0.24 × VCC	-	V	-
Operation stabilization wait time		T_{cmp}	100	-	-	µs	-

2.12.3 Serial Wire Debug (SWD)

Table 2.62 SWD characteristics (1)
Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	80	-	-	ns	Figure 2.71
SWCLK clock high pulse width	t_{SWCKH}	35	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	35	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	
SWDIO setup time	t_{SWDS}	16	-	-	ns	Figure 2.72
SWDIO hold time	t_{SWDH}	16	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	70	ns	

Table 2.63 SWD characteristics (2)
Conditions: VCC = AVCC0 = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	250	-	-	ns	Figure 2.71
SWCLK clock high pulse width	t_{SWCKH}	120	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	120	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	
SWDIO setup time	t_{SWDS}	50	-	-	ns	Figure 2.72
SWDIO hold time	t_{SWDH}	50	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	150	ns	

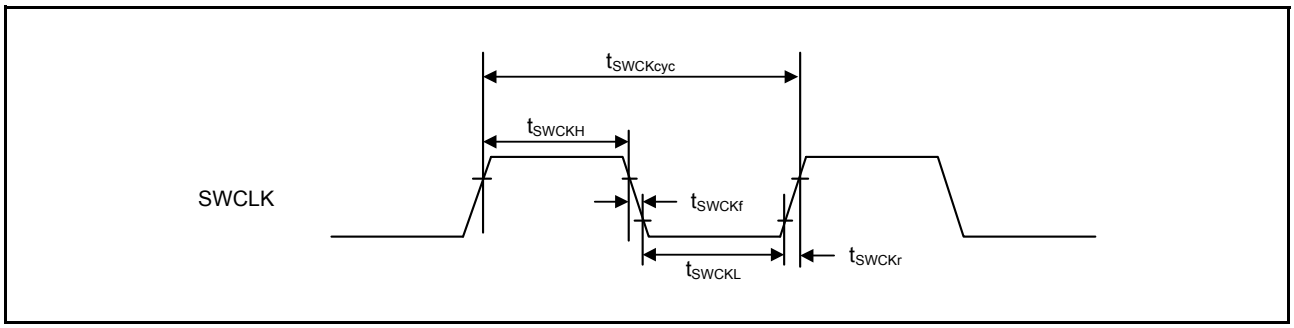


Figure 2.71 SWD SWCLK timing