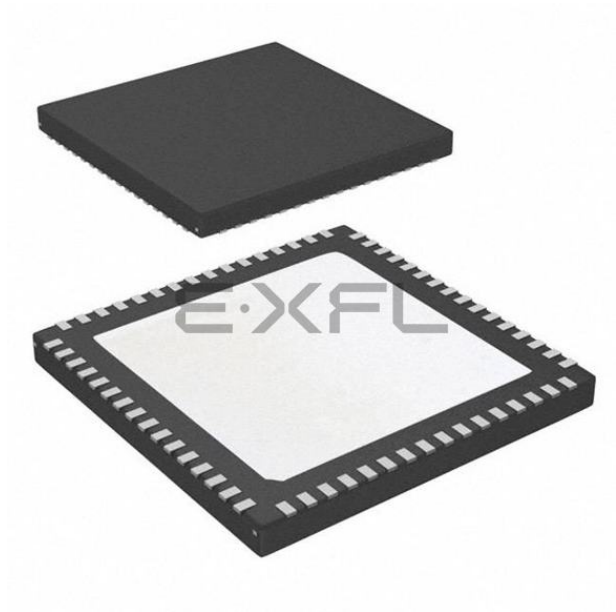
Renesas Electronics America Inc - R7FS124773A01CNB#AC0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 18x14b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-HWQFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs124773a01cnb-ac0

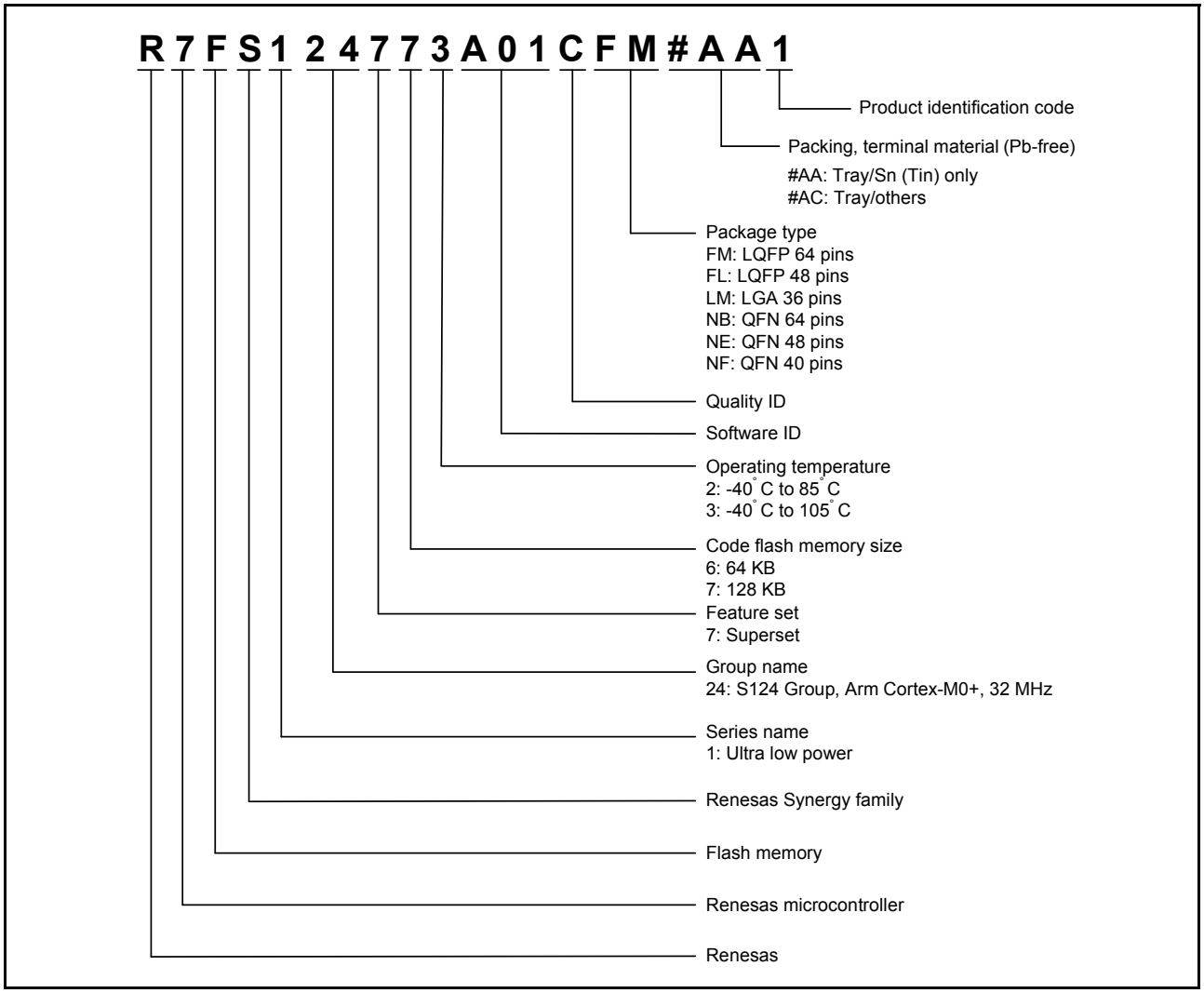


Figure 1.2 Part numbering scheme

Table 1.12 Product list

Product part number	Orderable part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FS124773A01CFM	R7FS124773A01CFM#AA1	PLQP0064KB-C	128 KB	4 KB	16 KB	–40 to +105°C
R7FS124773A01CNB	R7FS124773A01CNB#AC1	PWQN0064LA-A				–40 to +105°C
R7FS124773A01CFL	R7FS124773A01CFL#AA1	PLQP0048KB-B				–40 to +105°C
R7FS124773A01CNE	R7FS124773A01CNE#AC1	PWQN0048KB-A				–40 to +105°C
R7FS124773A01CNF	R7FS124773A01CNF#AC1	PWQN0040KC-A				–40 to +105°C
R7FS124772A01CLM	R7FS124772A01CLM#AC1	PWLG0036KA-A				–40 to +85°C
R7FS124763A01CFM	R7FS124763A01CFM#AA1	PLQP0064KB-C	64 KB			–40 to +105°C
R7FS124763A01CFL	R7FS124763A01CFL#AA1	PLQP0048KB-B				–40 to +105°C
R7FS124762A01CLM	R7FS124762A01CLM#AC1	PWLG0036KA-A				–40 to +85°C

Note: Earlier products with orderable part number suffix AA0 and AC0 have a restriction in AES functions. If AES functions are required for your application, refer to the products with orderable part number suffix AA1 or AC1. For details on the differences of AES functions between AA0/AC0 and AA1/AC1 products, see *Technical Update (TN-SY*-A024A/E)*. Contact your Renesas sales representative for additional information.

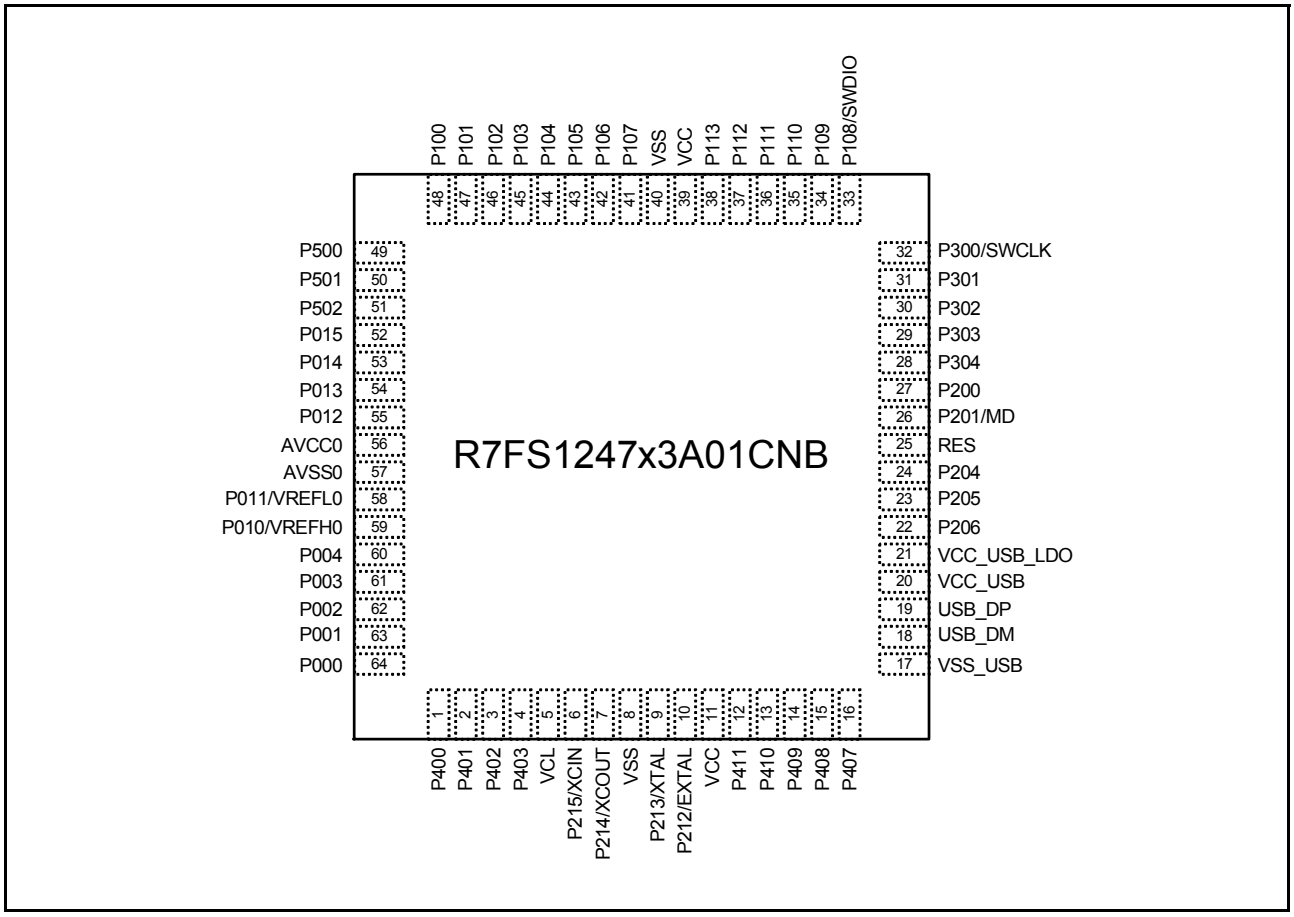


Figure 1.4 Pin assignment for QFN 64-pin (top view)

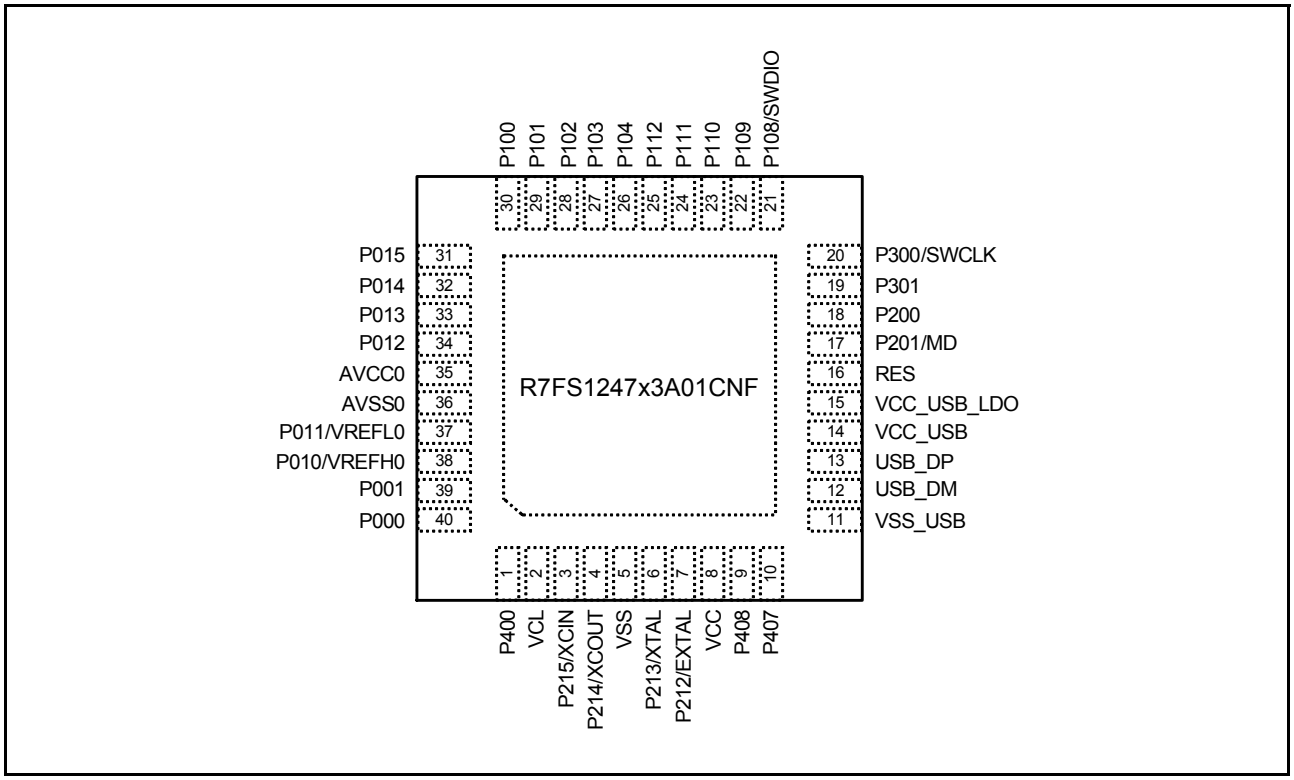


Figure 1.7 Pin assignment for QFN 40-pin (top view)

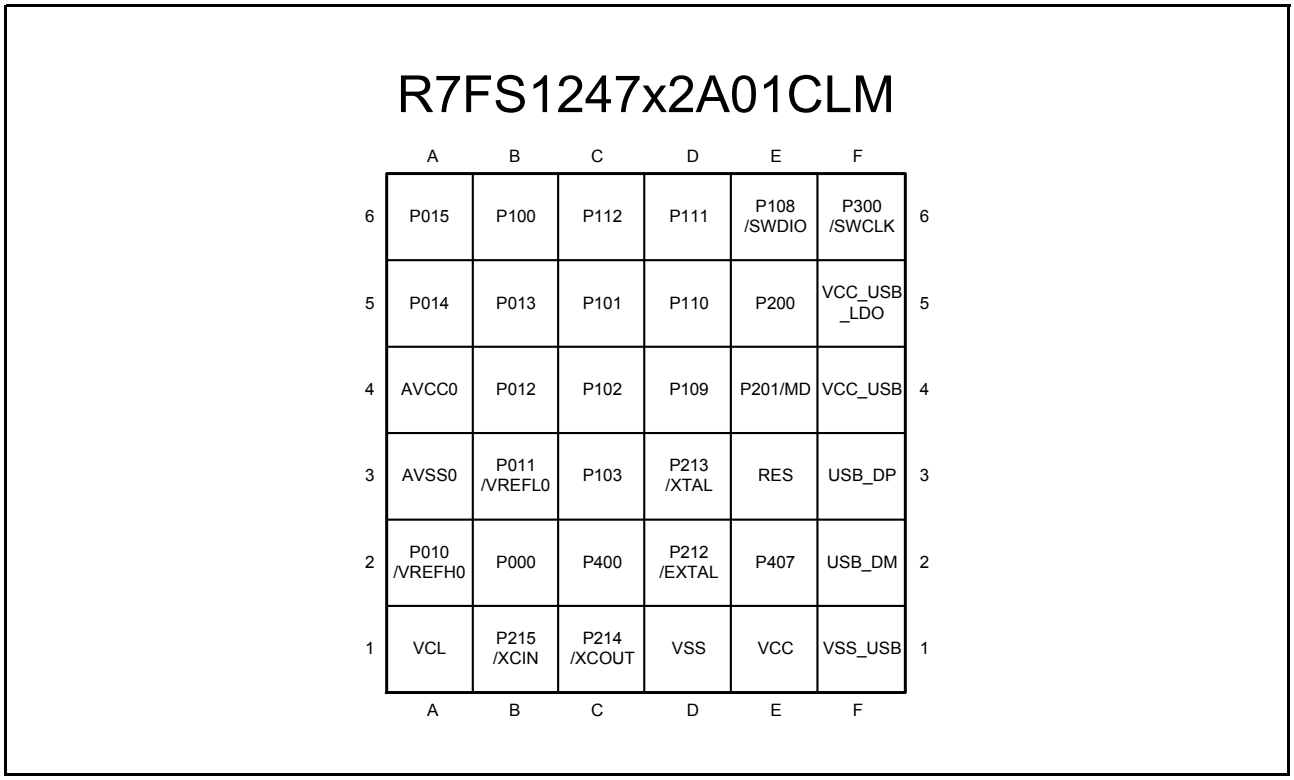


Figure 1.8 Pin assignment for LGA 36-pin (top view, pad side down)

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics
Conditions: Products with operating temperature (T_a) –40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	-	125	°C	High-speed mode Middle-speed mode Low-voltage mode Low-speed mode Subosc-speed mode
			105*1		

Note: Make sure that Tj = T_a + θja × total power consumption (W), where total power consumption = (VCC – V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.

Note 1. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, see section 1.3, Part Numbering. If the part number shows the operation temperature at 85°C, then the maximum value of Tj is 105°C, otherwise, it is 125°C.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} (1)
Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	IIC (except for SMBus)*1	V_{IH}	VCC × 0.7	-	5.8	V	-
		V_{IL}	-	-	VCC × 0.3		
		ΔV_T	VCC × 0.05	-	-		
	RES, NMI Other peripheral input pins excluding IIC	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		
		ΔV_T	VCC × 0.1	-	-		
Input voltage (except for Schmitt trigger input pin)	IIC (SMBus)*2	V_{IH}	2.2	-	-		VCC = 3.6 to 5.5 V
		V_{IH}	2.0	-	-		VCC =2.7 to 3.6 V
		V_{IL}	-	-	0.8		-
	5V-tolerant ports*3	V_{IH}	VCC × 0.8	-	5.8		
		V_{IL}	-	-	VCC × 0.2		
	P000 to P004 P010 to P015	V_{IH}	AVCC0 × 0.8	-	-		
		V_{IL}	-	-	AVCC0 × 0.2		
	EXTAL Input ports pins except for P000 to P004, P010 to P015	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		

Note 1. SCL0_A, SDA0_A, SDA0_B, SCL1_A, SDA1_A (total 5 pins)
Note 2. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL1_A, SDA1_A, SCL1_B, SDA1_B (total 8 pins)
Note 3. P205, P206, P400, P401, P407 (total 5pins)

Table 2.9 I/O V_{OH}, V_{OL} (3)
Conditions: VCC = AVCC0 = 1.6 to 2.7 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P004 P010 to P015	Low drive	V_{OH}	AVCC0 – 0.3	-	-		I_{OH} = –0.5 mA
			V_{OL}	-	-	0.3		I_{OL} = 0.5 mA
		Middle drive	V_{OH}	AVCC0 – 0.3	-	-		I_{OH} = –1.0 mA
			V_{OL}	-	-	0.3		I_{OL} = 1.0 mA
	Other output pins*1	Low drive	V_{OH}	VCC – 0.3	-	-	V	I_{OH} = –0.5 mA
			V_{OL}	-	-	0.3		I_{OL} = 0.5 mA
		Middle drive*2	V_{OH}	VCC – 0.3	-	-		I_{OH} = –1.0 mA
			V_{OL}	-	-	0.3		I_{OL} = 1.0 mA

Note 1. Except for Ports P200, P214, P215, which are input ports.
Note 2. Except for P212, P213.

Table 2.10 I/O other characteristics
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES, Ports P200, P214, P215	$\lvert I_{in} \rvert$	-	-	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5V-tolerant ports	$\lvert I_{TSI} \rvert$	-	-	1.0	µA	V_{in} = 0 V V_{in} = 5.8 V
	Other ports		-	-	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up resistor	All ports (except for P200, P214, P215)	R_U	10	20	50	kΩ	V_{in} = 0 V
Input capacitance	USB_DP, USB_DM, P200	C_{in}	-	-	30	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	Other input pins		-	-	15		

2.2.5 I/O Pin Output Characteristics of Low Drive Capacity

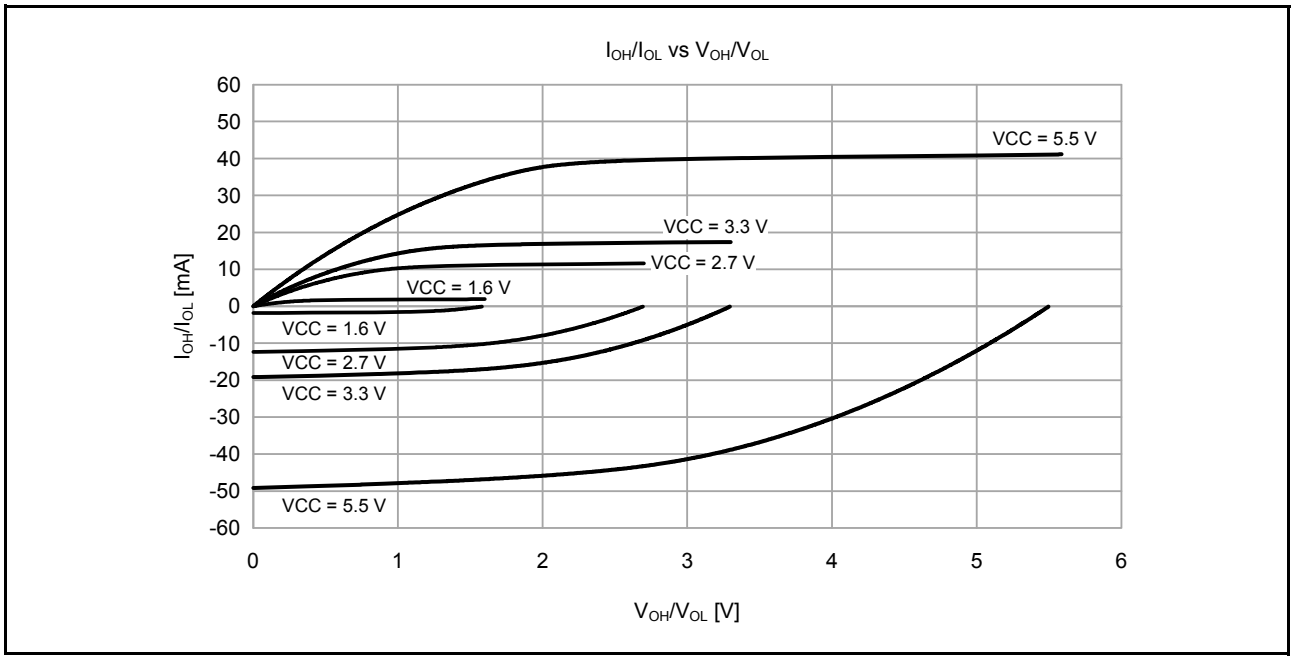


Figure 2.2 **V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C when low drive output is selected (reference data)**

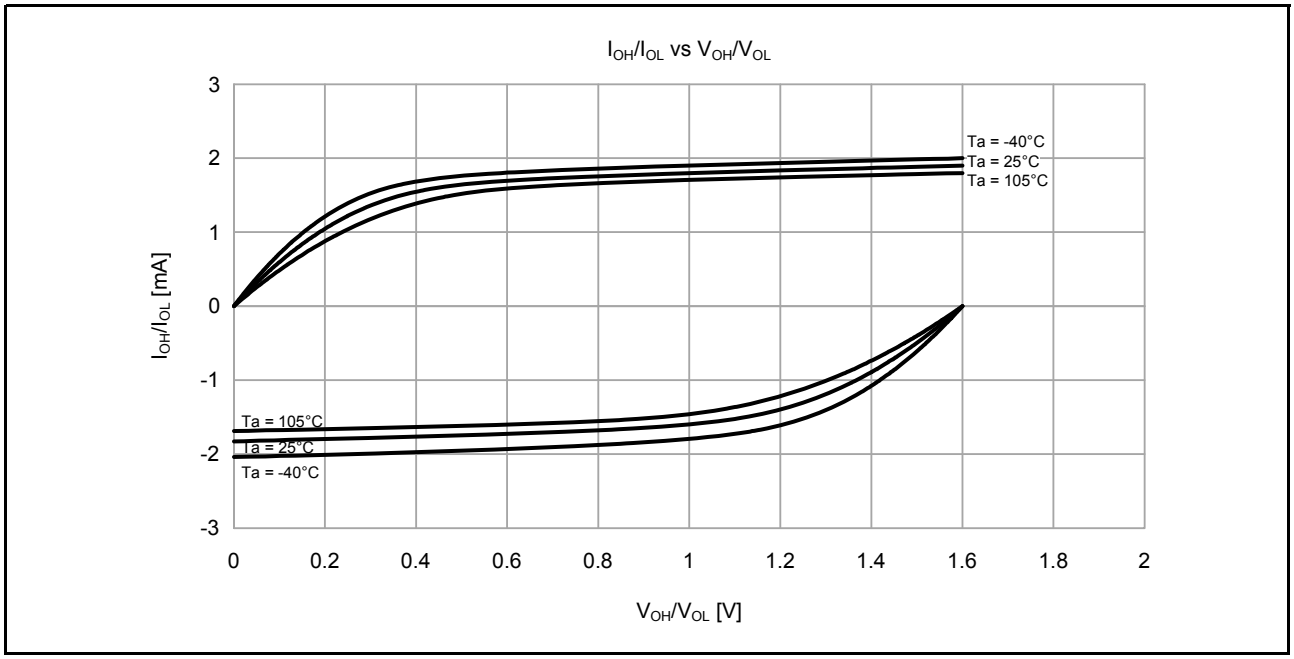
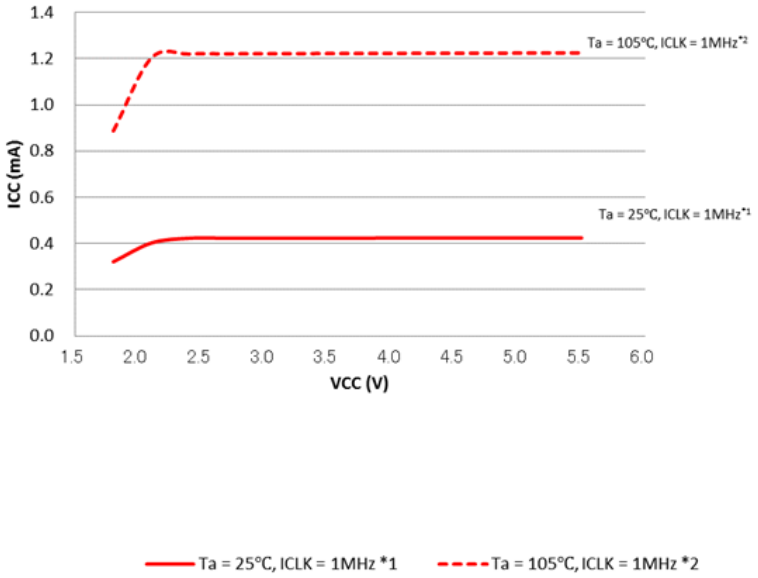


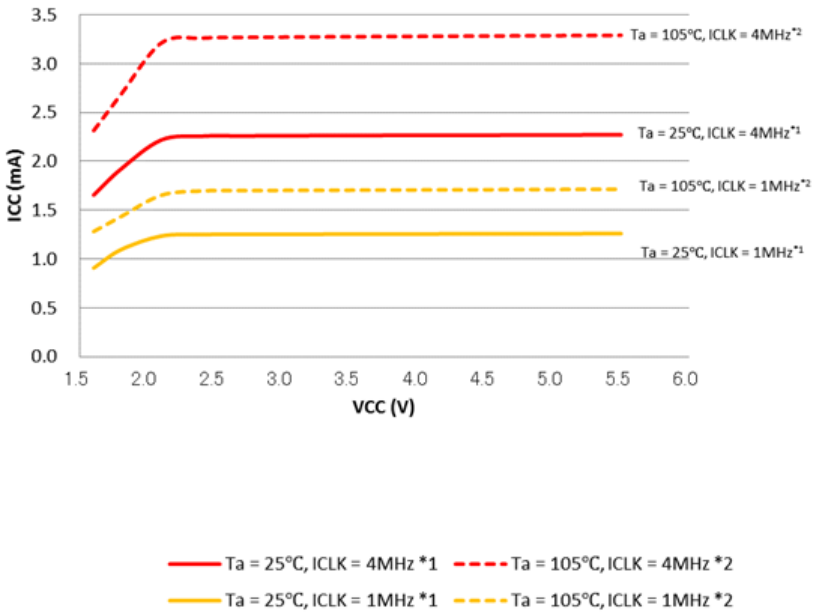
Figure 2.3 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 1.6 V when low drive output is selected (reference data)**



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.

Figure 2.19 Voltage dependency in low-speed operating mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.

Figure 2.20 Voltage dependency in low-voltage operating mode (reference data)

Table 2.18 Operation frequency in low-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1, *2, *4	1.8 to 5.5 V	f	0.032768	-	1	MHz
	Peripheral module clock (PCLKB)*4	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKD)*3, *4	1.8 to 5.5 V		-	-	1	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory.
Note 2. The frequency accuracy of ICLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.
Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 2.21, Clock timing.

Table 2.19 Operation frequency in low-voltage mode

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1, *2, *4	1.6 to 5.5 V	f	0.032768	-	4	MHz
	Peripheral module clock (PCLKB)*4	1.6 to 5.5 V		-	-	4	
	Peripheral module clock (PCLKD)*3, *4	1.6 to 5.5 V		-	-	4	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 2.21, Clock timing.

Table 2.20 Operation frequency in Subosc-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*1, *3	1.8 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	Peripheral module clock (PCLKB)*3	1.8 to 5.5 V		-	-	37.6832	
	Peripheral module clock (PCLKD)*2, *3	1.8 to 5.5 V		-	-	37.6832	

Note 1. Programming and erasing the flash memory is not possible.
Note 2. The 14-bit A/D converter cannot be used.
Note 3. See section 8, Clock Generation Circuit in User's Manual for the relationship between ICLK, PCLKB, and PCLKD frequencies.

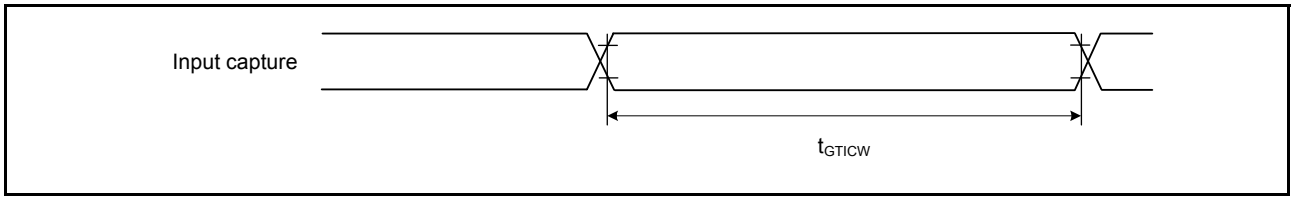


Figure 2.37 GPT input capture timing

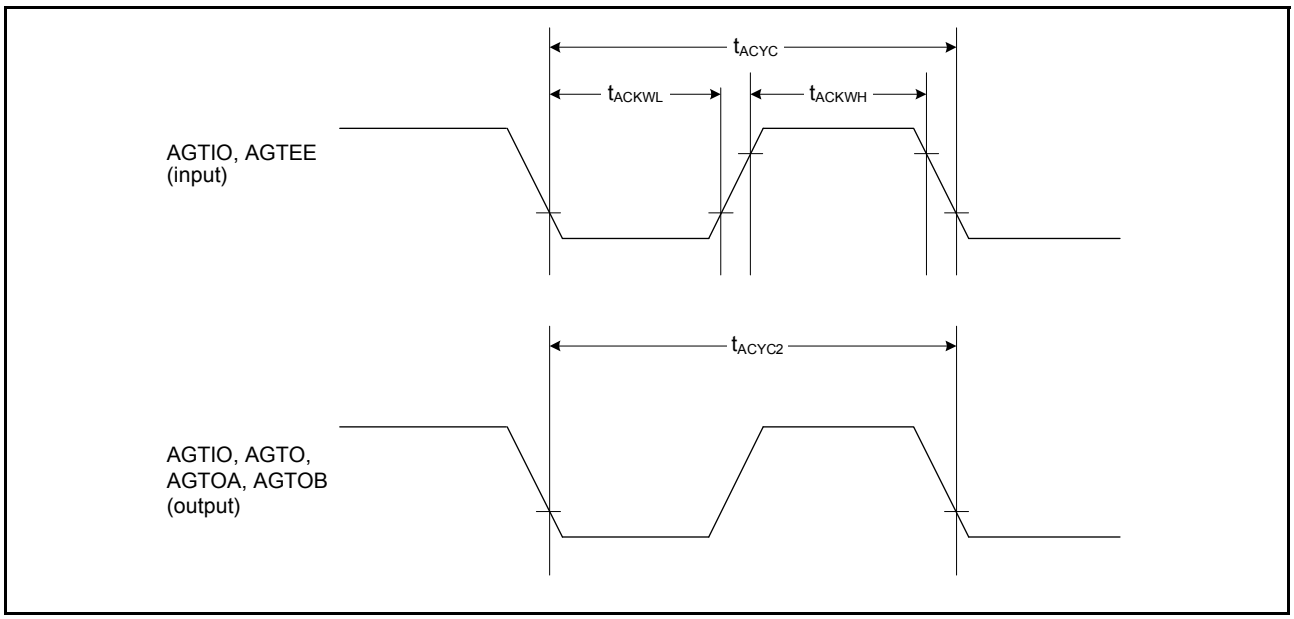


Figure 2.38 AGT I/O timing

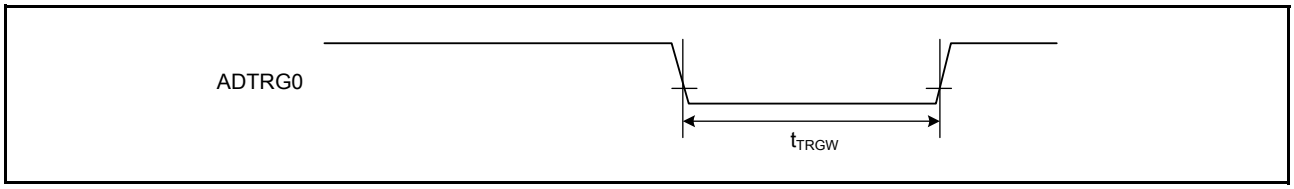


Figure 2.39 ADC14 trigger input timing

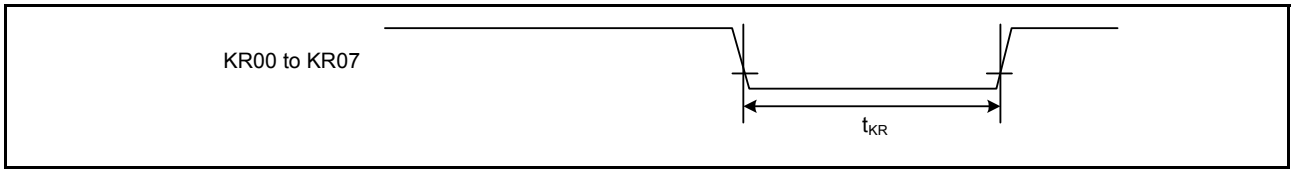


Figure 2.40 Key interrupt input timing

2.3.7 CAC Timing

Table 2.31 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq tcac$*2	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	-	-	ns	-
		$t_{PBcyc} > tcac$*2		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	-	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.

Note 2. t_{cac}: CAC count clock source cycle.

2.3.8 SCI Timing

Table 2.32 SCI timing (1)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SCI	Input clock cycle	Asynchronous		t_{Scyc}	4	-	t_{Pcyc}	Figure 2.41
		Clock synchronous			6	-		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	-	20	ns	
	Input clock fall time			t_{SCKf}	-	20	ns	
	Output clock cycle	Asynchronous		t_{Scyc}	6	-	t_{Pcyc}	
		Clock synchronous			4	-		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		1.8V or above	t_{SCKr}	-	20	ns	
			1.6V or above		-	30		
	Output clock fall time		1.8V or above	t_{SCKf}	-	20	ns	
			1.6V or above		-	30		
	Transmit data delay (master)	Clock synchronous	1.8V or above	t_{TXD}	-	40	ns	Figure 2.42
			1.6V or above		-	45		
	Transmit data delay (slave)	Clock synchronous	2.7V or above		-	55	ns	
			2.4V or above		-	60		
			1.8V or above		-	100		
			1.6V or above		-	125		
	Receive data setup time (master)	Clock synchronous	2.7V or above	t_{RXS}	45	-	ns	
			2.4V or above		55	-		
			1.8V or above		90	-		
			1.6V or above		110	-		
	Receive data setup time (slave)	Clock synchronous	2.7V or above		40	-	ns	
			1.6V or above		45	-		
	Receive data hold time (master)	Clock synchronous		t_{RXH}	5	-	ns	
	Receive data hold time (slave)	Clock synchronous		t_{RXH}	40	-	ns	

Note 1. t_{Pcyc}: PCLKB cycle.

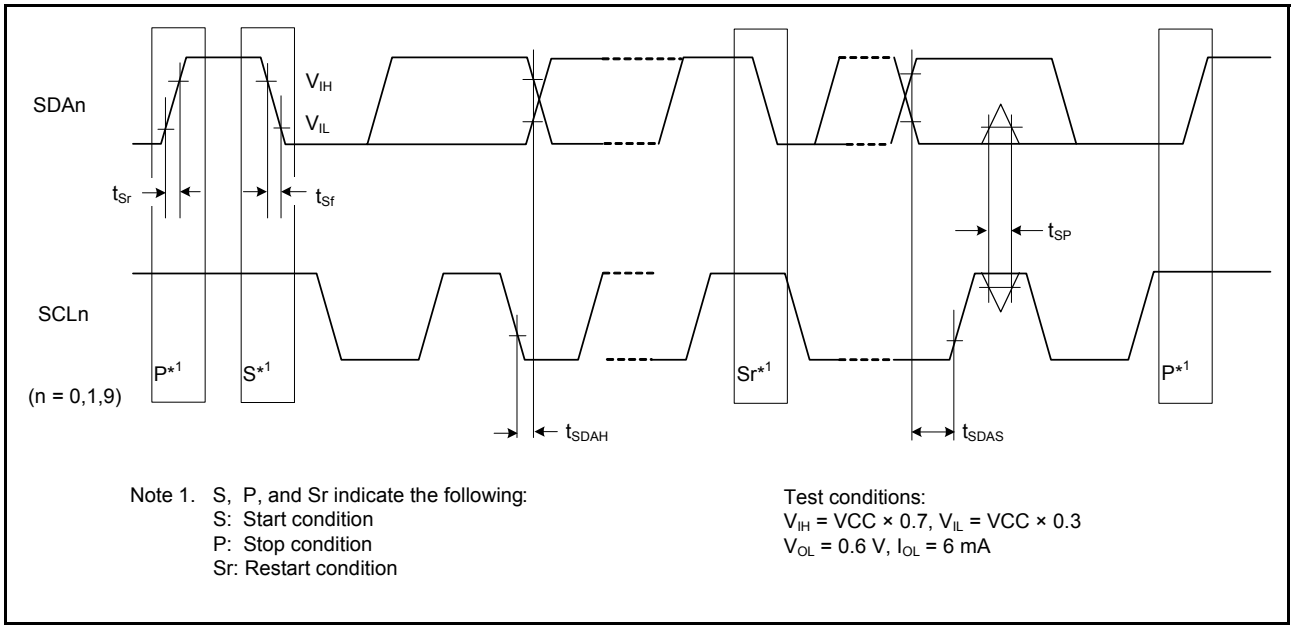


Figure 2.48 SCI simple IIC mode timing

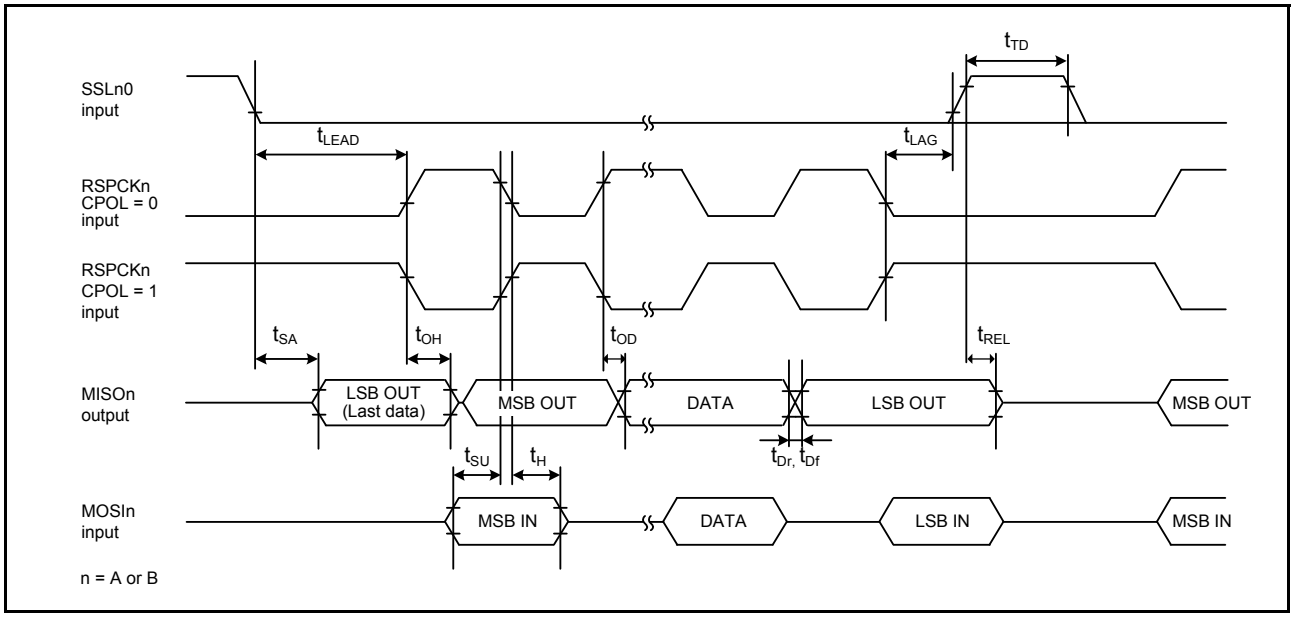


Figure 2.55 SPI timing (slave, CPHA = 1)

2.3.11 CLKOUT Timing

Table 2.37 CLKOUT timing

Parameter			Symbol	Min	Max	Unit*1	Test conditions
CLKOUT	CLKOUT pin output cycle*1	VCC = 2.7 V or above	t_{Ccyc}	62.5	-	ns	Figure 2.57
		VCC = 1.8 V or above		125	-		
		VCC = 1.6 V or above		250	-		
	CLKOUT pin high pulse width*2	VCC = 2.7 V or above	t_{CH}	15	-	ns	
		VCC = 1.8 V or above		30	-		
		VCC = 1.6 V or above		150	-		
	CLKOUT pin low pulse width*2	VCC = 2.7 V or above	t_{CL}	15	-	ns	
		VCC = 1.8 V or above		30	-		
		VCC = 1.6 V or above		150	-		
	CLKOUT pin output rise time	VCC = 2.7 V or above	t_{Cr}	-	12	ns	
		VCC = 1.8 V or above		-	25		
		VCC = 1.6 V or above		-	50		
	CLKOUT pin output fall time	VCC = 2.7 V or above	t_{Cf}	-	12	ns	
		VCC = 1.8 V or above		-	25		
		VCC = 1.6 V or above		-	50		

Note 1. When the EXTAL external clock input or an oscillator is used with division by 1 (the CKOCR.CKOSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

Note 2. When the MOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 001b), set the clock output division ratio selection to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).

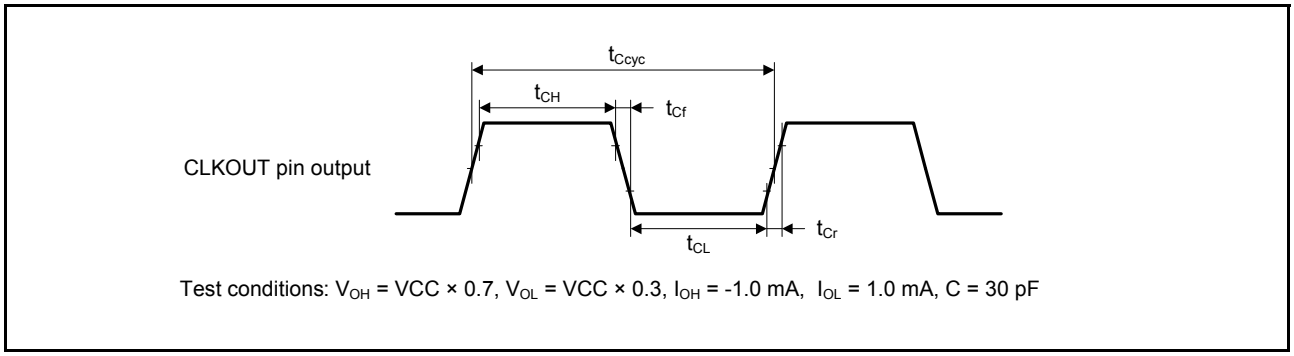


Figure 2.57 CLKOUT output timing

Table 2.40 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Conversion time*1 (Operation at PCLKD = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.80	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.22	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4, I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.

Table 2.41 A/D conversion characteristics (2) in high-speed A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	48	MHz	-
Analog input capacitance*2	Cs	-	-	8*3	pF	High-precision channel
		-	-	9*3	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5*3	kΩ	High-precision channel
		-	-	6.7*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.94	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.50	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-

Table 2.53 Power-on reset circuit and voltage detection circuit characteristics (2) (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Power-on reset enable time	$t_{W\ (POR)}$	1	-	-	ms	Figure 2.67, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)	$T_{d\ (E-A)}$	-	-	300	µs	Figure 2.69, Figure 2.70
Hysteresis width (POR)	V_{PORH}	-	110	-	mV	-
Hysteresis width (LVD0, LVD1, and LVD2)	V_{LVH}	-	60	-	mV	LVD0 selected
		-	100	-		V_{det1_0} to V_{det1_2} selected.
		-	60	-		V_{det1_3} to V_{det1_9} selected.
		-	50	-		V_{det1_A} to V_{det1_B} selected.
		-	40	-		V_{det1_C} to V_{det1_F} selected.
		-	60	-		LVD2 selected

Note 1. When OFS1.LVDAS = 0
Note 2. When OFS1.LVDAS = 1
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

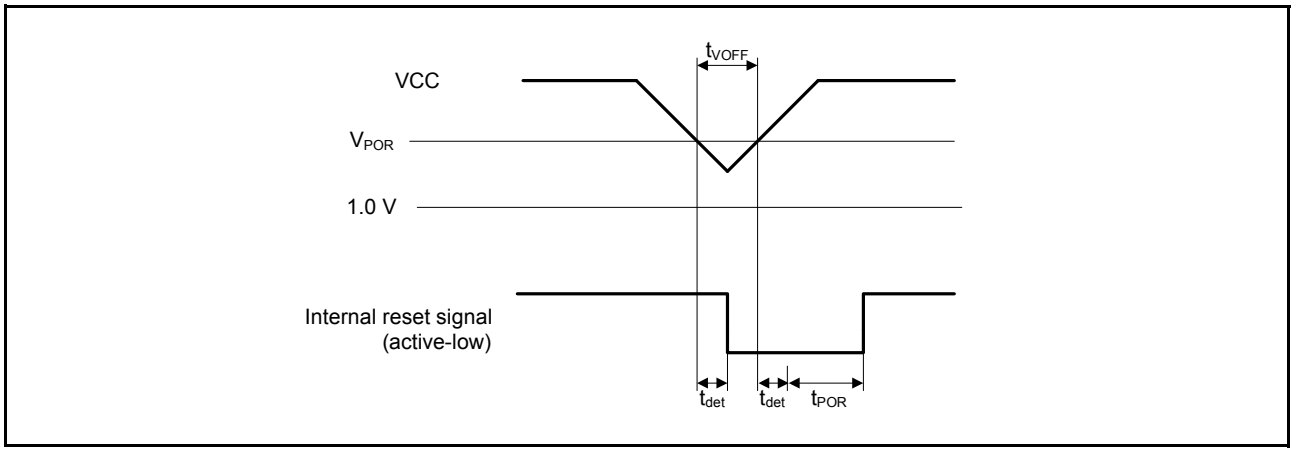
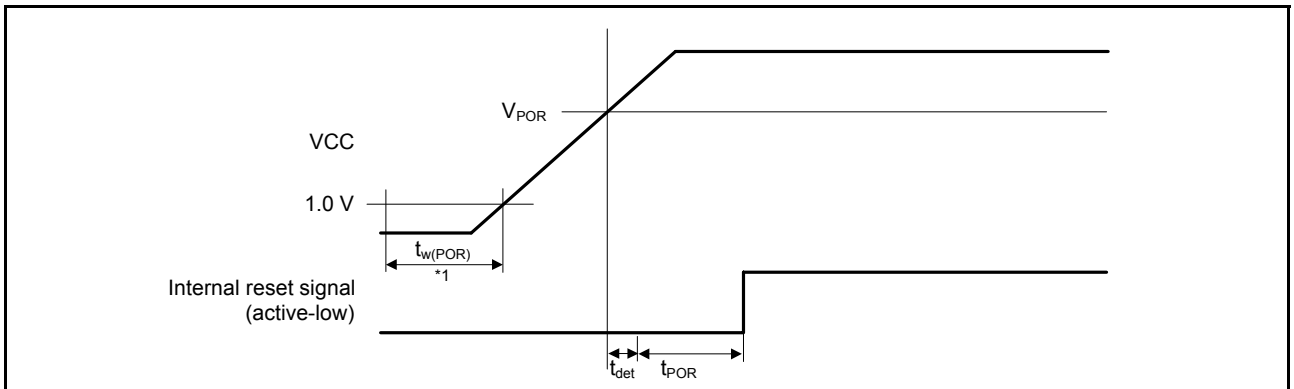


Figure 2.66 Voltage detection reset timing



Note: $t_{W(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{W(POR)}$ for 1.0 ms or more.

Figure 2.67 Power-on reset timing

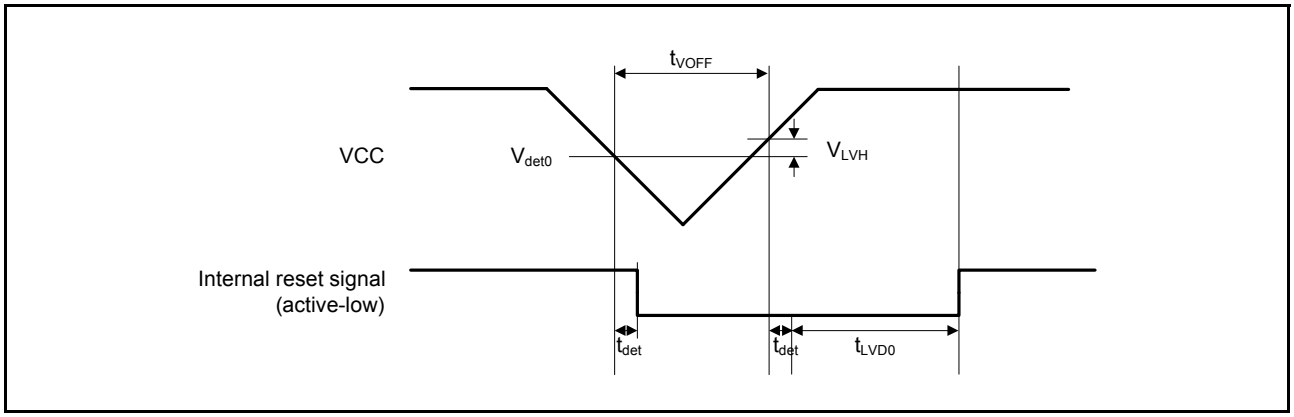


Figure 2.68 Voltage detection circuit timing (V_{det0})

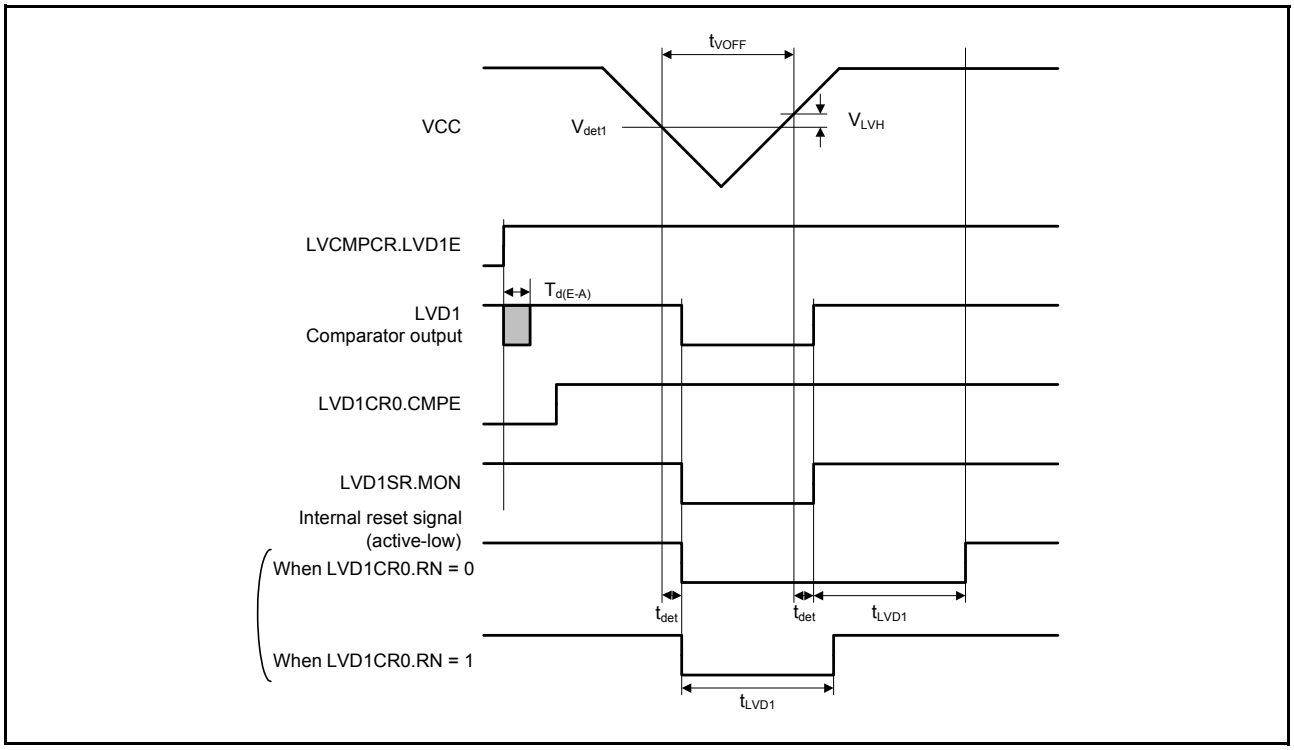


Figure 2.69 Voltage detection circuit timing (V_{det1})

Table 2.58 Code flash characteristics (3)

Middle-speed operating mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V, Ta = -40 to +85°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 8 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{P4}	-	157	1411	-	101	966	µs
Erasure time	1-KB	t_{E1K}	-	9.10	289	-	6.10	228	ms
Blank check time	2-byte	t_{BC4}	-	-	87.7	-	-	52.5	µs
	1-KB	t_{BC1K}	-	-	1930	-	-	414	µs
Erase suspended time		t_{SED}	-	-	32.7	-	-	21.6	µs
Startup area switching setting time		t_{SAS}	-	22.8	592	-	14.2	465	ms
Access window time		t_{AWS}	-	22.8	592	-	14.2	465	ms
OCD/serial programmer ID setting time		t_{OSIS}	-	22.8	592	-	14.2	465	ms
Flash memory mode transition wait time 1		t_{DIS}	2	-	-	2	-	-	µs
Flash memory mode transition wait time 2		t_{MS}	720	-	-	720	-	-	ns

Note 1. Does not include the time until each operation of the flash memory is started after instructions are executed by the software.

Note 2. The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 3. The frequency accuracy of ICLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

2.12.2 Data Flash Memory Characteristics

Table 2.59 Data flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	-	Times	-
Data hold time	After 10000 times of N_{DPEC}	t_{DDRP}	20*2, *3	-	-	Year	Ta = +85°C
	After 100000 times of N_{DPEC}		5*2, *3	-	-	Year	
	After 1000000 times of N_{DPEC}		-	1*2, *3	-	Year	Ta = +25°C

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,000 times for different addresses in 1-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as 1. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited.)

Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

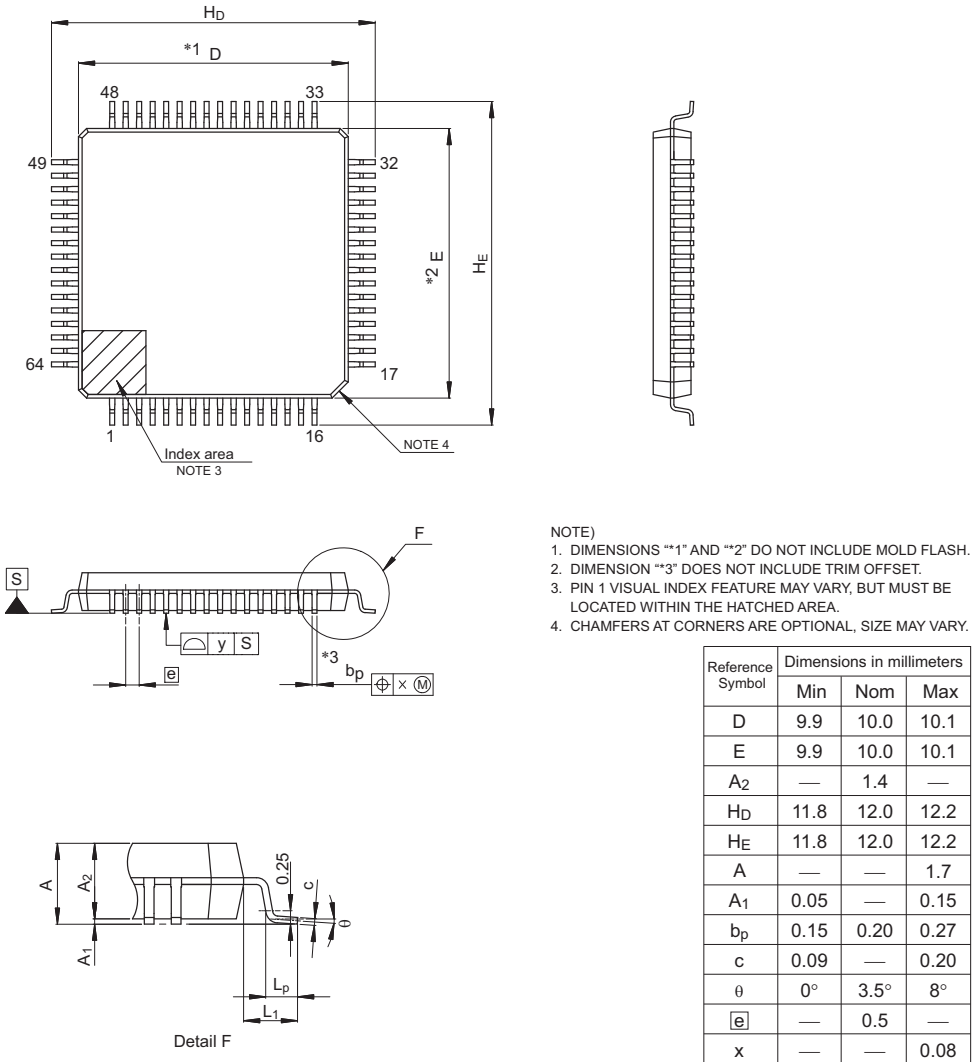
Note 3. These results are obtained from reliability testing.

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm

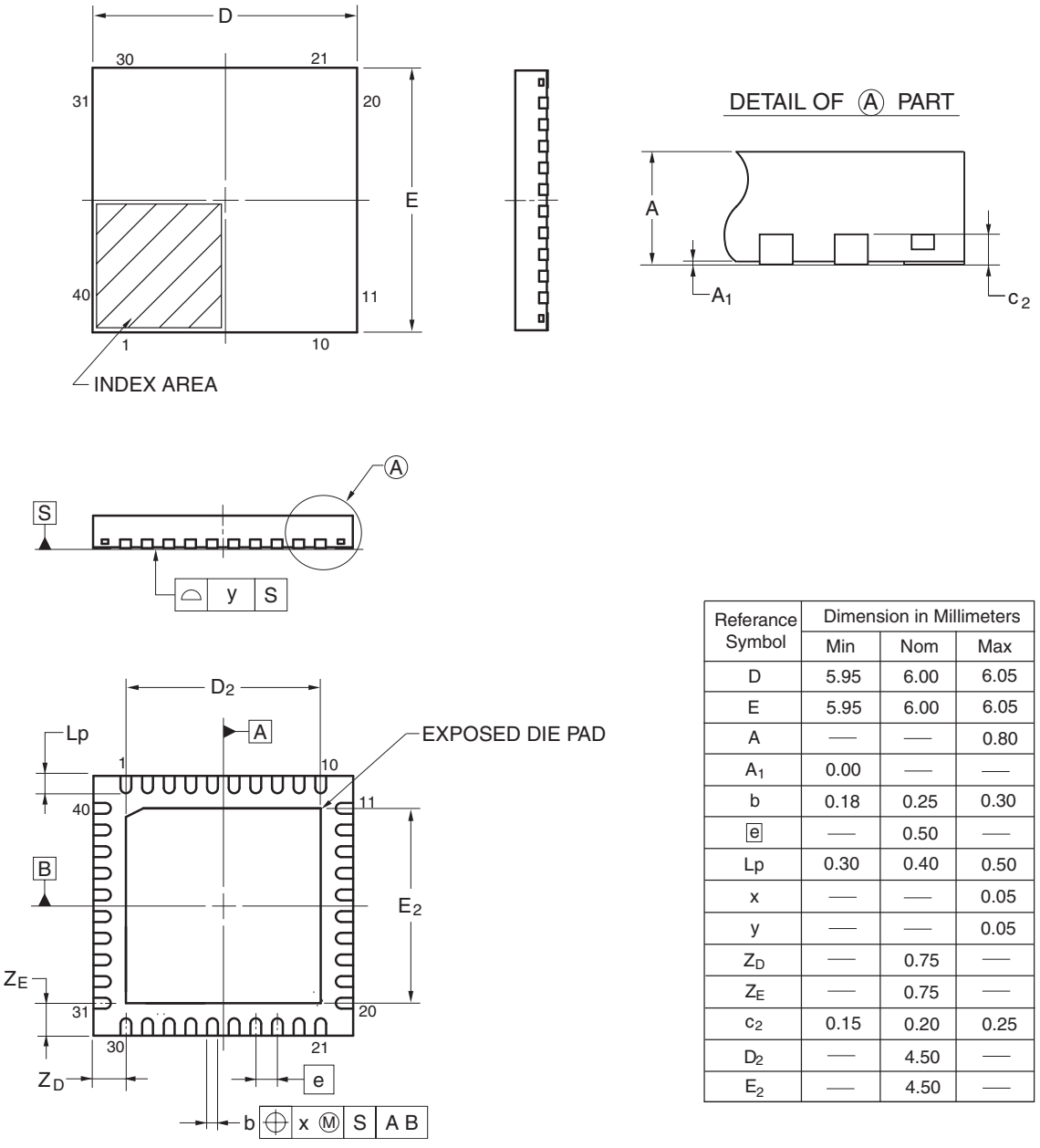


NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 1.1 LQFP 64-pin

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-5	0.09



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	5.95	6.00	6.05
E	5.95	6.00	6.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	4.50	—
E_2	—	4.50	—

Figure 1.6 QFN 40-pin

Revision History	S124 Microcontroller Group Datasheet

Rev.	Date	Summary
1.00	May 19, 2016	1st release
1.01	Oct 3, 2016	2nd release
1.30	Feb 5, 2018	3rd release