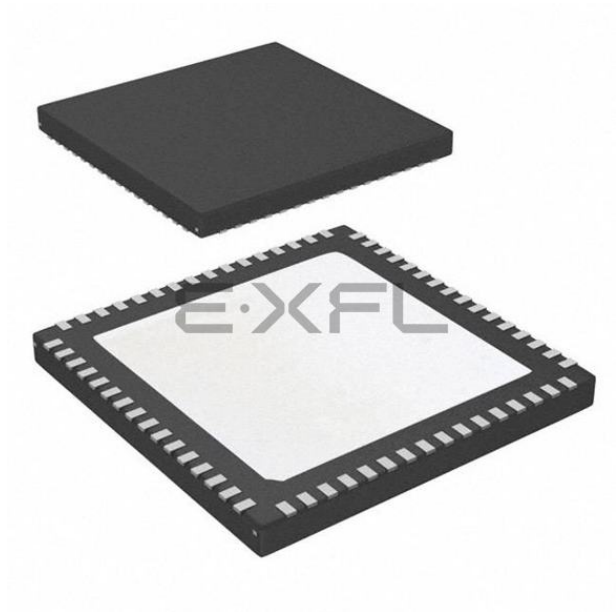
Renesas Electronics America Inc - R7FS124773A01CNB#AC1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 18x14b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	64-HWQFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs124773a01cnb-ac1

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit MCUs that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

Based on the energy-efficient Arm Cortex®-M0+ core, the MCU is particularly well suited for cost-sensitive and low-power applications with the following features:

- 128-KB code flash memory
- 16-KB SRAM
- Capacitive Touch Sensing Unit (CTSU)
- 14-bit A/D Converter (ADC14)
- 12-bit D/A Converter (DAC12)
- Security features.

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M0+	• Maximum operating frequency: up to 32 MHz • Arm Cortex-M0+: - Revision: r0p1-00rel0 - Armv6-M architecture profile - Single-cycle integer multiplier. • SysTick timer - Driven by SYSTICCLK (LOCO) or ICLK.

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 128 KB code flash memory. See section 37, Flash Memory in User's Manual.
Data flash memory	4 KB data flash memory. See section 37, Flash Memory in User's Manual.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 6, Option-Setting Memory in User's Manual.
SRAM	On-chip high-speed SRAM with even parity bit. See section 36, SRAM in User's Manual.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating mode	Two operating modes: • Single-chip mode • SCI boot mode. See section 3, Operating Modes in User's Manual.
Reset	9 types of resets: • RES pin reset • Power-on reset • Independent watchdog timer reset • Watchdog timer reset • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset • SRAM parity error reset • Software reset. See section 5, Resets in User's Manual.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) monitors the voltage level input to the VCC pin and the detection level can be selected using a software program. See section 7, Low Voltage Detection (LVD) in User's Manual.

Table 1.3 System (2 of 2)

Feature	Functional description
Clock	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • Independent watchdog timer on-chip oscillator • Clock out support. See section 8, Clock Generation Circuit in User's Manual.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) is used to check the system clock frequency with a reference clock signal by counting the number of pulses of the system clock to be measured. The reference clock can be provided externally through a CACREF pin or internally from various on-chip oscillators. Event signals can be generated when the clock does not match or measurement ends. This feature is particularly useful in implementing a fail-safe mechanism for home and industrial automation applications. See section 9, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 12, Interrupt Controller Unit (ICU) in User's Manual.
Key interrupt function (KINT)	A key interrupt can be generated by setting the Key Return Mode register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 17, Key Interrupt Function (KINT) in User's Manual.
Low Power Mode	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 10, Low Power Modes in User's Manual.
Register Write Protection	The Register Write Protection function protects important registers from being overwritten due to software errors. See section 11, Register Write Protection in User's Manual.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down-counter. It can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. The refresh-permitted period can be set to refresh the counter and used as the condition to detect when the system runs out of control. See section 22, Watchdog Timer (WDT) in User's Manual.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt/interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail safe mechanism when the system runs out of control. The watchdog timer can be triggered automatically on reset, underflow, or refresh error, or by a refresh of the count value in the registers. See section 23, Independent Watchdog Timer (IWDT) in User's Manual.

Table 1.4 Event Link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 15, Event Link Controller (ELC) in User's Manual.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	The MCU incorporates a Data Transfer Controller (DTC) that performs data transfers when activated by an interrupt request. See section 14, Data Transfer Controller (DTC) in User's Manual.

Table 1.14 Pin functions (2 of 3)

Function	Signal	I/O	Description
SCI	SCK0, SCK1, SCK9	I/O	Input/output pins for the clock (clock synchronous mode).
	RXD0, RXD1, RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode).
	TXD0, TXD1, TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode).
	CTS0_RTS0, CTS1_RTS1, CTS9_RTS9	I/O	Input/Output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	SCL0, SCL1, SCL9	I/O	Input/output pins for the IIC clock (simple IIC).
	SDA0, SDA1, SDA9	I/O	Input/output pins for the IIC data (simple IIC).
	SCK0, SCK1, SCK9	I/O	Input/output pins for the clock (simple SPI).
	MISO0, MISO1, MISO9	I/O	Input/output pins for slave transmission of data (simple SPI).
	MOSI0, MOSI1, MOSI9	I/O	Input/output pins for master transmission of data (simple SPI).
	SS0, SS1, SS9	Input	Chip-select input pins (simple SPI), active-low.
IIC	SCL0, SCL1	I/O	Input/output pins for clock.
	SDA0, SDA1	I/O	Input/output pins for data.
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin.
	MOSIA, MOSIB	I/O	Inputs or outputs data output from the master.
	MISOA, MISOB	I/O	Inputs or outputs data output from the slave.
	SSLA0, SSLB0	I/O	Input or output pin for slave selection.
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pin for slave selection.
CAN	CRX0	Input	Receive data.
	CTX0	Output	Transmit data.
USBFS	VSS_USB	Input	Ground pins.
	VCC_USB_LDO	Input	Power supply pin for USB LDO regulator.
	VCC_USB	I/O	Input: Power supply pin for USB transceiver. Output: USB LDO regulator output pin. This pin should be connected to an external capacitor.
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus.
	USB_DM	I/O	D– I/O pin of the USB on-chip transceiver. This pin should be connected to the D– pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. This pin should be connected to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller.
Analog power supply	AVCC0	Input	Analog block power supply pin
	AVSS0	Input	Analog block power supply ground pin
	VREFH0	Input	Reference power supply pin
	VREFL0	Input	Reference power supply ground pin
ADC14	AN000 to AN010, AN016 to AN022	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active-low.
DAC12	DA0	Output	Output pins for the analog signals to be processed by the D/A converter.

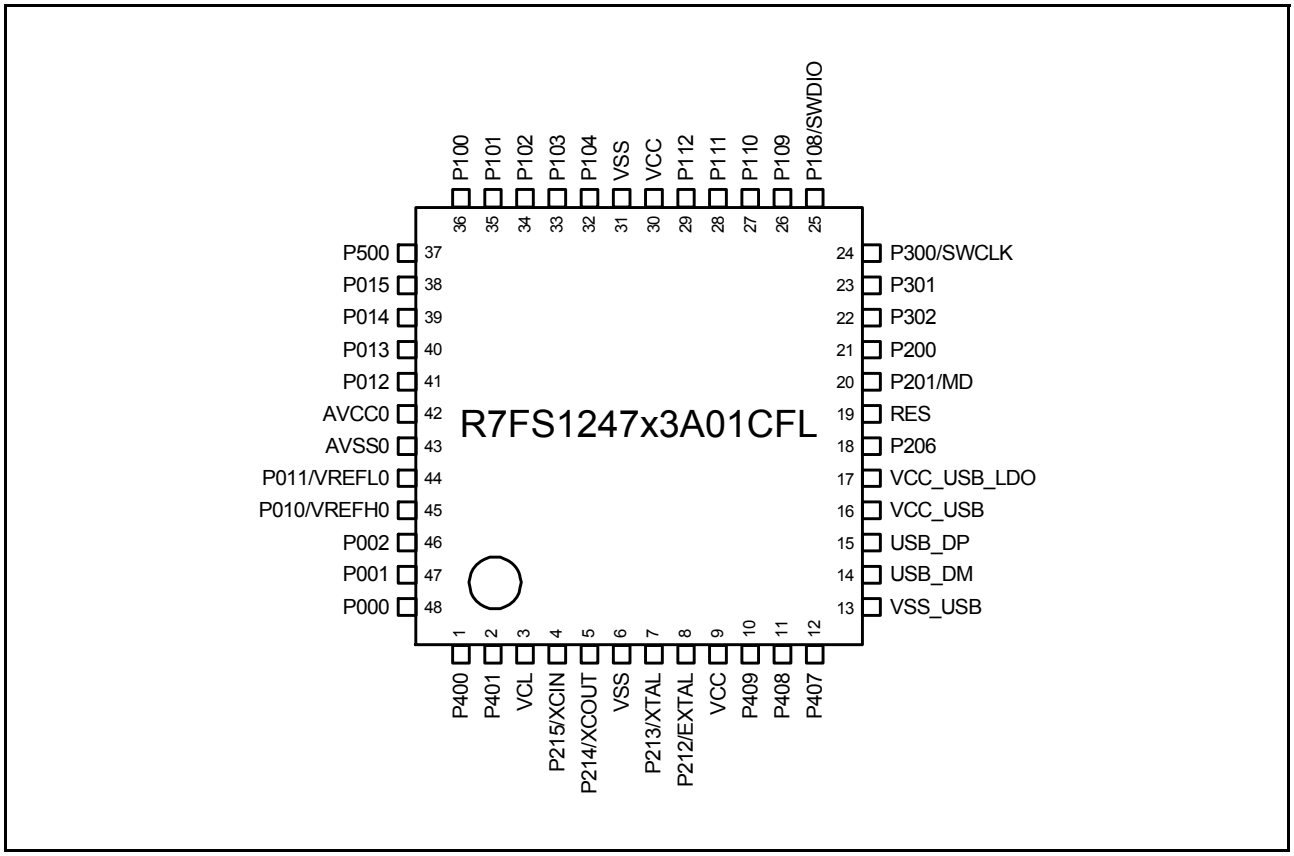


Figure 1.5 Pin assignment for LQFP 48-pin (top view)

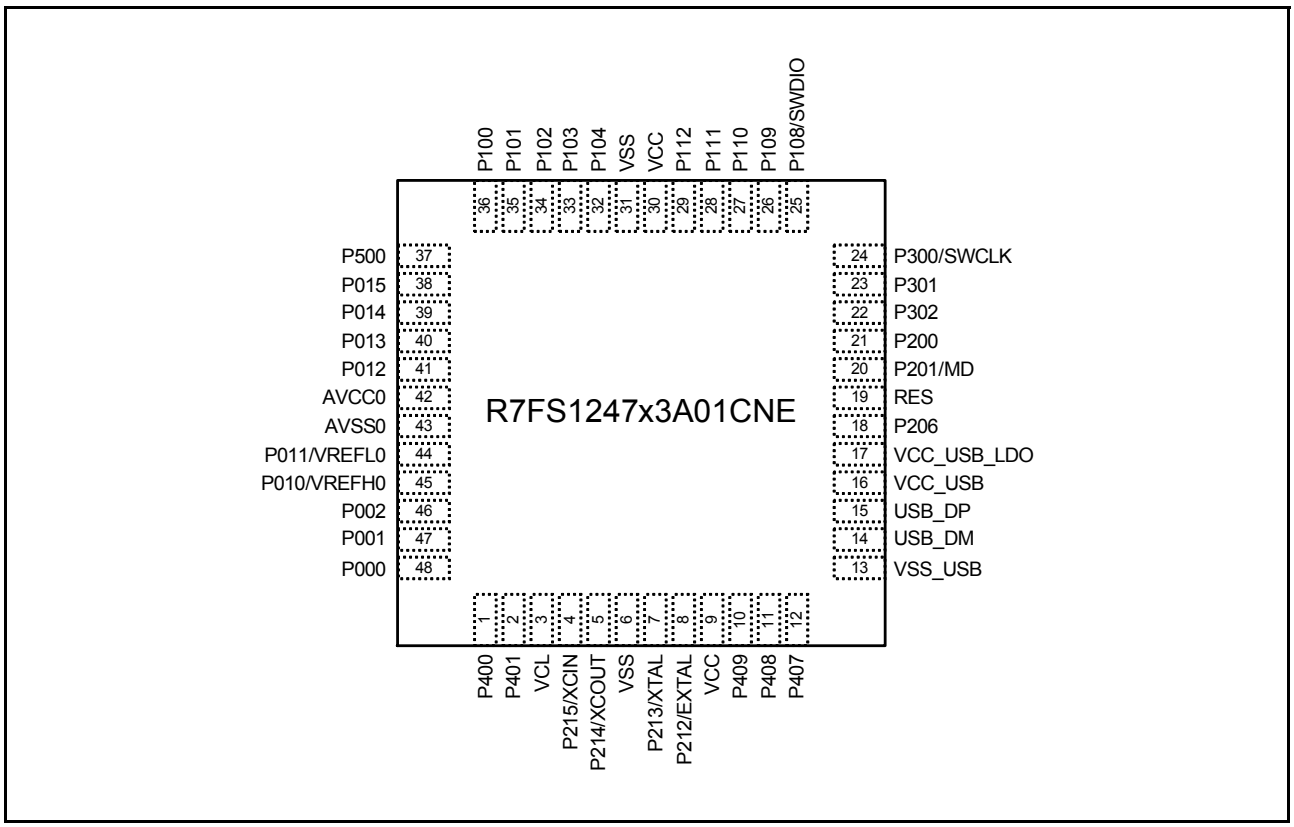


Figure 1.6 Pin assignment for QFN 48-pin (top view)

Table 2.5 I/O V_{IH}, V_{IL} (2)
Conditions: VCC = AVCC0 = 1.6 to 2.7 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	RES, NMI Peripheral input pins	V_{IH}	VCC × 0.8	-	-	V	-
		V_{IL}	-	-	VCC × 0.2		
		ΔV_T	VCC × 0.01	-	-		
Input voltage (except for Schmitt trigger input pin)	5V-tolerant ports*1	V_{IH}	VCC × 0.8	-	5.8		
		V_{IL}	-	-	VCC × 0.2		
	P000 to P004 P010 to P015	V_{IH}	AVCC0 × 0.8	-	-		
		V_{IL}	-	-	AVCC0 × 0.2		
	EXTAL Input ports pins except for P000 to P004, P010 to P015	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		

Note 1. P205, P206, P400, P401, P407 (total 5pins)

2.2.3 I/O I_{OH}, I_{OL}

Table 2.6 I/O I_{OH}, I_{OL}
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P000 to P004, P010 to P015, P212, P213	-	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P408, P409	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2 VCC = 2.7 to 3.0 V	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 VCC = 3.0 to 5.5 V	I_{OH}	-	-	–20.0	mA
			I_{OL}	-	-	20.0	mA
	Other output pins*3	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
Permissible output current (max value per pin)	Ports P000 to P004, P010 to P015, P212, P213	-	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P408, P409	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2 VCC = 2.7 to 3.0 V	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 VCC = 3.0 to 5.5 V	I_{OH}	-	-	–20.0	mA
			I_{OL}	-	-	20.0	mA
	Other output pins*3	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
Permissible output current (max value total pins)	Total of ports P000 to P004, P010 to P015		$\Sigma I_{OH\ (max)}$	-	-	–30	mA
			$\Sigma I_{OL\ (max)}$	-	-	30	mA
	Total of all output pin		$\Sigma I_{OH\ (max)}$	-	-	–60	mA
			$\Sigma I_{OL\ (max)}$	-	-	60	mA

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

Note 1. This is the value when low driving ability is selected with the Port Drive Capability bit in the PmnPFS register.

Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the register.

Note 3. Except for Ports P200, P214, P215, which are input ports.

2.2.5 I/O Pin Output Characteristics of Low Drive Capacity

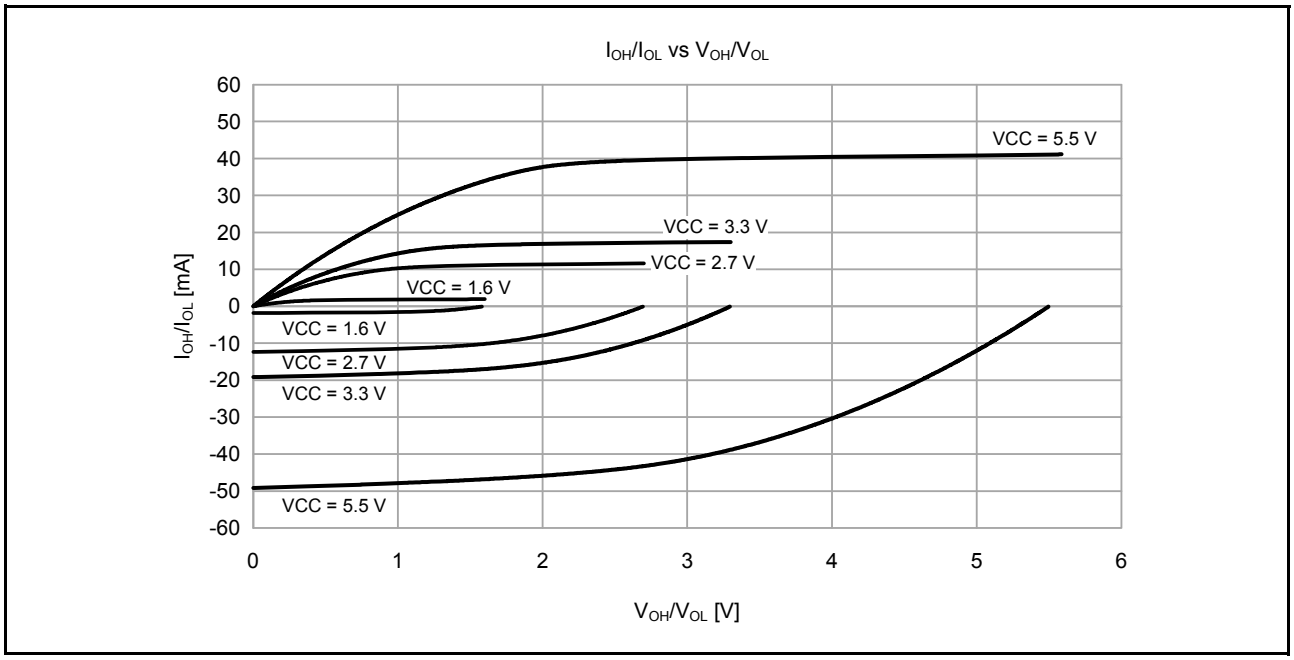


Figure 2.2 **V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C when low drive output is selected (reference data)**

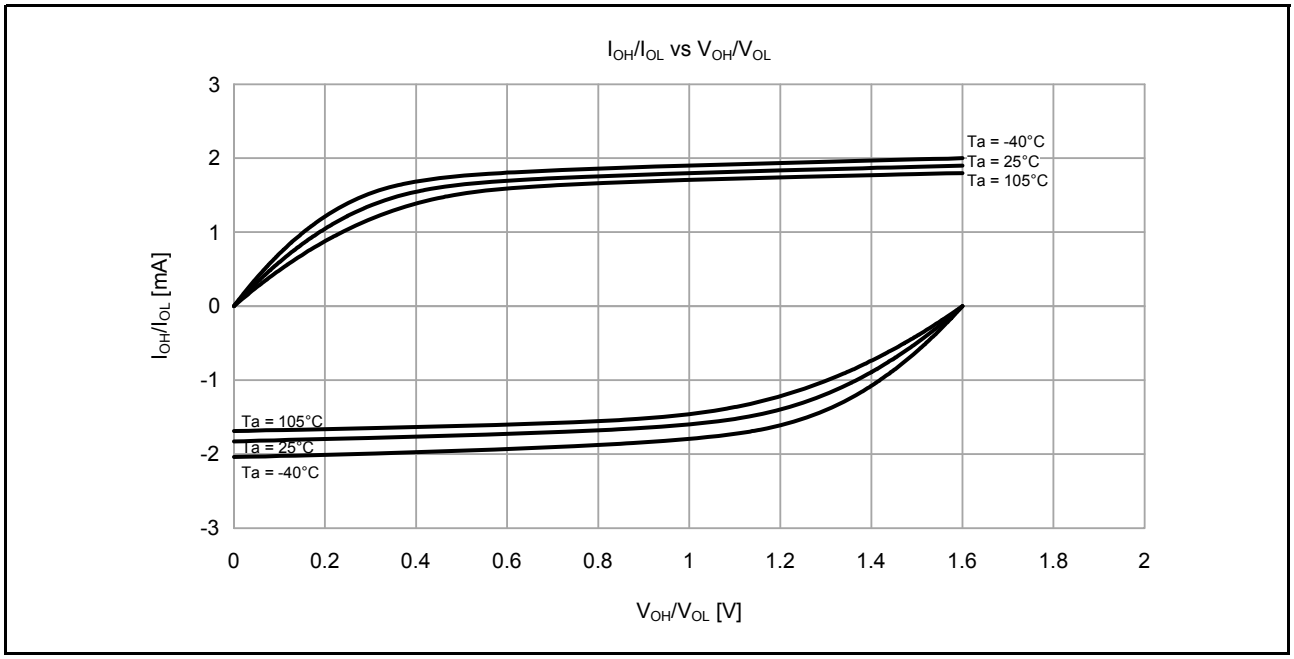


Figure 2.3 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 1.6 V when low drive output is selected (reference data)**

Table 2.13 Operating and standby current (3) (2 of 2)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Low-power analog comparator (ACMPLP) operating current	Window mode	I_{CMPLP}	-	15	-	µA	-
	Comparator high-speed mode		-	10	-	µA	-
	Comparator low-speed mode		-	2	-	µA	-
USB operating current	During USB communication under the following settings and conditions: • Function controller is in Full-Speed mode and - Bulk OUT transfer is (64 bytes) × 1 - Bulk IN transfer is (64 bytes) × 1 • Host device is connected by a 1-meter USB cable from the USB port.	I_{USBF}*2	-	3.6 (VCC) 1.1 (VCC_USB)*4	-	mA	-
	During suspended state under the following setting and conditions: • Function controller is in Full-Speed mode (the USB_DP pin is pulled up) • Software Standby mode • Host device is connected by a 1-meter USB cable from the USB port.	I_{SUSP}*3	-	0.35 (VCC) 170 (VCC_USB)*4	-	µA	-

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.
Note 2. Current is consumed only by the USBFS.
Note 3. Includes the current supplied from the pull-up resistor of the USB_DP pin to the pull-down resistor of the host device, in addition to the current consumed by the MCU in the suspended state.
Note 4. When VCC = VCC_USB = 3.3 V.
Note 5. When the MSTPCRD.MSTPD16 (ADC140 module-stop bit) is in the module-stop state.

Table 2.18 Operation frequency in low-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1, *2, *4	1.8 to 5.5 V	f	0.032768	-	1	MHz
	Peripheral module clock (PCLKB)*4	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKD)*3, *4	1.8 to 5.5 V		-	-	1	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory.
Note 2. The frequency accuracy of ICLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.
Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 2.21, Clock timing.

Table 2.19 Operation frequency in low-voltage mode

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1, *2, *4	1.6 to 5.5 V	f	0.032768	-	4	MHz
	Peripheral module clock (PCLKB)*4	1.6 to 5.5 V		-	-	4	
	Peripheral module clock (PCLKD)*3, *4	1.6 to 5.5 V		-	-	4	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 2.21, Clock timing.

Table 2.20 Operation frequency in Subosc-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*1, *3	1.8 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	Peripheral module clock (PCLKB)*3	1.8 to 5.5 V		-	-	37.6832	
	Peripheral module clock (PCLKD)*2, *3	1.8 to 5.5 V		-	-	37.6832	

Note 1. Programming and erasing the flash memory is not possible.
Note 2. The 14-bit A/D converter cannot be used.
Note 3. See section 8, Clock Generation Circuit in User's Manual for the relationship between ICLK, PCLKB, and PCLKD frequencies.

2.3.3 Reset Timing

Table 2.22 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on	t_{RESWP}	3	-	-	ms	Figure 2.29
	Not at power-on	t_{RESW}	30	-	-	μs	Figure 2.30
Wait time after RES cancellation (at power-on)	LVD0 enabled*1	t_{RESWT}	-	0.7	-	ms	Figure 2.29
	LVD0 disabled*2		-	0.3	-		
Wait time after RES cancellation (during powered-on state)	LVD0 enabled*1	t_{RESWT2}	-	0.5	-	ms	Figure 2.30
	LVD0 disabled*2		-	0.05	-		
Internal reset cancellation time (Watchdog timer reset, SRAM parity error reset, Software reset)	LVD0 enabled*1	t_{RESWT3}	-	0.6	-	ms	
	LVD0 disabled*2		-	0.15	-		

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.

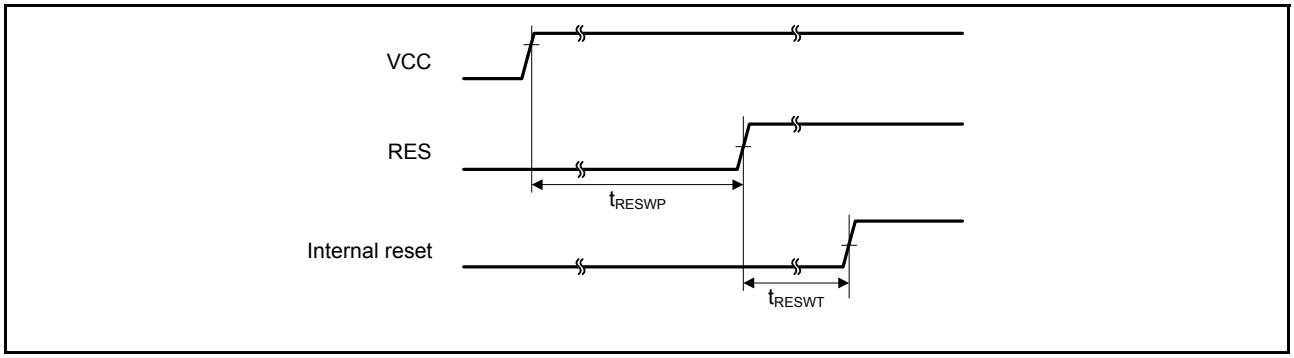


Figure 2.29 Reset input timing at power-on

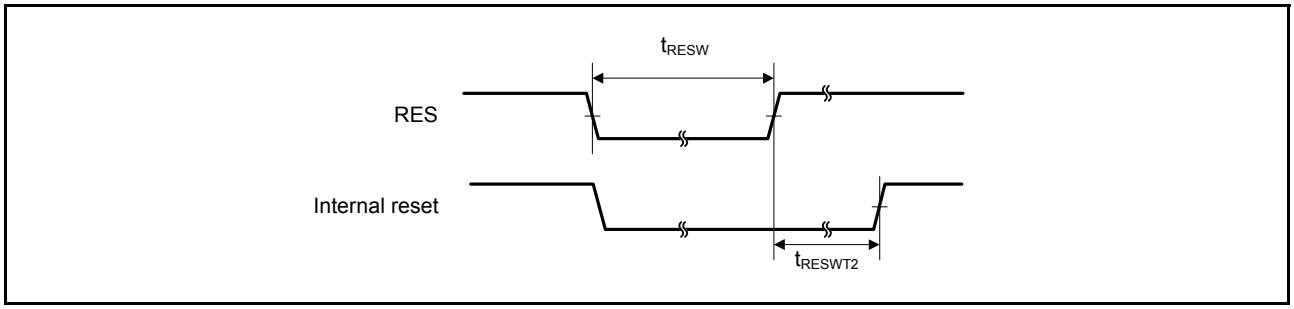


Figure 2.30 Reset input timing (1)

Table 2.25 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (1 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 2.31
		External clock input to main clock oscillator	System clock source is main clock oscillator (1 MHz)*3	t_{SBYEX}	-	28	50	µs	
		System clock source is MOCO		t_{SBYMO}	-	25	35	µs	

Note 1. The division ratio of ICK and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 2.26 Timing of recovery from low power modes (4)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-voltage mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (4 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 2.31
		External clock input to main clock oscillator	System clock source is main clock oscillator (4 MHz)*3	t_{SBYEX}	-	108	130	µs	
		System clock source is HOCO		t_{SBYHO}	-	108	130	µs	

Note 1. The division ratio of ICK and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 2.27 Timing of recovery from low power modes (5)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	SubOSC-speed mode	System clock source is sub-clock oscillator (32.768 kHz)	t_{SBYSC}	-	0.85	1	ms	Figure 2.31
		System clock source is LOCO (32.768 kHz)	t_{SBYLO}	-	0.85	1.2	ms	

Note 1. The sub-clock oscillator or LOCO itself continues oscillating in Software Standby mode during Subosc-speed mode.

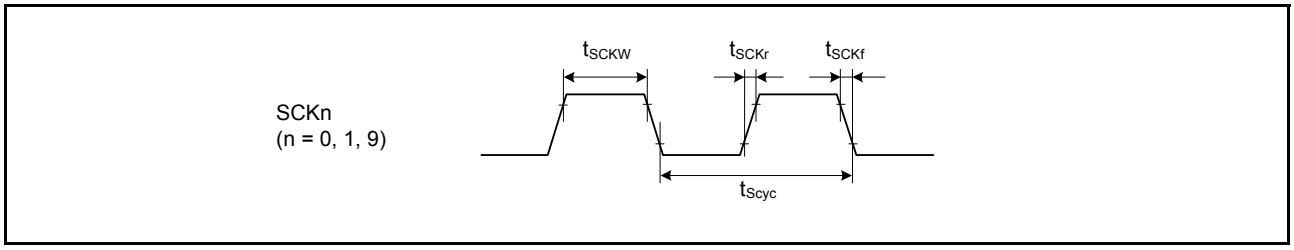


Figure 2.41 SCK clock input timing

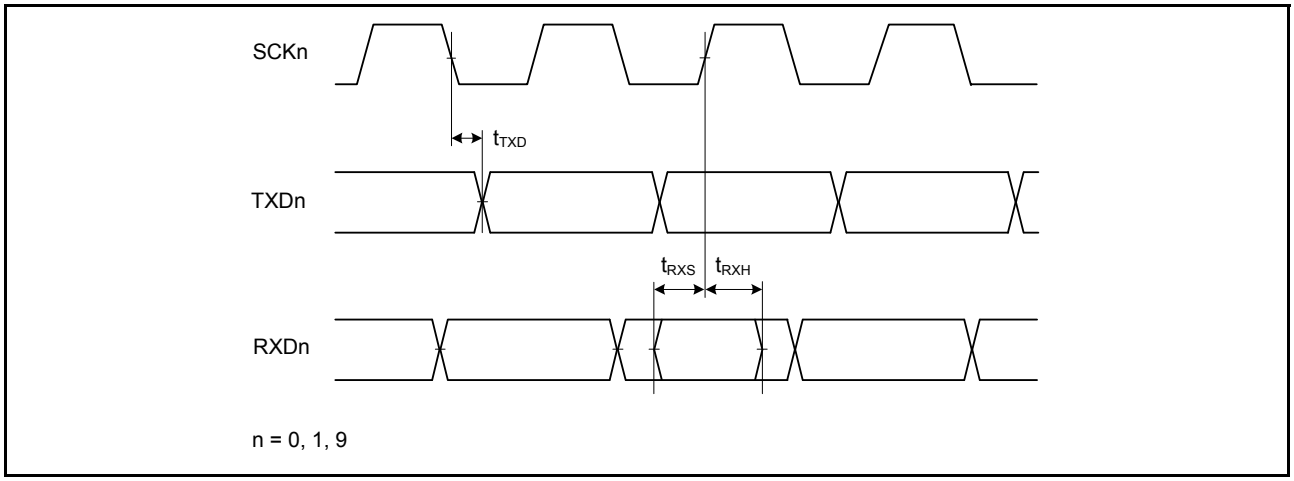


Figure 2.42 SCI input/output timing in clock synchronous mode

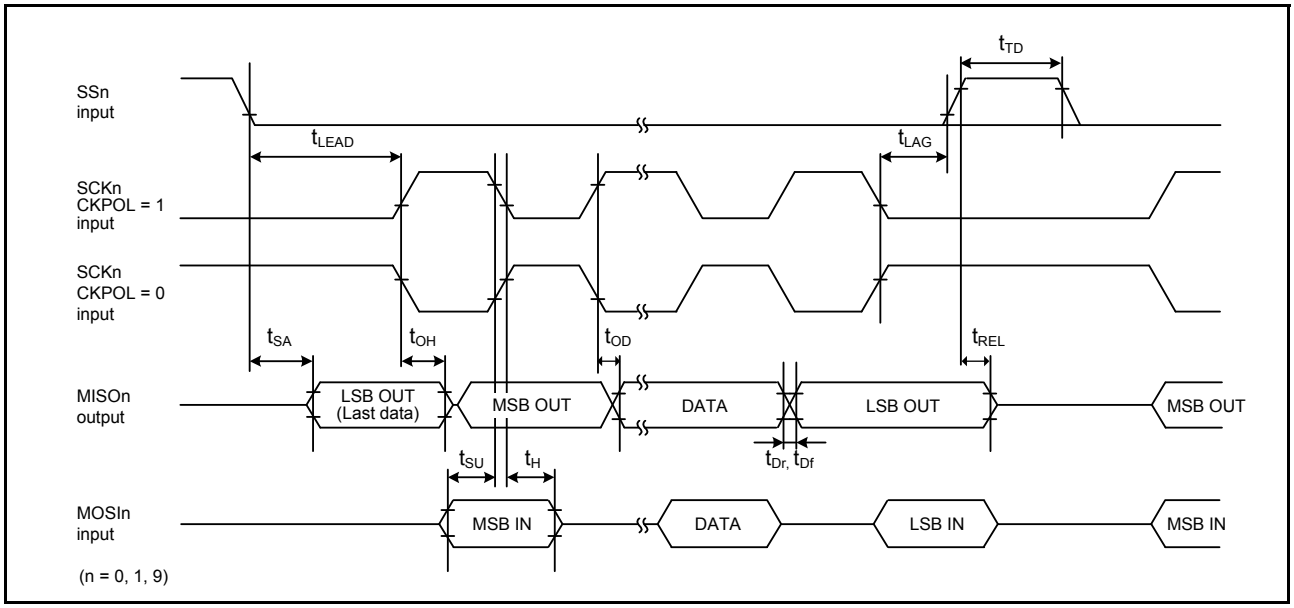


Figure 2.47 SCI simple SPI mode timing (slave, CKPH = 0)

Table 2.34 SCI timing (3)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	-	1000	ns	Figure 2.48
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	
Simple IIC*2 (Fast mode)	SDA input rise time	t_{Sr}	-	300	ns	Figure 2.48
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	

Note: t_{IICcyc}: Clock cycle selected by the SMR.CKS[1:0] bits.

Note 1. Cb indicates the total capacity of the bus line.

Note 2. Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

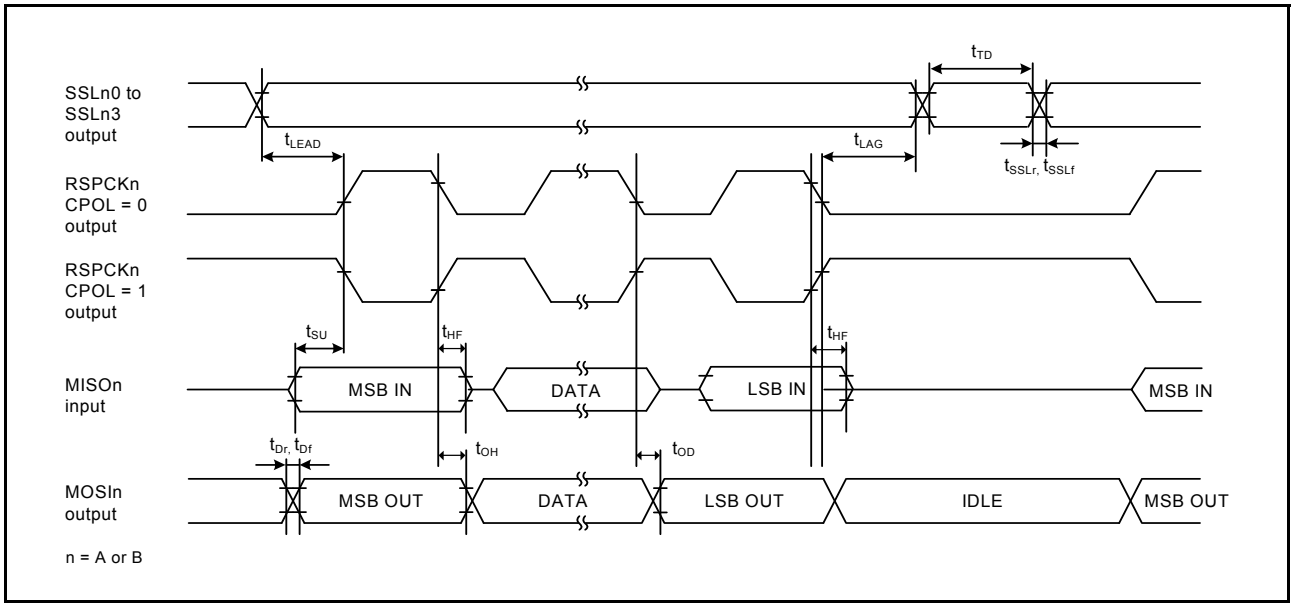


Figure 2.51 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to 1/2)

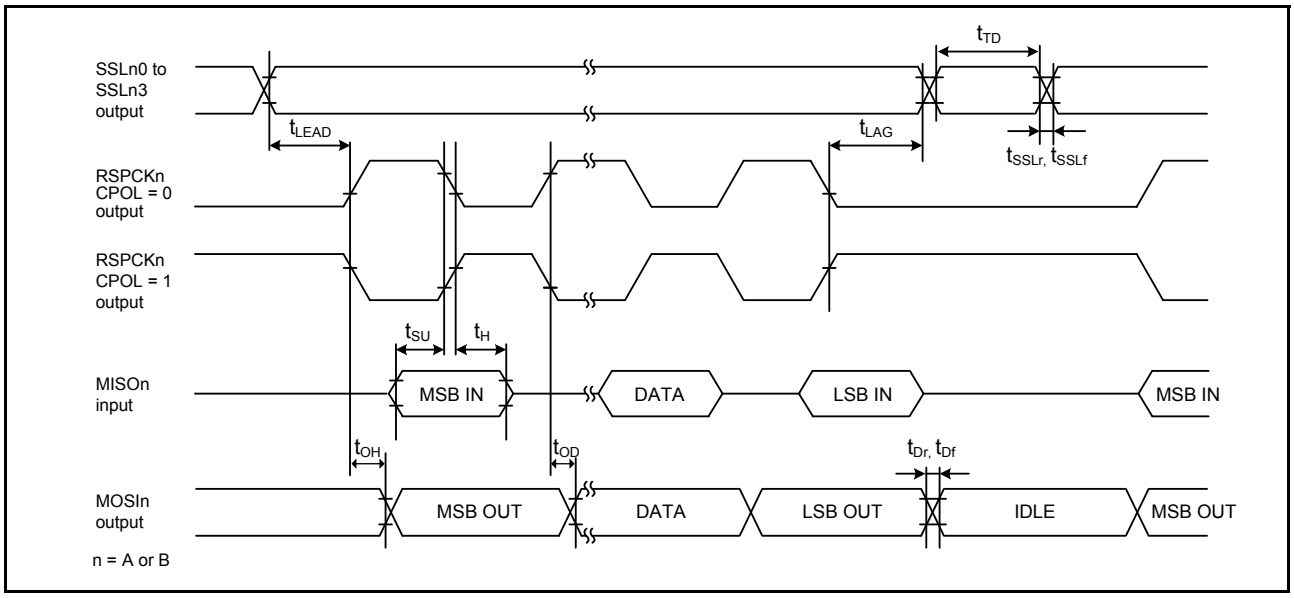


Figure 2.52 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to any value other than 1/2)

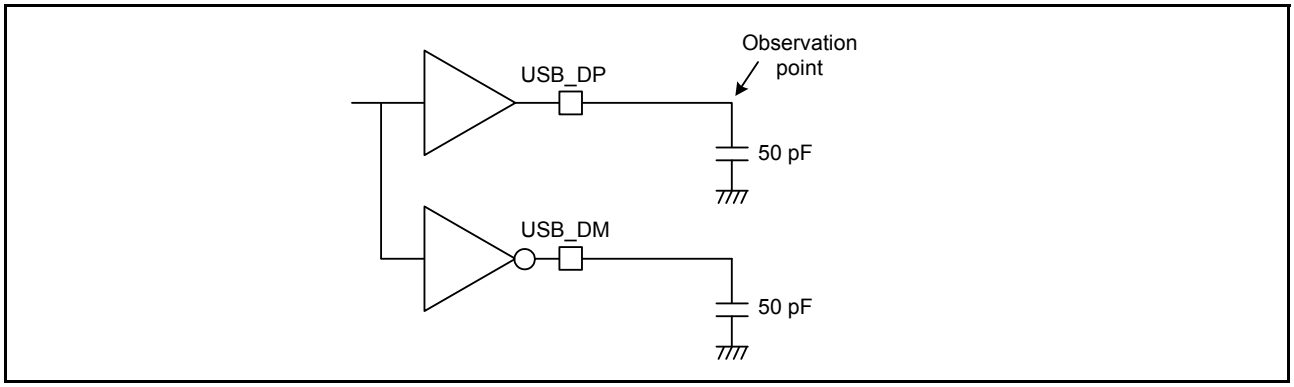


Figure 2.59 Test circuit for Full-Speed (FS) connection

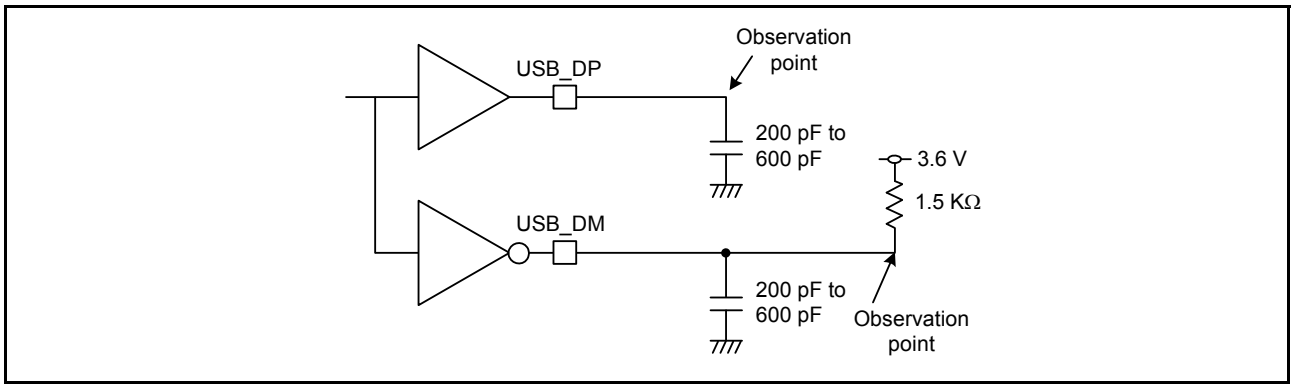


Figure 2.60 Test circuit for Low-Speed (LS) connection

2.4.2 USB External Supply

Table 2.39 USB regulator

Parameter		Min	Typ	Max	Unit	Test conditions
VCC_USB supply current	VCC_USB_LDO ≥ 3.8V	-	-	50	mA	-
	VCC_USB_LDO ≥ 4.5V	-	-	100	mA	-
VCC_USB supply voltage		3.0	-	3.6	V	-

2.5 ADC14 Characteristics

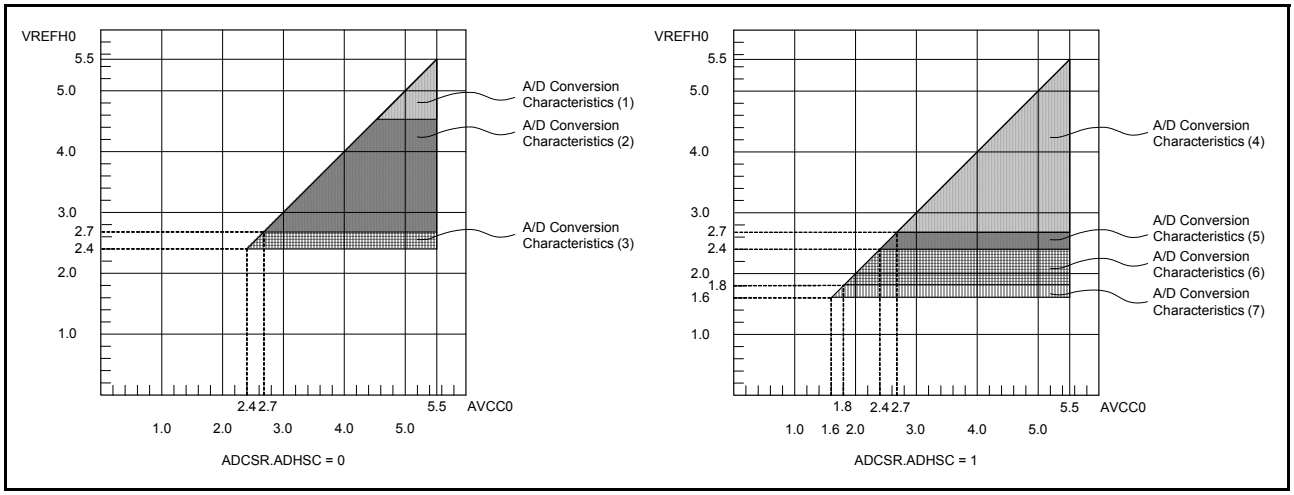


Figure 2.61 AVCC0 to VREFH0 voltage range

Table 2.40 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	64	MHz	-
Analog input capacitance*2	Cs	-	-	8*3	pF	High-precision channel
		-	-	9*3	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5*3	kΩ	High-precision channel
		-	-	6.7*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.70	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.13	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-

Table 2.53 Power-on reset circuit and voltage detection circuit characteristics (2) (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Power-on reset enable time	$t_{W\ (POR)}$	1	-	-	ms	Figure 2.67, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)	$T_{d\ (E-A)}$	-	-	300	µs	Figure 2.69, Figure 2.70
Hysteresis width (POR)	V_{PORH}	-	110	-	mV	-
Hysteresis width (LVD0, LVD1, and LVD2)	V_{LVH}	-	60	-	mV	LVD0 selected
		-	100	-		V_{det1_0} to V_{det1_2} selected.
		-	60	-		V_{det1_3} to V_{det1_9} selected.
		-	50	-		V_{det1_A} to V_{det1_B} selected.
		-	40	-		V_{det1_C} to V_{det1_F} selected.
		-	60	-		LVD2 selected

Note 1. When OFS1.LVDAS = 0
Note 2. When OFS1.LVDAS = 1
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

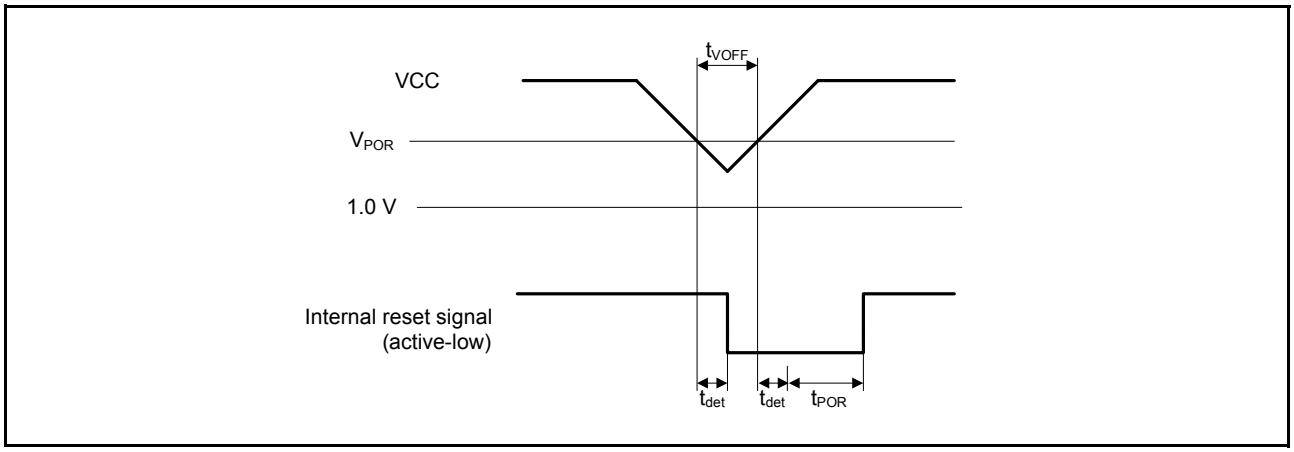
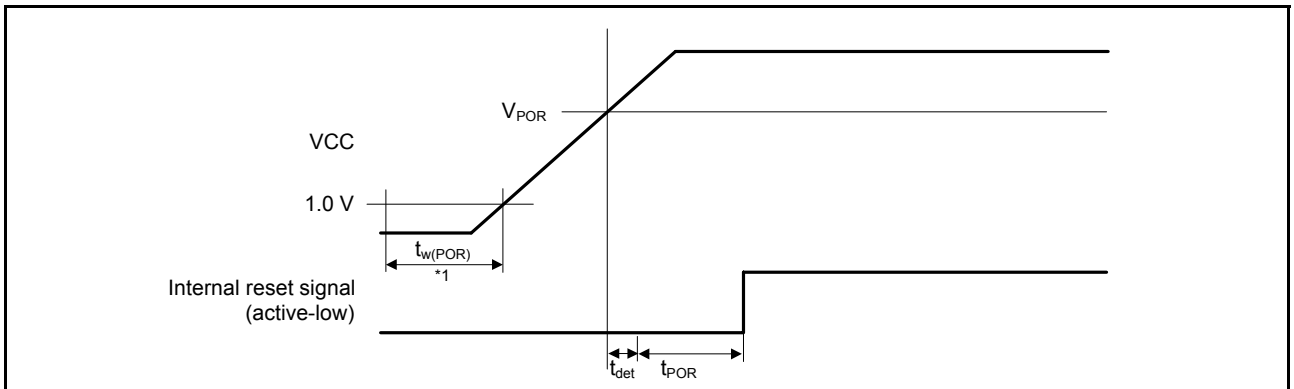


Figure 2.66 Voltage detection reset timing



Note: $t_{W(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{W(POR)}$ for 1.0 ms or more.

Figure 2.67 Power-on reset timing

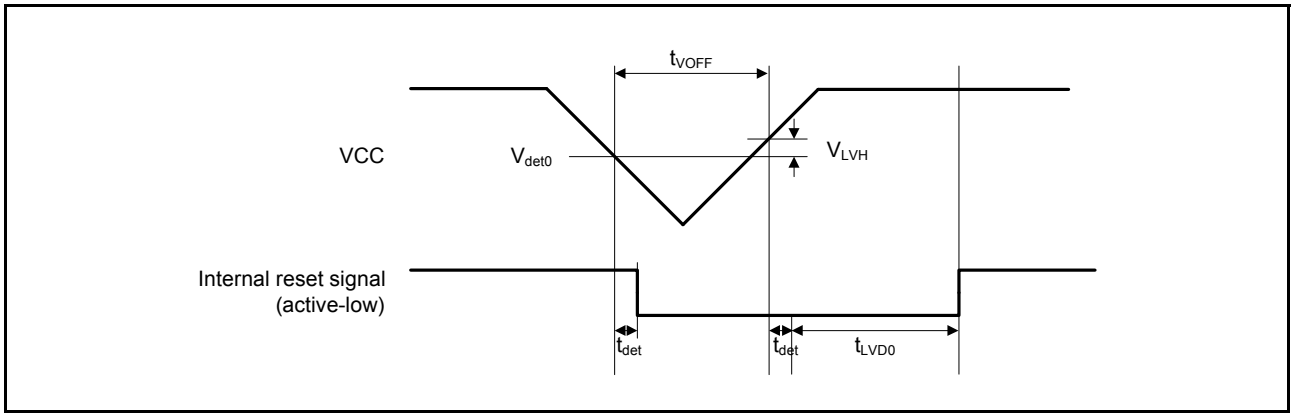


Figure 2.68 Voltage detection circuit timing (V_{det0})

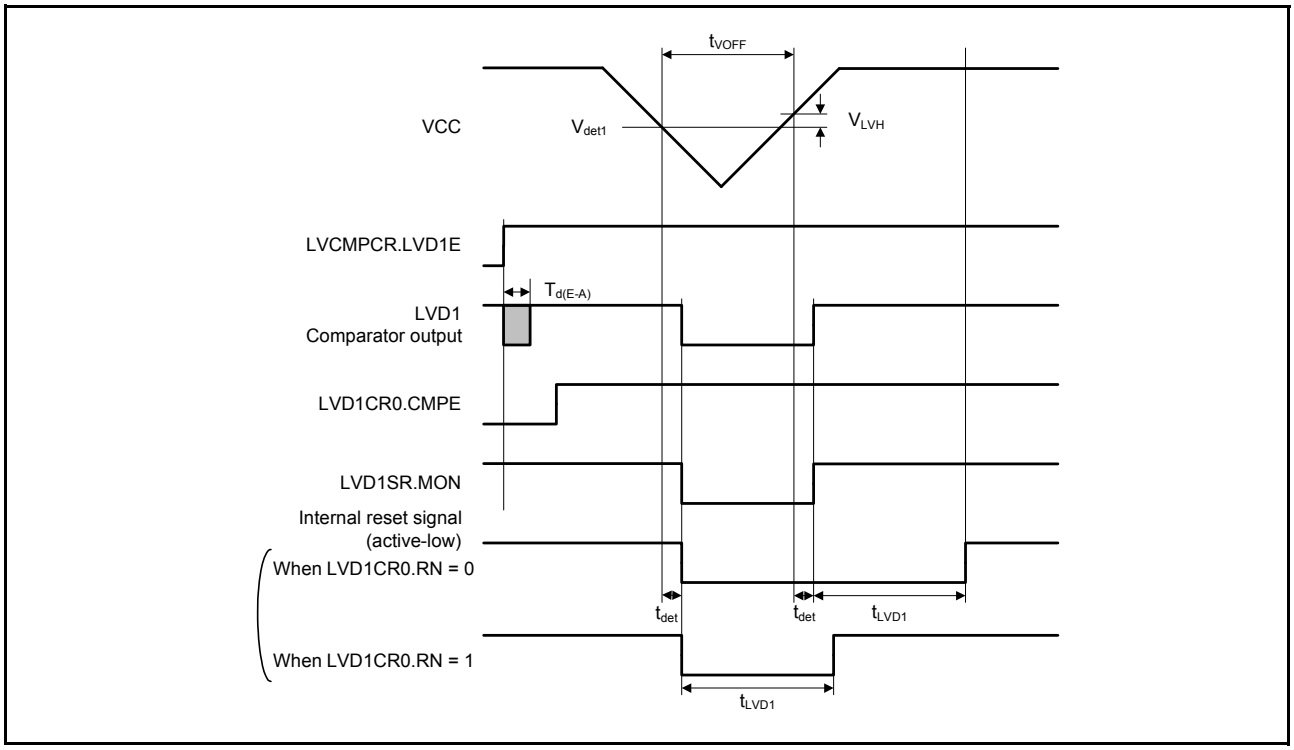
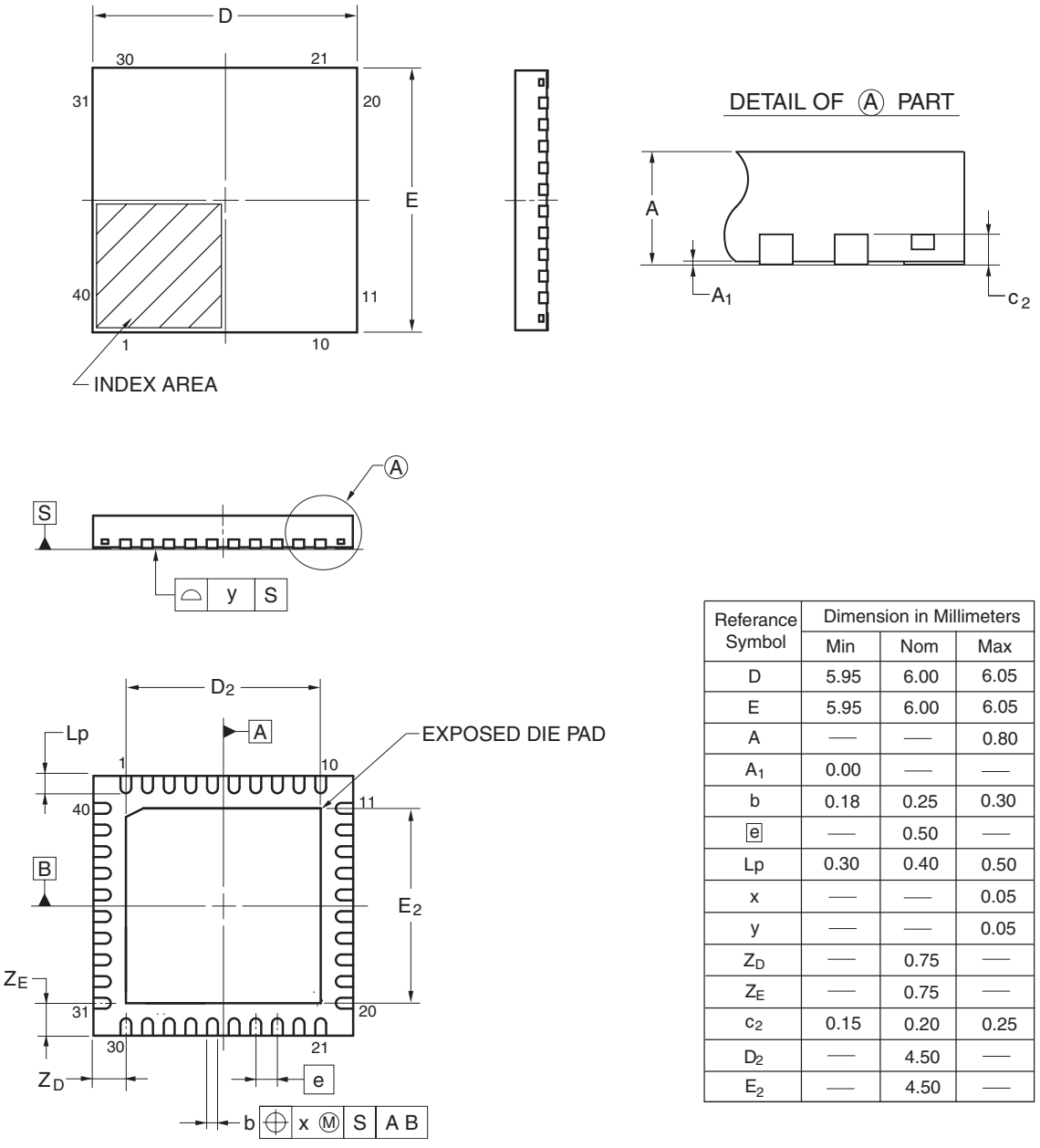


Figure 2.69 Voltage detection circuit timing (V_{det1})

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-5	0.09



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	5.95	6.00	6.05
E	5.95	6.00	6.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	4.50	—
E_2	—	4.50	—

Figure 1.6 QFN 40-pin

Renesas Synergy™ Platform
S124 Microcontroller Group

Renesas Electronics Corporation

R01DS0264EU0130